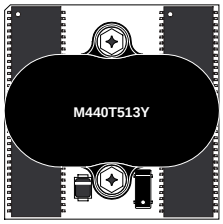
M440T513Y

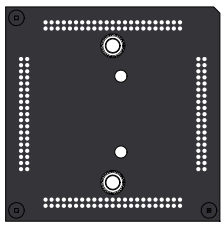
5.0V, 16 Mbit (512 Kbit x 32) TIMEKEEPER® SRAM

FEATURES SUMMARY

- 5.0V ± 10%
- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT, BATTERY, AND CRYSTAL
- PRECISION POWER MONITORING AND POWER SWITCHING CIRCUITRY
- AUTOMATIC WRITE-PROTECTION WHEN V_{CC} IS OUT-OF-TOLERANCE
- POWER-FAIL DESELECT VOLTAGE:
  - V_{CC} = 4.5 to 5.5V; 4.0V ≤ V_{PFD} ≤ 4.5V
- BATTERY LOW PIN ($\overline{BL}$)
- 5 YEARS OF DATA RETENTION AND CLOCK OPERATION IN THE ABSENCE OF POWER @ 45°C
- DUAL-BATTERY SNAPHAT® HOUSING IS REPLACEABLE
- 85ns SRAM CHIP ENABLE ACCESS (70ns ADDRESS ACCESS)
- SLEEP MODE FUNCTION
- 150ns CLOCK ACCESS

Figure 1. Package





168-ball PBGA
Module

TABLE OF CONTENTS

SUMMARY DESCRIPTION

The M440T513Y TIMEKEEPER® RAM is a 16Mbit, non-volatile static RAM organized as 512K by 32 bits and real time clock organized as 64 bytes by 8 bits. The special PBGA package provides a fully integrated battery back-up memory and real time clock solution. In the event of power instability or absence, a self-contained battery maintains the timekeeping operation and provides power for a CMOS static RAM. Control circuitry monitors V_{CC} and invokes write protection to prevent data corruption in the memory and RTC.

The clock keeps track of tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The last day of the month is automatically adjusted for months with less than 31 days, including leap year correction.

The clock operates in one of two formats:

– a 12-hour mode with an AM/PM indicator; or

– a 24-hour mode

The M440T513Y is a 168-ball PBGA module that integrates the RTC, the battery, and SRAM in one package.

Figure 2. Logic Diagram

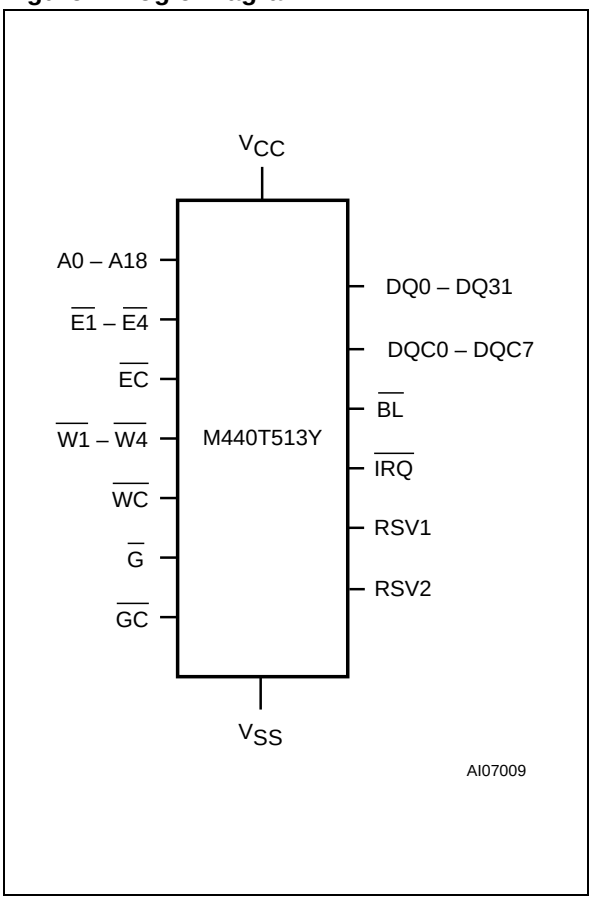
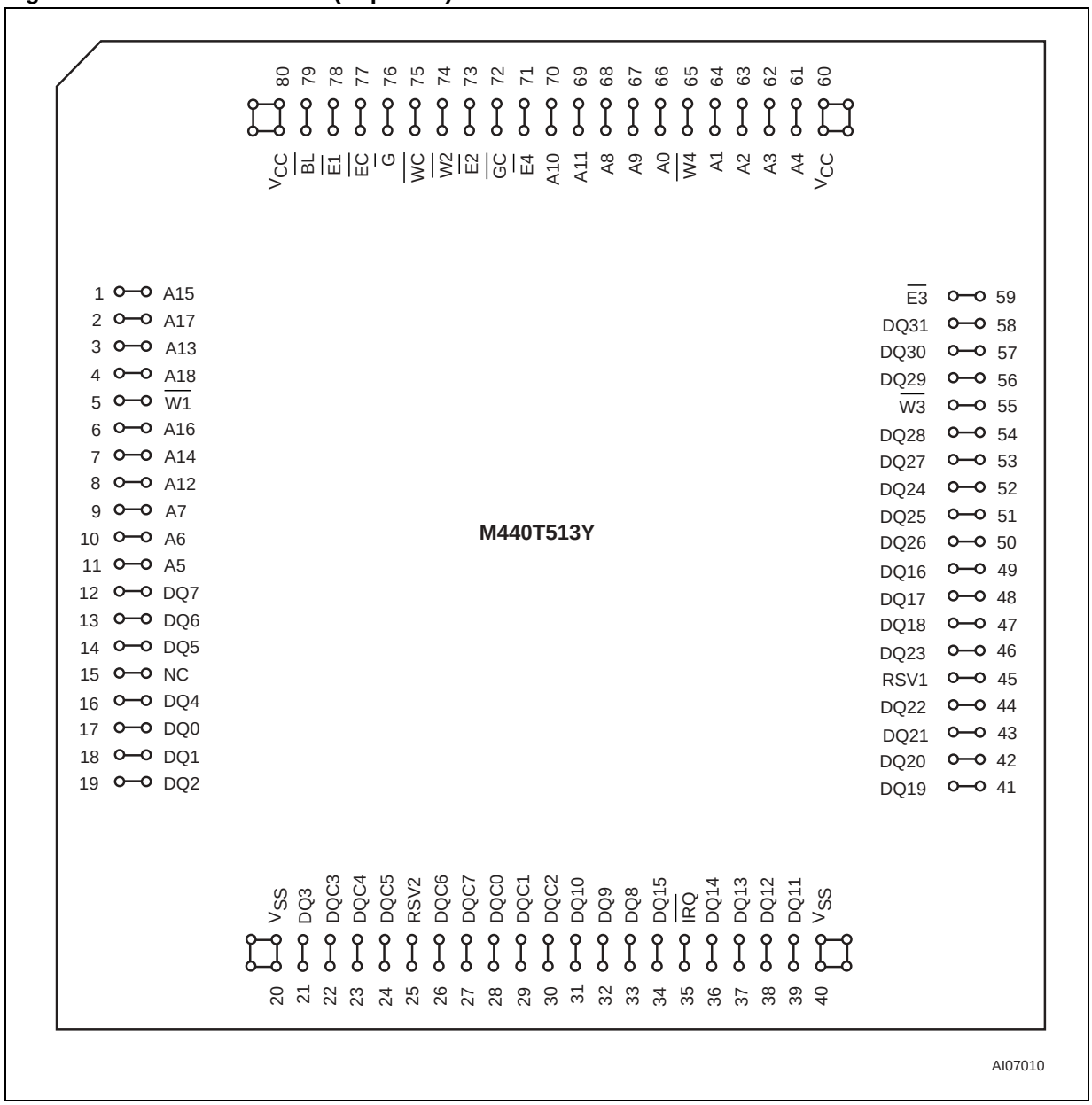


Table 1. Signal Names

A0 - A18	Address Inputs
DQ0 - DQ31	NVRAM Data Input/Output
DQC0 - DQC7	Clock Data Input/Output
$\overline{E1}$ - $\overline{E4}$	NVRAM Chip Enable Inputs
$\overline{EC}$	Clock Chip Enable Input
$\overline{W1}$ - $\overline{W4}$	NVRAM WRITE Enable Inputs
$\overline{WC}$	Clock WRITE Enable Input
$\overline{G}$	Output Enable Input
$\overline{GC}$	Clock Output Enable Input
$\overline{BL}$	Battery Low Output (Open Drain)
$\overline{IRQ}$	Interrupt Output (Open Drain)
RSV1	Reserved
RSV2	Reserved
NC	No Connect
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 3. PBGA Connections (Top View)



Note: This diagram is TOP VIEW perspective (view through package).

Figure 4. M440T513Y Hardware Hookup

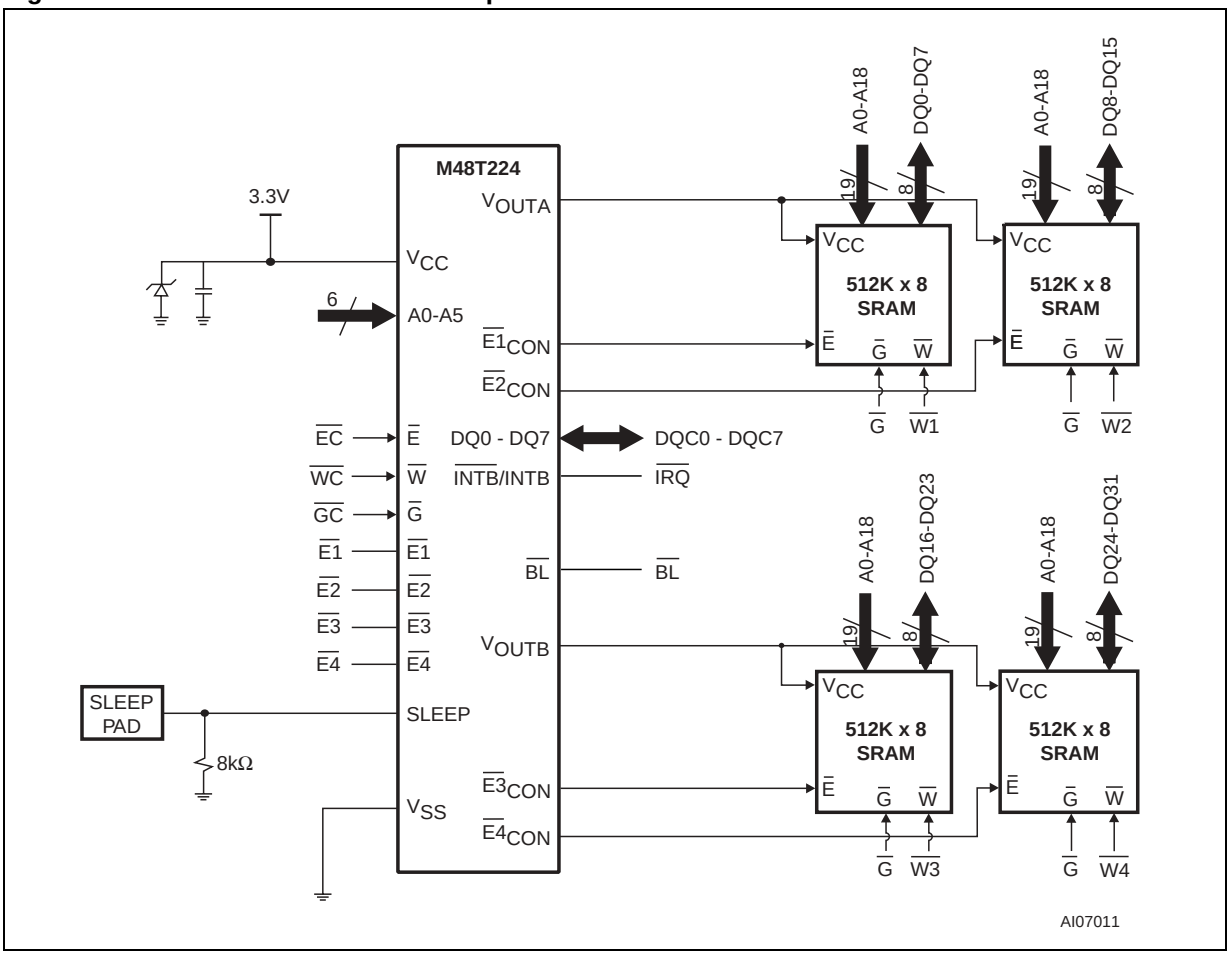
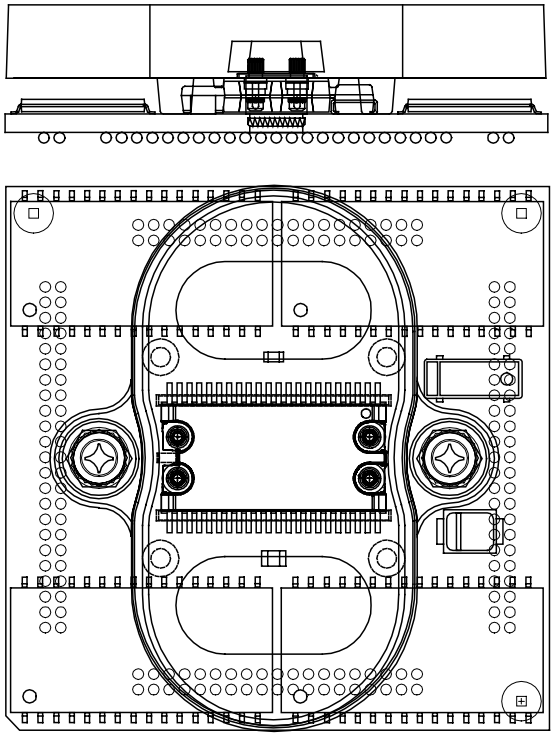


Figure 5. M440T513Y PBGA Module Solution (Side/Top)



OPERATION MODES

Memory READ Mode

The M440T513Y is in the 32-bit READ Mode whenever $\overline{W1}$ - $\overline{W4}$ (WRITE Enable Byte 1 to 4) are high and $\overline{E1}$ - $\overline{E4}$ – Chip Enable Bytes 1 to 4 are low (see Table 2., page 8). The unique address specified by the 19 address inputs defines which one of the 524,288 long words of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access Time (t_{AVQV}) after the last address input signal is stable, providing the $\overline{E1\text{-}4}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E1\text{-}4}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Times (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the thirty-two three-state Data I/O signals is controlled by $\overline{E1\text{-}4}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E1\text{-}4}$ and $\overline{G}$ remain active, output data will remain valid for Output Data Hold Time (t_{AXQX}) but will go indeterminate until the next Address Access.

Clock READ Mode

The clock is in the READ Mode whenever $\overline{WC}$ (Clock WRITE Enable) is high and $\overline{EC}$ (Clock Chip Enable) is low. The unique address specified by the 6 Address Inputs defines which one of the 64 bytes of clock data is to be accessed. Valid data will be available at the Data I/O pins (DQC0-7) within Address Access Time (t_{AVQV}) after the last address input signal is stable, providing the $\overline{EC}$ and $\overline{GC}$ access times are also satisfied. If the $\overline{EC}$ and $\overline{GC}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Times (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{EC}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{EC}$ and $\overline{G}$ remain active, output data will remain valid for Output Data Hold Time (t_{AXQX}) but will go indeterminate until the next Address Access. See section on Reading and Setting the Clock under CLOCK OPERATION for more details.

Table 2. Memory Operating Modes

Mode	V_{CC}	$\overline{E4}$	$\overline{E3}$	$\overline{E2}$	$\overline{E1}$	$\overline{G}$	$\overline{W4}$	$\overline{W3}$	$\overline{W2}$	$\overline{W1}$	DQ24-DQ31	DQ16-DQ23	DQ8-DQ15	DQ0-DQ7	Power
Byte WRITE	4.5 to 5.5V	H	H	H	L	H	X	X	X	L	Hi-Z	Hi-Z	Hi-Z	D_{IN}	Active
Byte WRITE		H	H	L	H	H	X	X	L	X	Hi-Z	Hi-Z	D_{IN}	Hi-Z	Active
Byte WRITE		H	L	H	H	H	X	L	X	X	Hi-Z	D_{IN}	Hi-Z	Hi-Z	Active
Byte WRITE		L	H	H	H	H	L	X	X	X	D_{IN}	Hi-Z	Hi-Z	Hi-Z	Active
Byte WRITE		X	X	X	L	H	H	H	H	L	Hi-Z	Hi-Z	Hi-Z	D_{IN}	Active
Byte WRITE		X	X	L	X	H	H	H	L	H	Hi-Z	Hi-Z	D_{IN}	Hi-Z	Active
Byte WRITE		X	L	X	X	H	H	L	H	H	Hi-Z	D_{IN}	Hi-Z	Hi-Z	Active
Byte WRITE		L	X	X	X	H	L	H	H	H	D_{IN}	Hi-Z	Hi-Z	Hi-Z	Active
Long Word WRITE		L	L	L	L	H	L	L	L	L	D_{IN}	D_{IN}	D_{IN}	D_{IN}	Active
Byte READ		H	H	H	L	L	X	X	X	H	Hi-Z	Hi-Z	Hi-Z	D_{OUT}	Active
Byte READ		H	H	L	H	L	X	X	H	X	Hi-Z	Hi-Z	D_{OUT}	Hi-Z	Active
Byte READ		H	L	H	H	L	X	H	X	X	Hi-Z	D_{OUT}	Hi-Z	Hi-Z	Active
Byte READ		L	H	H	H	L	H	X	X	X	D_{OUT}	Hi-Z	Hi-Z	Hi-Z	Active
Long Word READ		L	L	L	L	L	H	H	H	H	D_{OUT}	D_{OUT}	D_{OUT}	D_{OUT}	Active
Deselect		H	H	H	H	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Stdby
Deselect	V_{SO} to V_{PFD}(min)(1)	X	X	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	CMOS Standby
Deselect	≤ V_{SO}(1)	X	X	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage.

1. See Table 12., page 20 for details.

Table 3. Clock Operating Modes

Mode	V_{CC}	$\overline{EC}$	$\overline{GC}$	$\overline{WC}$	DQC0 - 7
Deselect	4.5 to 5.5V	V_{IH}	X	X	Hi-Z
WRITE		V_{IL}	X	V_{IL}	D_{IN}
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}
READ		V_{IL}	V_{IH}	V_{IH}	Hi-Z
Deselect	V_{SO} to V_{PFD}(min)(1)	X	X	X	Hi-Z
Deselect	≤ V_{SO}(1)	X	X	X	Hi-Z

Note: X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage.
1. See Table 12., page 20 for details.

Figure 6. Memory READ Mode AC Waveforms, Chip Enable- or Output Enable-Controlled

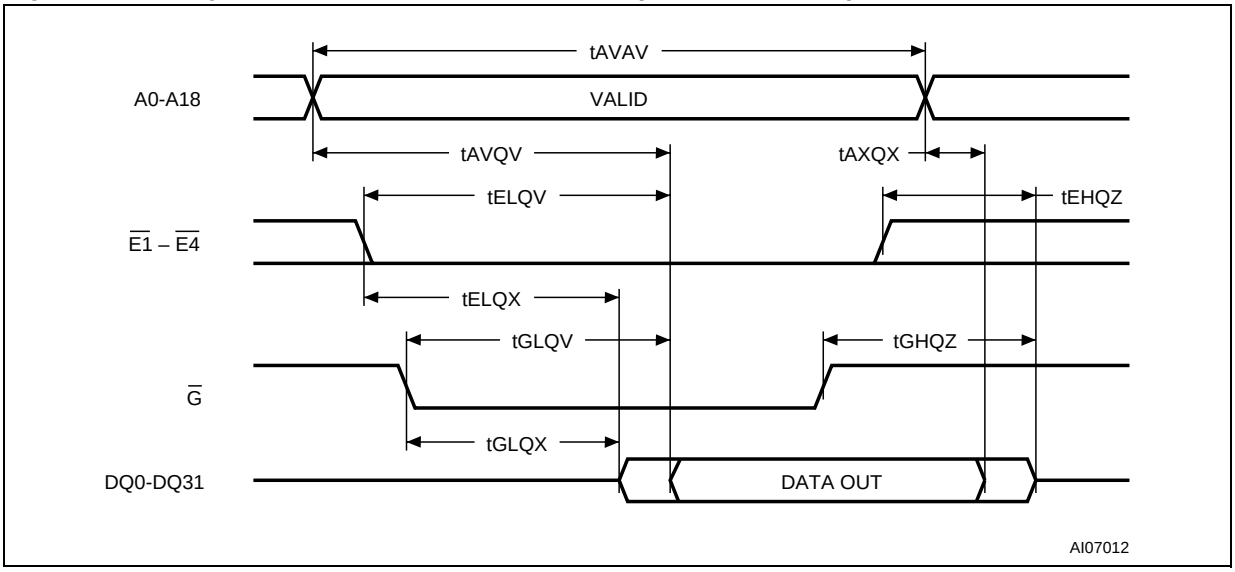


Figure 7. Memory READ Mode AC Waveforms, Address-Controlled

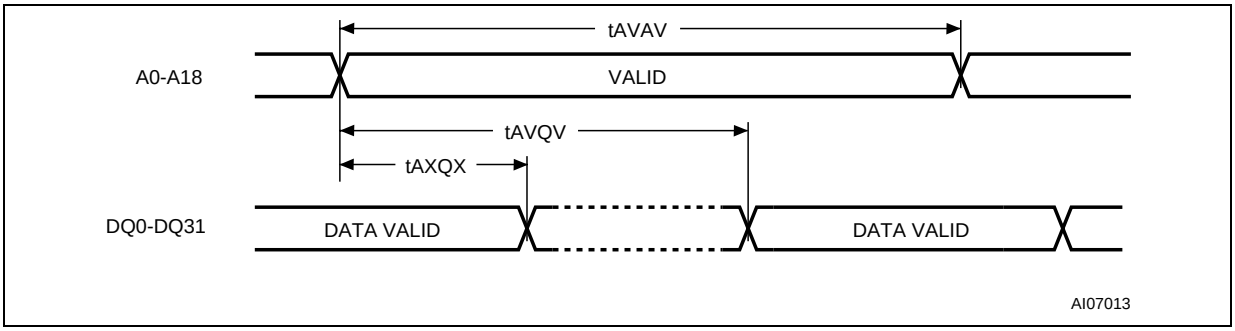


Figure 8. Clock READ Mode AC Waveforms, Chip Enable- or Output Enable-Controlled

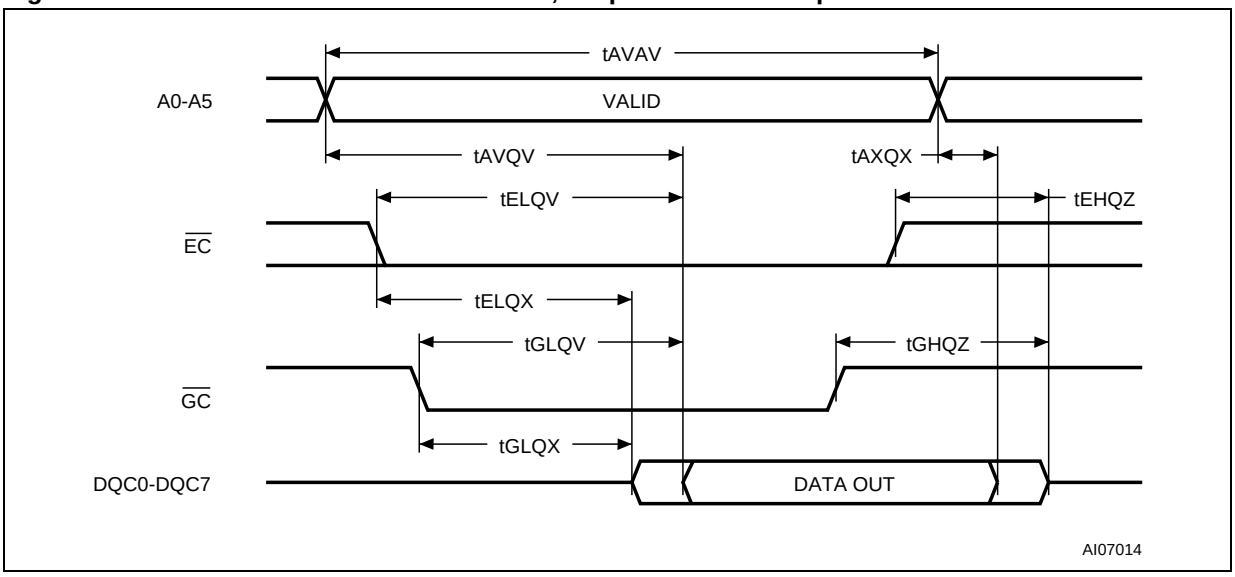


Figure 9. Clock READ Mode AC Waveforms, Address-Controlled

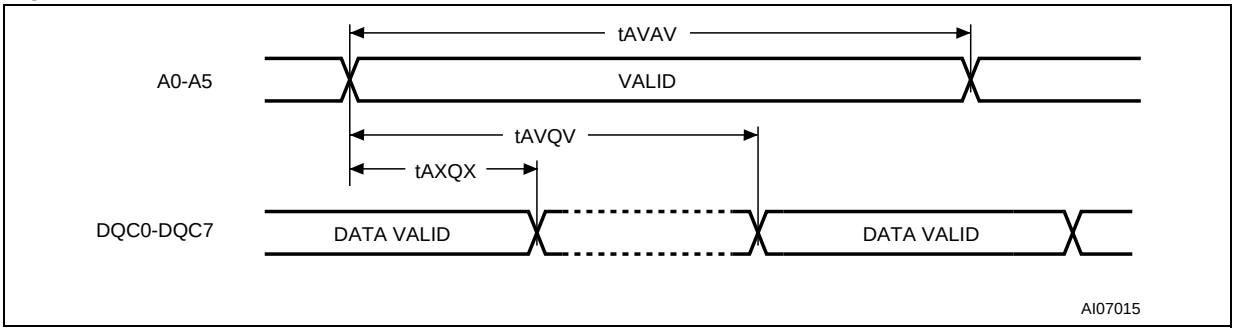


Table 4. Memory/Clock READ Mode AC Characteristics

Symbol		Parameter[1]	M440T513Y				Unit
			Memory		Clock		
			–85		–15		
			Min	Max	Min	Max	
t_{RC}	t_{AVAV}	READ Cycle Time	85		150		ns
t_{ACC}	t_{AVQV}	Address Valid to Output Valid		70		150	ns
t_{CO}	t_{ELQV}	Chip Enable Low to Output Valid		85		150	ns
t_{OE}	t_{GLQV}	Output Enable Low to Output Valid		55		70	ns
t_{COE}	t_{ELQX}	Chip Enable Low to Output Transition	5		10		ns
t_{COE}	t_{GLQX}	Output Enable Low to Output Transition	5		5		ns
t_{OD}	t_{EHQZ}[2]	Chip Enable High to Output Hi-Z		30		50	ns
t_{ODO}	t_{GHQZ}[2]	Output Enable High to Output Hi-Z		30		50	ns
t_{OH}	t_{AXQX}	Address Transition to Output Transition	5		5		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = –15 to 75°C; V_{CC} = 4.5 to 5.5V (except where noted).
2. C_L = 5pF.

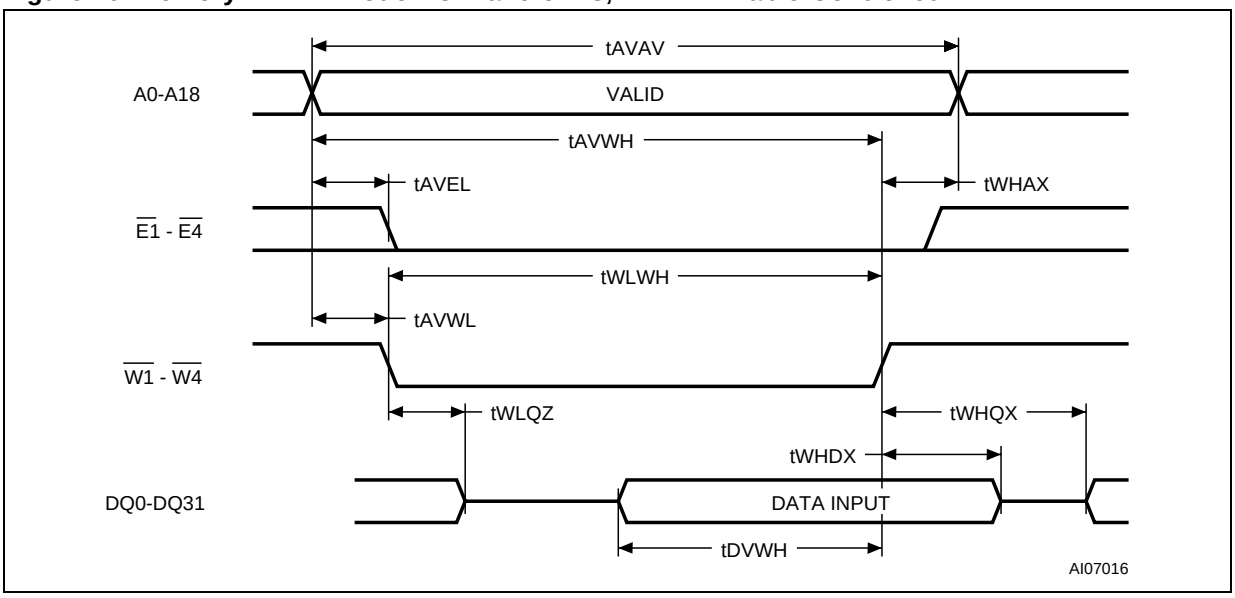
Memory WRITE Mode

The M440T513Y is in the WRITE Mode whenever any or all of $\overline{W1\text{-}4}$ (WRITE Enable Byte 1 to 4) and any corresponding $\overline{E1\text{-}4}$ are in a low state after the address inputs are stable. Thus a Byte WRITE (8-bit), Word WRITE (16-bit) or Long Word WRITE (32-bit) may be performed. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W1\text{-}4}$ or $\overline{E1\text{-}4}$. A WRITE is terminated by the earlier rising edge of $\overline{W1\text{-}4}$ or $\overline{E1\text{-}4}$. The addresses must be held valid throughout the cycle. $\overline{E1\text{-}4}$ or $\overline{W1\text{-}4}$ must return high for a minimum of t_{EHAX} from Chip Enable or t_{WHAX} from WRITE Enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E1\text{-}4}$ and $\overline{G}$, a low on $\overline{W1\text{-}4}$ will disable the outputs t_{WLQZ} after $\overline{W1\text{-}4}$ falls.

Clock WRITE Mode

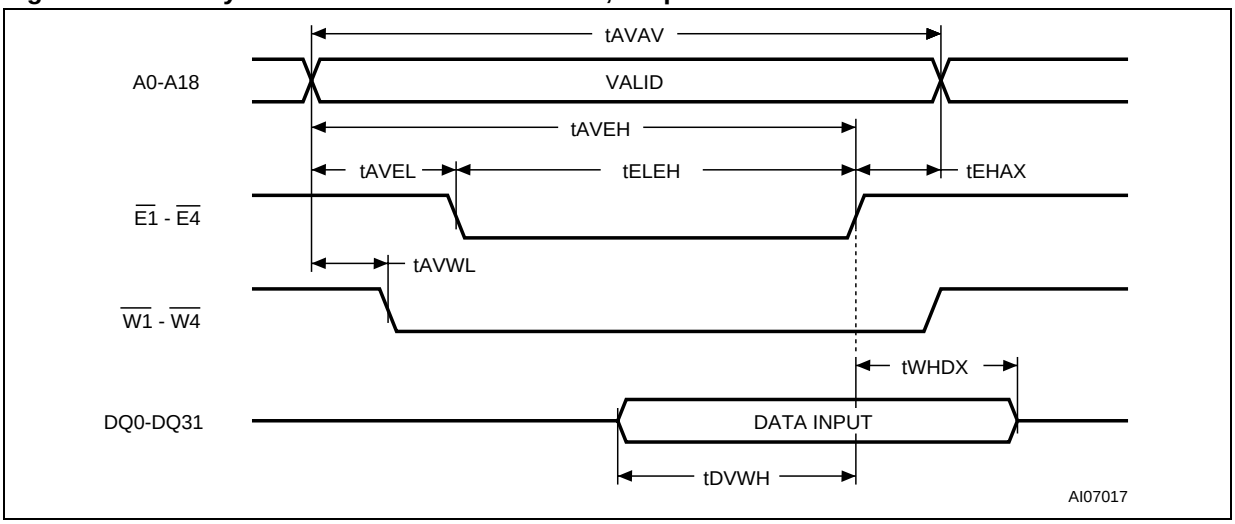
The clock is in the WRITE Mode whenever $\overline{WC}$ (Clock WRITE Enable) and $\overline{EC}$ (Clock Chip Enable) are in the low state after the address inputs are stable. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{WC}$ or $\overline{EC}$. A WRITE is terminated by the earlier rising edge of $\overline{WC}$ or $\overline{EC}$. The addresses must be held valid throughout the cycle. $\overline{EC}$ or $\overline{WC}$ must return high for a minimum of t_{EHAX} from Chip Enable Clock or t_{WHAX} from WRITE Enable Clock prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{GC}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{EC}$ and $\overline{GC}$ a low on $\overline{WC}$ will disable the outputs t_{WLQZ} after $\overline{WC}$ falls. See section on Reading and Setting the Clock under CLOCK OPERATION for more details.

Figure 10. Memory WRITE Mode AC Waveforms, WRITE Enable-Controlled



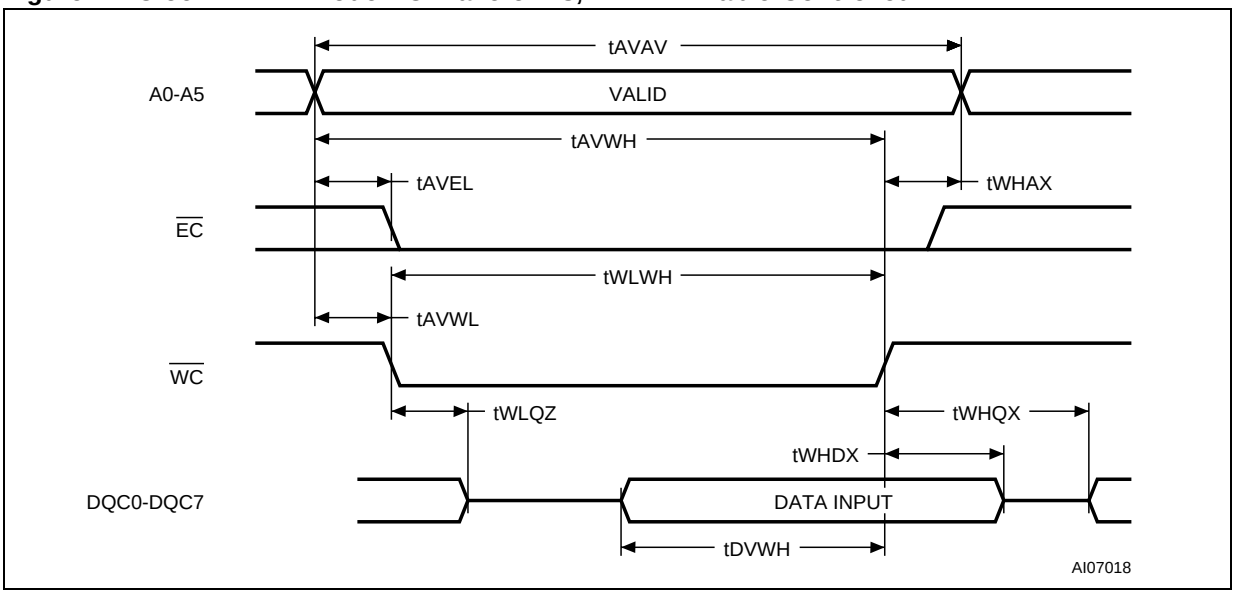
Note: Output Enable ($\overline{G}$) = Low

Figure 11. Memory WRITE Mode AC Waveforms, Chip Enable-Controlled



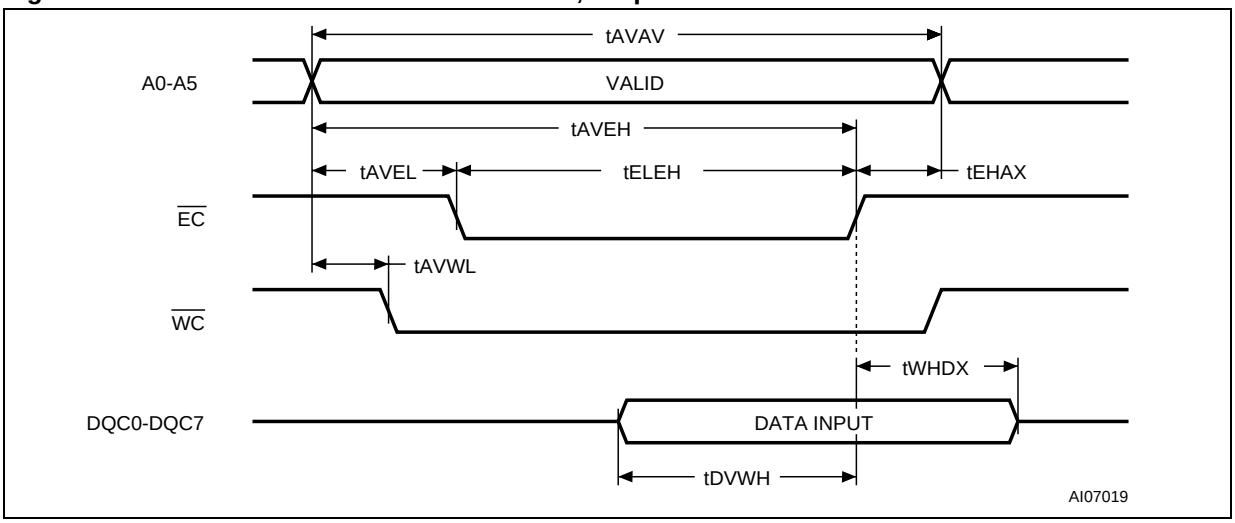
Note: Output Enable ($\overline{G}$) = High

Figure 12. Clock WRITE Mode AC Waveforms, WRITE Enable-Controlled



Note: Clock Output Enable ($\overline{GC}$) = Low

Figure 13. Clock WRITE Mode AC Waveforms, Chip Enable-Controlled



Note: Clock Output Enable ($\overline{GC}$) = High

Table 5. Memory/Clock WRITE Mode AC Characteristics

Symbol		Parameter[1]	M440T513Y				Unit
			Memory		Clock		
			–85		–15		
			Min	Max	Min	Max	
t_{WC}	t_{AVAV}	WRITE Cycle Time	85		150		ns
t_{AW}	t_{AVWL}	Address Valid to WRITE Enable Low	0		0		ns
t_{AW}	t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WP}	t_{WLWH}	WRITE Enable Pulse Width	60		100		ns
t_{WP}	t_{ELEH}	Chip Enable Low to Chip Enable High	65		150		ns
t_{WR}	t_{WHAX}	WRITE Enable High to Address Transition	5		10		ns
t_{WR}	t_{EHAX}	Chip Enable High to Address Transition	15		10		ns
t_{DS}	t_{DVWH}	Input Valid to WRITE Enable High	35		50		ns
t_{DS}	t_{DVEH}	Input Valid to Chip Enable High	35		50		ns
t_{DH}	t_{WHDX}	WRITE Enable High to Input Transition	5		0		ns
t_{DH}	t_{EHDX}	Chip Enable High to Input Transition	15		0		ns
t_{ODW}	t_{WLQZ}[2]	WRITE Enable Low to Output Hi-Z		30		50	ns
	t_{AVWH}	Address Valid to WRITE Enable High	70		150		ns
	t_{AVEH}	Address Valid to Chip Enable High	70		150		ns
t_{OEW}	t_{WHQX}	WRITE Enable High to Output Transition	5		5		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = –15 to 75°C; V_{CC} = 4.5 to 5.5V (except where noted).
2. C_L = 5pF.

CLOCK OPERATION

Clock Registers

Registers 00h, 01h, 02h, 04h, 06h, 08h, 09h, and 0Ah contain the time of day data in BCD. Eleven bits within these eight registers are not used and will always read '0' regardless of how they are written. Bits 6 and 7 in the Months Register (09h) are binary bits. When set to logic '0,' $\overline{EOSC}$ (Bit 7) enables the Real Time Clock oscillator. This bit will normally be turned on by the user during device initialization. However, the oscillator can be turned on and off as necessary by setting this bit to the appropriate level. Bit 6 of the Hours Register is defined as the 12- or 24-hour select bit. When set to logic '1,' the 12-hour format is selected. In the 12-hour format, Bit 5 is the AM/PM bit with logic '1' being PM. In the 24-hour mode, Bit 5 is the second 10-hour bit (20-23 hours). The Clock Registers are updated every 0.01 seconds from the Real Time Clock, except when the TE Bit (Bit 7 of Register 0Bh) is set low or the clock oscillator is not running.

Reading and Setting the Clock

The preferred method of synchronizing data access to and from the TIMEKEEPER® is to access the Command Register by doing a WRITE cycle to address location 0Bh and setting TE Bit (Transfer Enable Bit) to a logic '0.' This will freeze the External Clock Registers at the present recorded time, allowing access to occur without danger of simultaneous update. When the clock registers have been read or written, a second WRITE cycle to location 0Bh and setting the TE Bit to a logic '1' will put the Clock Registers back to being updated every 0.01 second. No time is lost in the Real Time Clock because the internal copy of the Clock Register buffers is continually incremented while the external memory registers are frozen. An alternate method of reading and writing the Clock Registers is to ignore synchronization. However, any single READ may give erroneous data as the Real Time Clock may be in the process of updating the external memory registers as data is being read. The internal copies of seconds through years are incremented, and the time of day alarm is checked during the period that hundreds of seconds reads “99” to “00.” A way of making sure data is valid is to do multiple READs and compare. Writing the registers can also produce erroneous results for the same reasons. A way of making sure that the WRITE cycle has caused proper update is to do a READ to verify and re-execute the WRITE cycle if data is not correct. While the possibility of erroneous results from READ and WRITE cycles has been stated, it is worth noting that the probability of an incorrect result is kept to a minimum due to the redundant structure of the TIMEKEEPER.

Clock Alarm Registers

Registers 03h, 05h, and 07h contain the Clock Alarm Registers. Bits 3, 4, 5, and 6 of Register 07h will always read '0' regardless of how they are written. Bit 7 of Registers 03h, 05h, and 07h are mask bits (see Table 6., page 15). When all of the mask bits are logic '0,' a Clock Alarm will only occur when Registers 02h, 04h, and 06h match the values stored in Registers 03h, 05h, and 07h. An alarm will be generated every day when Bit 7 of Register 07h is set to a logic '1.' Similarly, an alarm is generated every hour when Bit 7 of Registers 07h and 05h is set to a logic '1.' When Bit 7 of Registers 07h, 05h, and 03h is set to a logic '1,' an alarm will occur every minute when Register 1 (seconds) rolls from “59” to “00.”

Clock Alarm Registers are written and read in the same format as the Clock Registers. The Clock Alarm Flag and Interrupt are always cleared when alarm Registers are read or written.

Watchdog Alarm Registers

Registers 0Ch and 0Dh contain the time for the watchdog alarm. The two registers contain a time count from 00.01 to 99.99 seconds in BCD. The value written into the Watchdog Alarm Registers can be written or read in any order. Any access to Register 0Ch or 0Dh will cause the watchdog alarm to re-initialize and clears the Watchdog Flag Bit and the Watchdog Interrupt Output. When a new value is entered or the Watchdog Registers are read, the watchdog timer will start counting down from the entered value to zero. When zero is reached, the Watchdog Interrupt Output will go to the active state. The watchdog timer countdown is interrupted and re-initialized back to the entered value every time either of the registers are accessed. In this manner, controlled periodic accesses to the watchdog timer can prevent the watchdog alarm from going to an active level. If access does not occur, the countdown alarm will be repetitive. The Watchdog Alarm Registers always read the entered value. The actual countdown register is internal and is not readable. Writing registers 0Ch and 0Dh to '0' will disable the watchdog alarm feature.

Table 6. Register Map

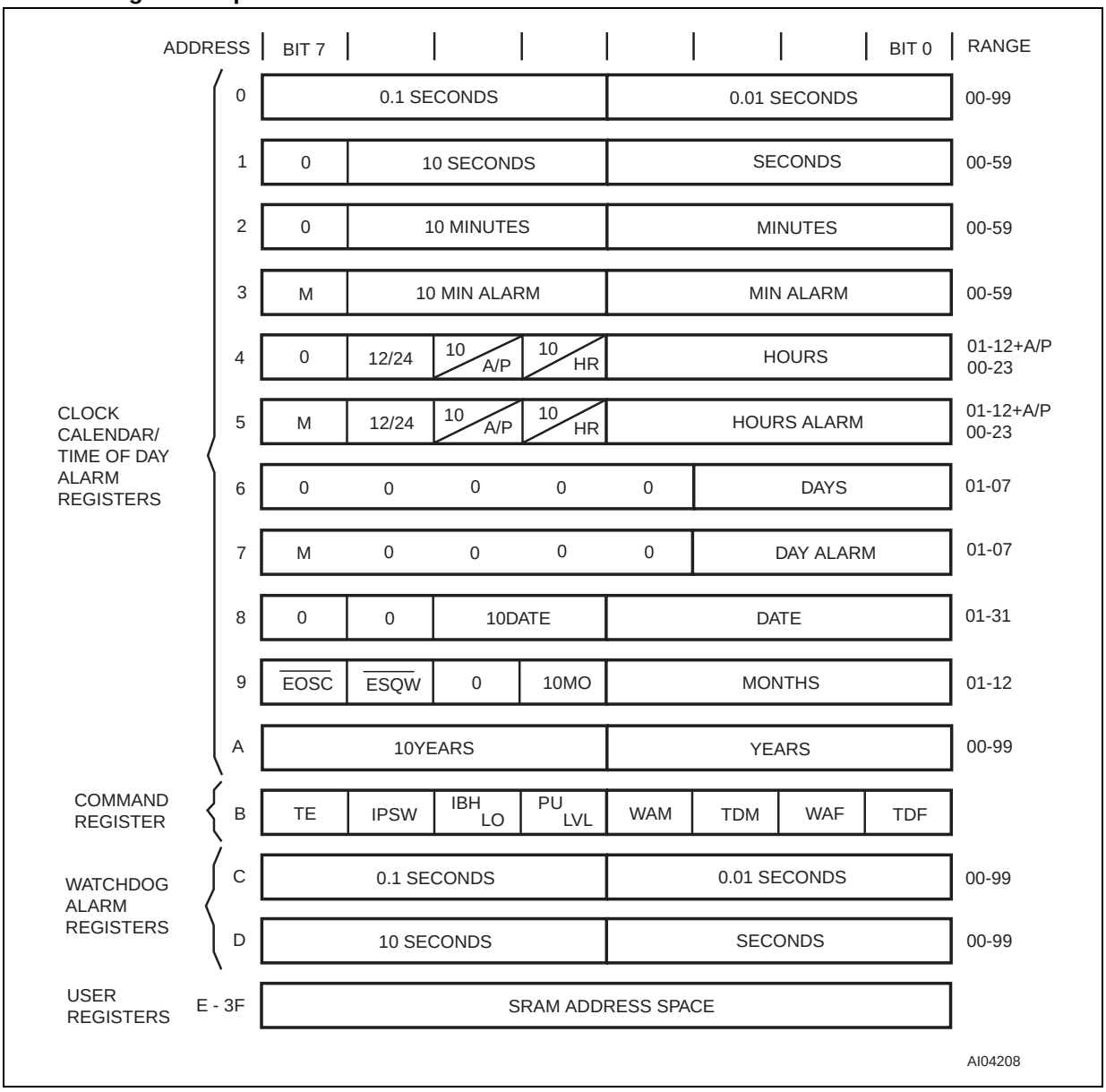


Table 7. Time of Day Alarm Mask Bits

Register			
(03h) Minutes	**(05h) Hours**	**(07h) Days**	
1	1	1	Alarm once per minute
0	1	1	Alarm when minutes match
0	0	1	Alarm when hours and minutes match
0	0	0	Alarm when hours, minutes, and days match

Note: Any other bit combinations of mask bit settings produce an illegal operation.

Command Register

Address location 0Bh is the Command Register where mask bits, control bits, and flag bits reside. The operation of each bit is as follows:

TE - Bit 7 Transfer Enable. This bit, when set to logic '0,' will disable the transfer of data between internal and external clock registers. The contents in the external clock registers are now frozen and READs or WRITEs will not be affected with updates. This bit must be set to a logic '1' to allow updates.

IPSW - Bit 6 Interrupt Switch. When set to a logic '1,' IRQ/($\overline{IRQ}$) is the Watchdog Alarm. When set to a logic '0,' IRQ/($\overline{IRQ}$) is the time of day alarm output.

IBH/LO - Bit 5 $\overline{IRQ}$ Sink or Source Current. When this bit is set to a logic '1' and V_{CC} is applied, IRQ/($\overline{IRQ}$) will source current (see Table 11., page 19, I_{OH}). When this bit is set to a logic '0,' IRQ will sink current (see Table 11., page 19, I_{OL}).

PU/LVL - Bit 4 Interrupt Pulse Mode or Level Mode. This bit determines whether the interrupt will output a pulse or level signal. When set to a logic '0,' IRQ/($\overline{IRQ}$) will be in the level mode. When this bit is set to a logic '1,' the pulse mode is selected. IRQ/($\overline{IRQ}$) will either sink or source current, depending on the condition of Bit 5, for a minimum of 3ms and then release. IRQ will only source current when there is voltage present on V_{CC}.

WAM - Bit 3 Watchdog Alarm Mask. When this bit is set to a logic '0,' the watchdog interrupt output will be activated. The activated state is determined by bits 1, 4, 5, and 6 of the Command Register. when this bit is set to a logic '1,' the watchdog interrupt output is deactivated.

TDM - Bit 2 Time of Day Alarm Mask. When this bit is set to a logic '0,' the time of day alarm interrupt output will be activated. The activated state is determined by bits 0, 4, 5, and 6 of the Command Register. When this bit is set to a logic '1,' the time of day alarm interrupt output is deactivated.

WAF - Bit 1 Watchdog Alarm Flag. This bit is set to a logic '1' when a watchdog alarm interrupt occurs. This bit is “Read only.” The bit is reset when any of the watchdog alarm registers are accessed.

When the interrupt is in the pulse mode (see PU/LVL - Bit 4 Interrupt Pulse Mode or Level Mode), this flag will be in the logic '1' state only during the time the interrupt is active.

TDF - Bit 0 Time of Day Flag. This is a “Read only” bit. This bit is set to a logic '1' when a time of day alarm has occurred. the time the alarm occurred can be determined by reading the time of day alarm registers. This bit is reset to a logic '0' state when any of the time of day registers are accessed.

When the interrupt is in the pulse mode (see PU/LVL - Bit 4 Interrupt Pulse Mode or Level Mode), this flag will be in the logic '1' state only during the time the interrupt is active.

Battery Low

The M440T513Y automatically performs battery voltage monitoring upon power-up, and at factory-programmed time intervals of at least 24 hours. The Battery Low ($\overline{BL}$) signal will be asserted if the battery voltage is found to be less than approximately 2.5V. The $\overline{BL}$ signal will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval (see application note, “AN1540, NVRAM PBGA Dual Battery Hat Mounting and Removal” for more information).

If a battery low is generated during a power-up sequence, this indicates that the battery is below 2.5V and may not be able to maintain data integrity in the SRAM. Data should be considered suspect, and verified as correct. Fresh batteries should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that one of the batteries is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied. In order to insure data integrity during subsequent periods of battery back-up mode, the batteries should be replaced. The SNAPHAT® top should be replaced with valid V_{CC} applied to the device.

The M440T513Y only monitors the batteries when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique. The $\overline{BL}$ signal is an open drain output and an appropriate pull-up resistor should be chosen to control the rise time.

Sleep Mode

Forcing the sleep pad more positive than +7.5V above ground will cause the batteries to be isolated from the RAM, preserving the remaining battery life. This mode may be used when device operation is not necessary for an extended period of time.

Note: Implementation of this Sleep Mode will result in complete loss of data.

MAXIMUM RATINGS

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 8. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Operating Temperature	–15 to 75	°C
T_{STG}	Storage Temperature (V_{CC}, Oscillator Off)	–40 to 85	°C
T_{SLD}	Lead Solder Temperature for 10 seconds	260	°C
V_{CC}	Supply Voltage (on any pin relative to Ground)	–0.3 to + 7.0	V
V_{IO}	Input or Output Voltages	–0.3 to V_{CC} + 0.3	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

CAUTION! *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up Mode*

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 9. DC and AC Measurement Conditions

Parameter	M440T513Y
V_{CC} Supply Voltage	4.5 to 5.5V
Ambient Operating Temperature	–15 to 75°C
Load Capacitance (C_L)	50pF
Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 14. AC Testing Load Circuit

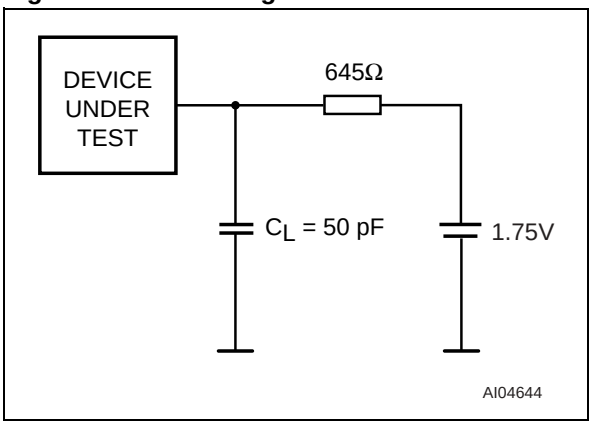


Table 10. Capacitance

Symbol	Parameter(1,2)		M440T513Y		Unit
			Min	Max	
C_{IN}	Input Capacitance	A0 - A5		50	pF
		A6 - A18, $\overline{G}$		40	pF
		All Other Inputs		10	pF
C_{OUT}	Output Capacitance ($\overline{BL}$)			10	pF
C_{IO}(3)	Input / Output Capacitance			10	pF

Note: 1. Effective capacitance measured with power supply at 3V; sampled only; not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs were deselected.

Table 11. DC Characteristics

Sym	Parameter	Test Condition(1)	M440T513Y			Unit
			Min	Typ	Max	
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$			±4	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$			±4	µA
I_{CC1}	Supply Current				385	mA
I_{CC2}	Supply Current (TTL Standby)	$\overline{E1\text{-}4}$, $\overline{EC} = V_{IH}$			20	mA
I_{CC3}	V_{CC} Power Supply Current	$\overline{E1\text{-}4}$, $\overline{EC} = V_{CCI} - 0.2$		2	3	mA
V_{IL}(2)	Input Low Voltage		–0.3		0.8	V
V_{IH}(2)	Input High Voltage		2.2		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA			0.4	V
	Output Low Voltage (Open drain)(3)	I_{OL} = 10mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1.0mA	2.4			V
V_{PFD}(2)	Power Fail Deselect		4.0		4.50	V
V_{SO}(2)	Battery Back-up Switchover			V_{BAT}		V

Note: 1. Valid for Ambient Operating Temperature: T_A = –15 to 75°C; V_{CC} = 4.5 to 5.5V (except where noted).
2. All voltages are referenced to Ground.
3. For $\overline{BL}$ and $\overline{IRQ}$ (Open drain); if pulled-up to supply other than V_{CC}, this supply must be equal to, or less than 3.0V when V_{CC} = 0V (during battery back-up mode).

Data Retention Mode

Should the supply voltage decay, the RAM will automatically deselect, write protecting itself when V_{CC} falls between V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance and all inputs are treated as “Don't care.”

Note: A power failure during a WRITE cycle may corrupt data at the current addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M440T513Y may respond to transient noise spikes on V_{CC} that cross into the deselect window during the time the device is sampling V_{CC}.Therefore, decoupling of the power supply lines is recommended. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery, preserving data and powering the clock. The internal energy source will maintain data in the M440T513Y for an accumulated period of at least 5 years at 45°C. As system power rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD} (min) plus t_{ER} (min). Normal RAM operation can resume t_{ER} after V_{CC} exceeds V_{PFD} (max). Refer to Application Note (AN1012) on the ST Web Site for more information on battery life.

Figure 15. Power Down/Up Mode AC Waveforms

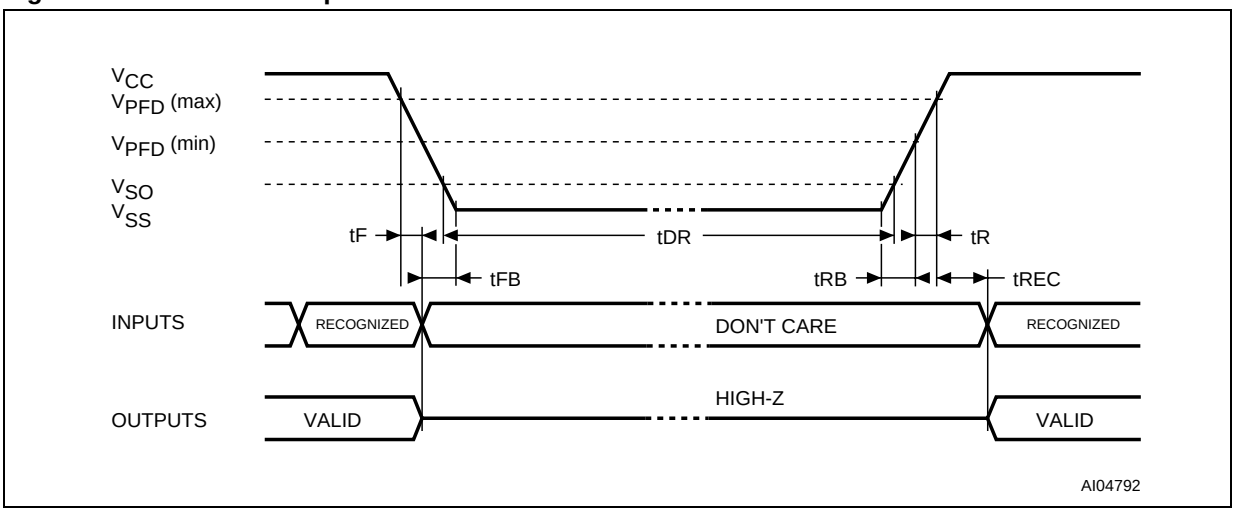


Table 12. Power Down/Up Trip Points DC Characteristics

Symbol	Parameter[1,2]	M440T513Y			Unit
		Min	Typ	Max	
V_{PFD}	Power-fail Deselect Voltage	4.0		4.5	V
V_{SO}	Battery Back-up Switchover Voltage		V_{BAT}		V
t_{DR}[3]	Expected Data Retention Time	5			YEARS

Note: 1. Valid for Ambient Operating Temperature: T_A = –15 to 75°C; V_{CC} = 4.5 to 5.5V (except where noted).
2. All voltages referenced to V_{SS}.
3. At 45°C, V_{CC} = 0V.

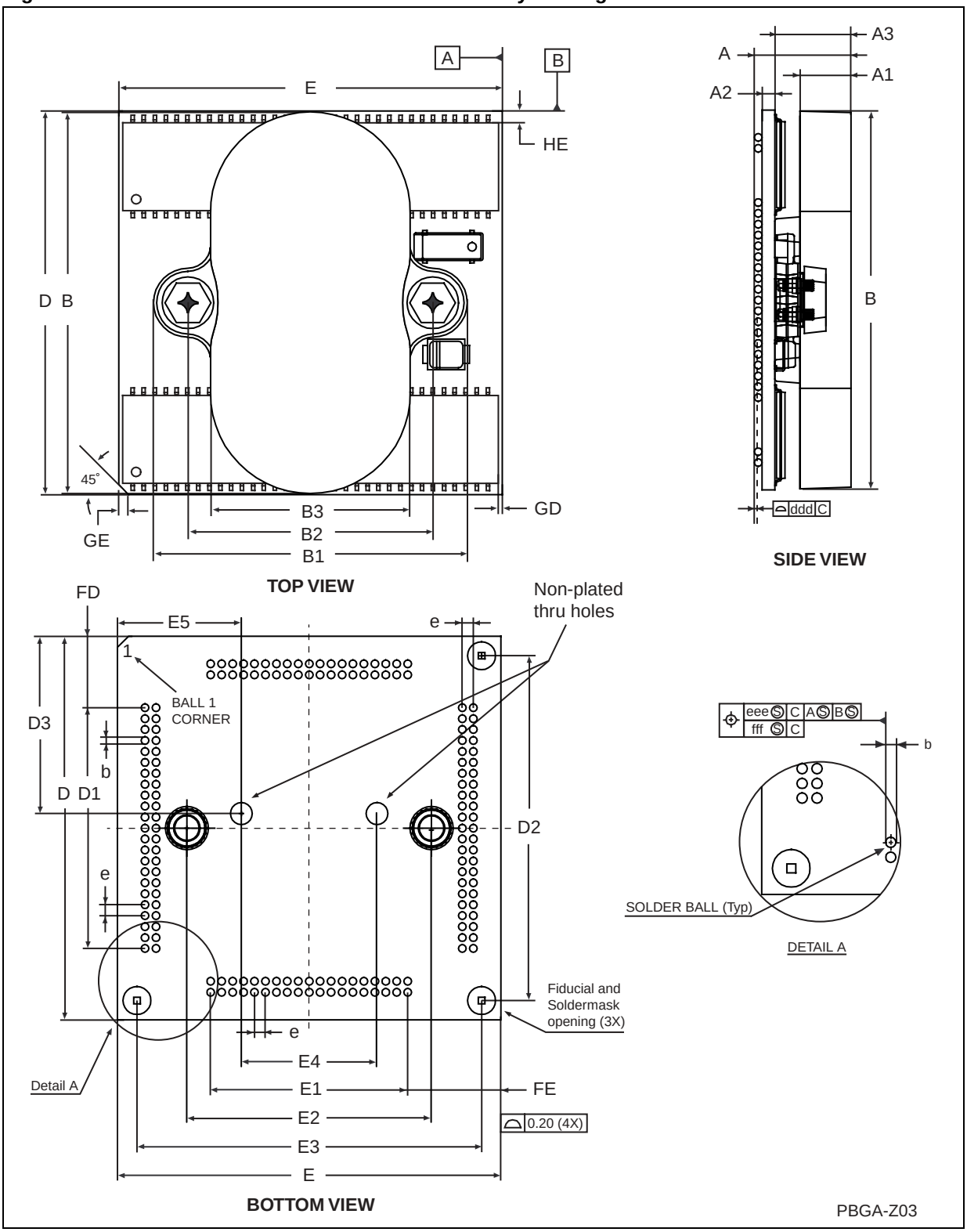
Table 13. Power Down/Up AC Characteristics

Symbol	Parameter[1]	Min	Max	Unit
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB}[3]	V_{PFD} (min) to V_{SS} V_{CC} Fall Time	10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	10		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	Power-up Deselect Time	40	200	ms

Note: 1. Valid for Ambient Operating Temperature: T_A = –15 to 75°C; V_{CC} = 4.5 to 5.5V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

PACKAGE MECHANICAL INFORMATION

Figure 16. PBGA-ZA – 168-ball Plastic Ball Grid Array Package Outline



Note: Drawing is not to scale.

Table 14. PBGA-ZA – 168-ball Plastic Ball Grid Array Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	11.64	11.24	12.04	0.458	0.443	0.474
A1	6.60	6.30	6.90	0.260	0.248	0.272
A2	1.50	1.40	1.60	0.059	0.055	0.063
A3	9.25	9.00	9.50	0.364	0.354	0.374
B	44.40	44.30	44.50	1.748	1.744	1.752
B1	36.60	36.50	36.70	1.441	1.437	1.445
B2	28.25	28.15	28.35	1.112	1.108	1.116
B3	23.10	23.00	23.20	0.909	0.906	0.913
b	0.76	0.71	0.81	0.030	0.028	0.032
D	44.50	44.30	44.70	1.752	1.744	1.760
D1	27.94			1.100		
D2	40.00	39.80	40.20	1.575	1.567	1.583
D3	20.56	20.46	20.66	0.809	0.806	0.813
e	1.27			0.050		
E	44.50	44.30	44.70	1.752	1.744	1.760
E1	22.86			0.900		
E2	28.40			1.118		
E3	40.00	39.80	40.20	1.575	1.567	1.583
E4	15.75	15.65	15.85	0.620	0.616	0.624
E5	14.38	14.28	14.48	0.566	0.562	0.570
FD	8.28	8.08	8.48	0.326	0.318	0.334
FE	10.82	10.72	10.92	0.426	0.422	0.430
GD	0.58	0.38	0.78	0.023	0.015	0.031
GE	1.00			0.039		
HE	1.42	1.22	1.62	0.056	0.048	0.064
n	168			168		
	Tolerance			Tolerance		
ddd	0.15			0.006		
eee	0.25			0.010		
fff	0.10			0.004		

PART NUMBERING

Table 15. Ordering Information Scheme

Example: M440T 513Y –15 ZA 9

Device Type

M440T

Supply Voltage and Write Protect Voltage

513Y = V_{CC} = 4.5 to 5.5V; V_{PFD} = 4.0 to 4.5V

Speed

–15 = 150ns

Package(1)

ZA = 168-ball Ball Grid Array

Temperature Range

9 = –15 to 75 °C

Note: 1. Where “Z” is the symbol for PBGA packages and “A” denotes 1.27mm ball pitch

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

REVISION HISTORY

Table 16. Document Revision History

Date	Rev. #	Revision Details
October 2002	1.0	First issue
16-Jan-03	1.1	Modify mechanical data (Table 14)
31-Mar-03	1.2	Update test condition (Table 12)
11-Apr-03	2.0	Updated with template v2.2
05-Oct-04	3.0	Reformatted; update mechanical dimensions (Figure 16; Table 14)