## Mescon SP5T PIN Diode Switch with Integrated Bias Network

## Features

■ Ultra Broad Bandwidth: 2 GHz to 18 GHz

- 1.8 dB Insertion Loss, 35 dB Isolation at 18 GHz
- Reliable. Fully Monolithic, Glass Encapsulated Construction


## Description

The MA4SW510B-1 is a SP5T Series-Shunt broad band switch with integrated bias networks made with M/A-COM's HMIC ${ }^{\text {TM }}$ (Heterolithic Microwave Integrated Circuit) process, US Patent $5,268,310$. This process allows the incorporation of silicon pedestals that form series and shunt diodes or vias by imbedding them in low loss glass. By using small spacing between elements, this combination of silicon and glass gives HMIC devices low loss and high isolation performance through 18 GHz .

## Applications

These high performance switches are suitable for the use in multiband ECM, Radar, and instrumentation control circuits where high isolation to insertion loss ratios are required. With a standard $+5 \mathrm{~V} /-5 \mathrm{~V}$, TTL controlled PIN diode driver, 80 ns switching speeds are achieved.

## Absolute Maximum Ratings ${ }^{1}$

@ TA = +25 ${ }^{\circ} \mathrm{C}$ (unless otherwise specified)

| Parameter | Value |
| :--- | :---: |
| Operating Temperature | $-65^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Storage Temperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| RF C.W. Incident Power <br> $(+/-20 \mathrm{~mA})$ | +30 dBm |
| DC Bias Current (Forward) | $+/-40 \mathrm{~mA}$ |
| Applied Voltage (Reverse) | 15 V |

1. Exceeding any of these values may result in permanent damage

MA4SW510B-1 Layout


## Nominal Chip Dimensions

| Chip Dimensions $(\mu \mathrm{m})$ |  |  |  |
| :---: | :---: | :---: | :---: |
|  | X | Y |  |
| Chip | 3120 | 3120 |  |
| Pad Dimensions $(\mu \mathrm{m})$ |  |  |  |
|  | X | Y |  |
| RF | 400 | 175 |  |
| DC | 125 | 125 |  |
| Pad Locations $(\mu \mathrm{m})$ |  |  |  |
|  |  |  |  |
| J1 | X | Y |  |
| J2 | 0 | 0 |  |
| B2 | -1385 | +500 |  |
| J3 | -1385 | +1200 |  |
| B3 | -1385 | +2000 |  |
| J4 | 0 | +2700 |  |
| B4 | +700 | +2770 |  |
| J5 | +1385 | +2770 |  |
| B5 | +1385 | +2000 |  |
| J6 | +1385 | +1300 |  |
| B6 | +900 | +500 |  |
| Pad Locations Relative to J1 |  |  |  |

## Electrical Specifications @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C},+/-10 \mathrm{~mA}$ Bias Current (On-Wafer Measurements)

| Parameters | Frequency | Minimum | Typical | Maximum | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Insertion Loss | 6 GHz | - | 0.9 | 1.0 | dB |
|  | 12 GHz | - | 1.2 | 1.5 | dB |
|  | 18 GHz | - | 1.8 | 2.1 | dB |
| Isolation | 6 GHz | 40 | 48 | - | dB |
|  | 12 GHz | 30 | 40 | - | dB |
|  | 18 GHz | 25 | 35 | - | dB |
| Input Return Loss | 6 GHz | - | 20 | - | dB |
|  | 12 GHz | - | 20 | - | dB |
|  | 18 GHz | - | 17 | - | dB |
| Output Return Loss | 6 GHz | - | 19 | - | dB |
|  | 12 GHz | - | 19 | - | dB |
|  | 18 GHz | - | 17 | - | dB |
| Switching Speed ${ }^{1}$ | 10 GHz | - | 80 | - | nS |

1. Typical switching speed is measured from $10 \%$ to $90 \%$ of the detected RF voltage driven by a TTL compatible driver. Driver output parallel RC network uses a capacitor between 390 pF-560 pF and a resistor between 150-220 Ohms to achieve 80 ns rise and fall times.

## Typical Driver Connections

| Control Level (DC Current) |  |  |  | Condition of RF Output |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| B2 | B3 | B4 | B5 | B6 | J2-J1 | J3-J1 | J4-J1 | J5-J1 | J6-J1 |
| $-\mathbf{1 0 ~ m A}$ | +10 mA | +10 mA | +10 mA | +10 mA | Low Loss | Isolation | Isolation | Isolation | Isolation |
| +10 mA | -10 mA | +10 mA | +10 mA | +10 mA | Isolation | Low Loss | Isolation | Isolation | Isolation |
| +10 mA | +10 mA | -10 mA | +10 mA | +10 mA | Isolation | Isolation | Low Loss | Isolation | Isolation |
| +10 mA | +10 mA | +10 mA | -10 mA | +10 mA | Isolation | Isolation | Isolation | Low Loss | Isolation |
| +10 mA | +10 mA | +10 mA | +10 mA | -10 mA | Isolation | Isolation | Isolation | Isolation | Low Loss |

Note: Typical Switching Speed measured from $10 \%$ to $90 \%$ of detected RF signal driven by a TTL compatible driver.

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## Assembly Considerations

The following precautions should be observed for successful assembly of the die.

## Cleanliness

These chips should be handled in a clean environment. Do not attempt to clean die after installation.

## Electro-Static Sensitivity

The MA4SW Series PIN switches are ESD, Class 1 sensitive. The proper ESD handling procedures should be used.

## Wire Bonding

Thermosonic wedge wire bonding using 0.003 " x 0.00025 " ribbon or $0.001 "$ diameter gold wire is recommended. A stage temperature of $150{ }^{\circ} \mathrm{C}$ and a force of 18 to 22 grams should be used. Ultrasonic energy should be adjusted to the minimum required. RF bonds should be as short as possible to minimize inductance.

## Mounting

These chips have Ti-Pt-Au back metal. They can be die mounted with a $80 \mathrm{Au} / 20 \mathrm{Sn}$ or $\mathrm{Sn} 62 / \mathrm{Pb} 36 / \mathrm{Ag} 2$ solder preform or electrically conductive Ag epoxy. Mounting surface must be clean of oils and contaminants and flat.

## Eutectic Die Attachment

An 80/20 gold-tin eutectic solder preform is recommended with a work surface temperature of $255{ }^{\circ} \mathrm{C}$ and a tool tip temperature of $265{ }^{\circ} \mathrm{C}$. When hot gas is applied, the tool tip temperature should be $290{ }^{\circ} \mathrm{C}$. The chip should not be exposed to temperatures greater than $320^{\circ} \mathrm{C}$ for more than 10 seconds. No more than three seconds should be required for the attachment.

## Epoxy Die Attachment

Assembly should be preheated to $125-150{ }^{\circ} \mathrm{C}$. A Controlled thickness of 2 mils is recommended for best electrical and thermal conductivity. A thin epoxy fillet should be visible around the perimeter of the chip after placement. Cure epoxy per manufacturer's recommended schedule.

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## Operation of the MA4SW510B-1 Switch

The Simultaneous Application of Negative DC Current to the Low Loss Port and Positive DC current to the Remaining Isolated Ports as shown in the schematic provides successful RF operation of the MA4SW Series of PIN Diode Switches. The Backside Area of the Die is the RF and DC Return Ground Plane. The DC Bias Return is located on Common Port J1. Constant Current Sources should supply the DC Control Currents.

In the Low Loss State, the Series Diode must be Forward Biased and the Shunt Diode Reverse Biased. For All the Isolated Ports, the Shunt Diode is Forward Biased while the Series Diode is Reverse Biased.

This Design Improves Insertion Loss, P1dB, IP3, and Switching Speed by Incorporating a Voltage Pull-up Resistor ( $\sim 100 \Omega$ ) in the DC Return Path, ( J1 ) under Insertion Loss Bias. A Typical Value of $|-3 \mathrm{~V}|$ is achieved at the Insertion Loss Bias Node using +/- 20 mA , with a Standard, +/- 5 V TTL Controlled PIN Diode Driver.

## Fig 1: MA4SW510B-1 Schematic



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