Features

- 750 pS Dynamic Range, 50 pS Step Size
- BGA Package
- Parallel Control Interface
- Positive Control Logic
- Cascadable
- No off chip components required

Description

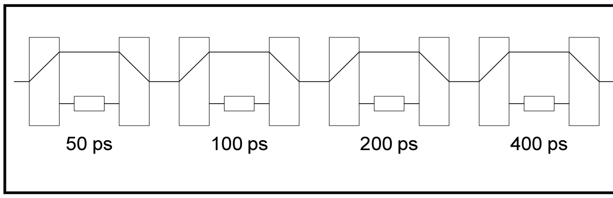
The M/A-COM MAMUSM0008 is a 0 to 750 pS variable delay line controlled by 4 complementary bit pairs. It provides the user with 50 pS delay step sizes for use in standard wireless applications. The MAMUSM0008 is particularly useful in providing time delay in the cancellation loops of feed-forward amplifiers.

Ordering Information[1]

Part Number	Package
MAMUSM0008	Bulk Packaging
MAMUSM0008TR	1000 piece reel
MAMUSM0008-TB	Units Mounted on Test Board

1. Reference Application Note M513 for reel size information.

Block Diagram

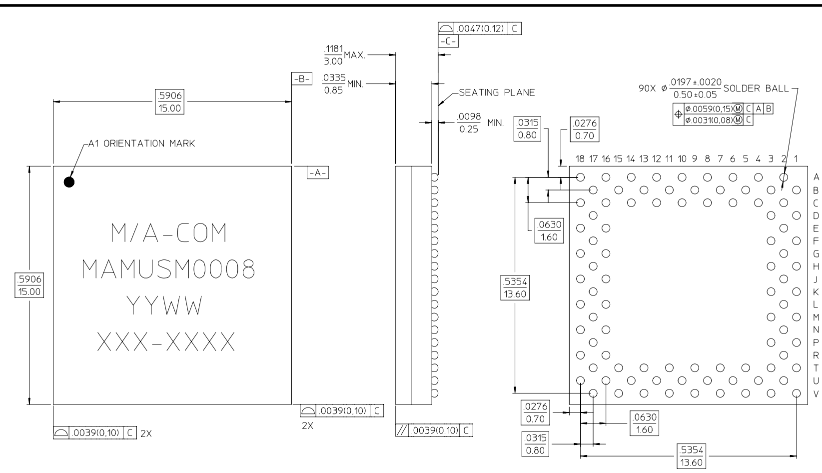


Absolute Maximum Ratings[2,3]

Parameter	Absolute Maximum
Control Voltage	8.5V
Maximum RF Input Power	+30 dBm
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

2. T_A = +25°C (unless otherwise specified)
3. Exceeding any one or combination of these limits may cause permanent damage to this device.

BGA Package



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Electrical Specifications: T_A = 25°C, Z_0 = 50 Ω

Parameter	Conditions	Units	Min.	Typ.	Max.
Frequency	1.8 - 2.4 GHz	—	—	—	—
Delay Line Control Range	—	pS	0	—	750
Delay Line Control Step Size	—	pS	—	50	—
Delay Step Accuracy	± 5 pS +5% of step size in pS	—	—	—	—
Output Return Loss	—	dB	15	20	—
Input Return Loss	—	dB	15	20	—
Input P1dB	—	dBm	— 7	27	—
Insertion Loss	—	dB	5	—	8
Output IP3	PIN = 0 dBm, 5 MHz Spacing	dBm	—	38	—
Control Voltage	—	V	2.7	3	8.5
Control Current	—	µA	2	20	—
Switching Speed (50% TTL to 90% RF)	3V Control	nS	—	72	100

Pin-Out Diagram

18	17	16	15	14	13	12	11	10	9	8	7	6	8	4	3	2	1	
GND		GND		GND		GND		GND		GND		GND		RF_OUT		GND		A
	GND		GND		GND		GND		GND		GND		GND		GND		GND	B
GND		CTL_C2		GND		CTL_D1		GND		CTL_D2		GND		GND		GND		C
	CTL_C1														GND		GND	D
GND		GND														GND		E
	GND														GND		GND	F
GND		GND														GND		G
	GND														GND		GND	H
GND		GND														GND		J
	GND														GND		GND	K
GND		GND														GND		L
	GND														GND		GND	M
GND		GND														GND		N
	GND														GND		GND	P
GND		CTL_B2														GND		R
	GND		CTL_B1		GND		CTL_A2		CTL_A1		GND		GND		GND		GND	T
GND		GND		GND		GND		GND		GND		GND		GND		GND		U
	GND		GND		GND		GND		GND		GND		GND		RF_IN		GND	V

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Control

Herein is described the control method for the MAMUSM0008 Digital Delay Line. The information will be aimed specifically at the use of the delay line mounted on a M/A-COM test sample board. The same theory and control scheme can be applied directly to the component by itself.

This product allows the insertion of a variable electrical delay between its two ports. The control consists of four complimentary bit pairs (8 bits total). Each pair is given a different letter, as shown in the table to the right:.

Delay Line	Associated Letter
50 ps	A
100 ps	B
200 ps	C
400 ps	D

Note that each delay line has a pair named as follows:
CTL_A1 and CTL_A2, CTL_B1 and CTL_B2,
CTL_C1 and CTL_C2, CTL_D1 and CTL_D2.

D2 D1 C2 C1 B2 B1 A2 A1	hex	decimal	state	ps delay
10101010	AA	170	0	0
10101001	A9	169	1	50
10100110	A6	166	2	100
10100101	A5	165	3	150
10011010	9A	154	4	200
10011001	99	153	5	250
10010110	96	150	6	300
10010101	95	149	7	350
01101010	6A	106	8	40
01101001	69	105	9	450
01100110	66	102	10	500
01100101	65	101	11	550
01011010	5A	90	12	600
01011001	59	89	13	650
01010110	56	86	14	700
01010101	55	85	15	750

The above table illustrates the method of controlling the bits for the desired delay in pico seconds. The hex and decimal representations are included for programming purposes. “1” denotes 5 volts and “0” denotes 0 volts. A given delay line is set when bits 2 and bit 1 are set to 0 and 1 respectively. The given delay line is bypassed when the bits 2 and 1 are set to 1 and 0 respectively.

The “GND” pin on the test board header must be connected to the DC supply ground.

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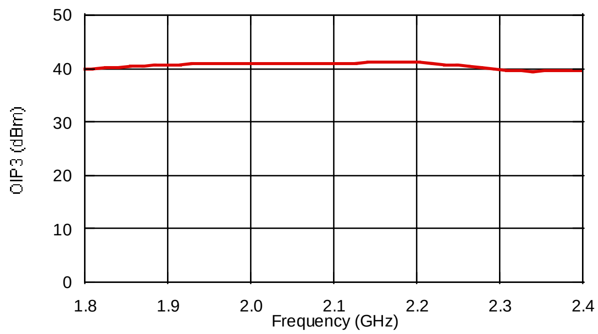
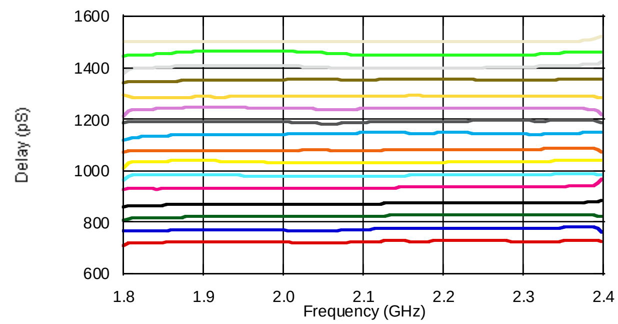
Typical Performance Curves

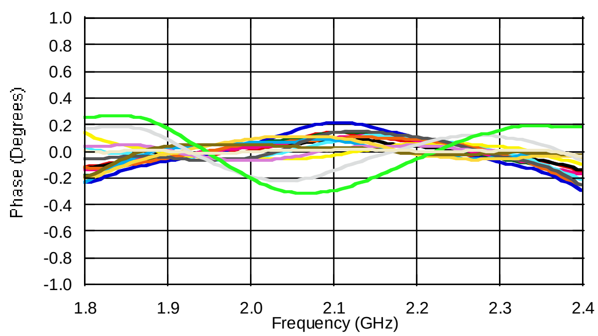
OIP3 vs. Frequency



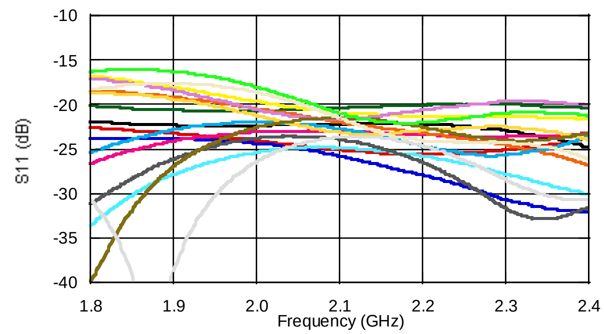
Delay vs. Frequency



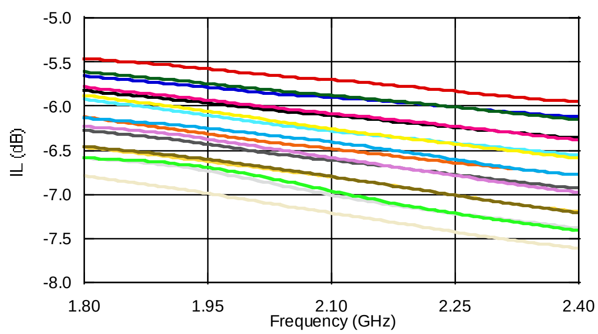
Phase vs. Frequency



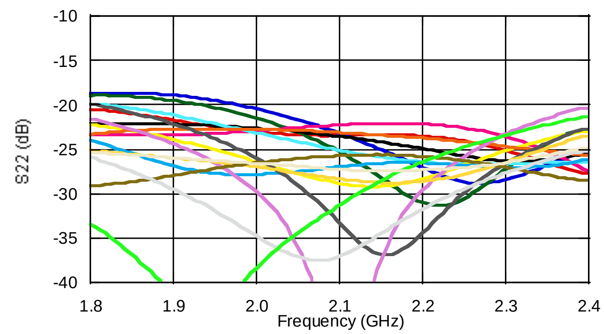
Input Return Loss vs. Frequency



Insertion Loss vs. Frequency



Output Return Loss vs. Frequency



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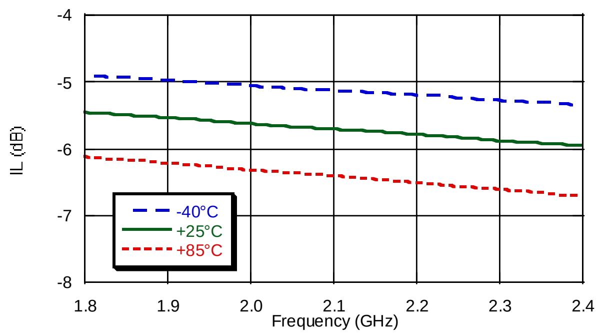
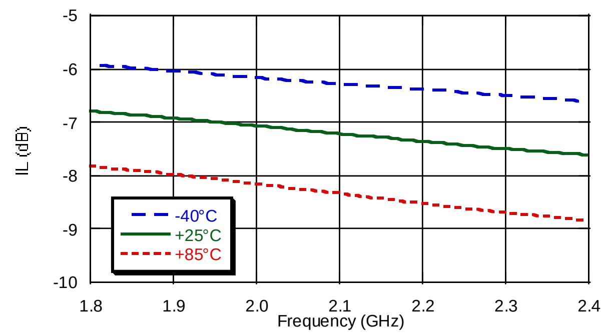
Typical Performance Curves

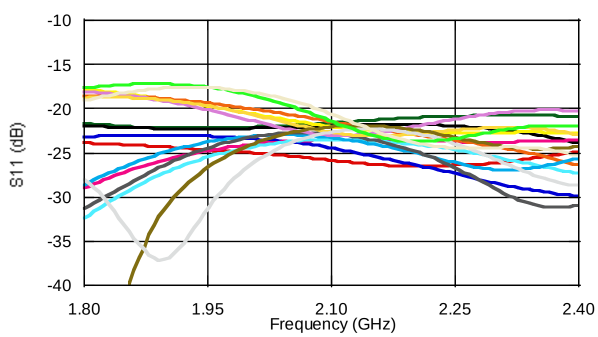
Insertion Loss vs. Frequency over Temperature at 0 pS State



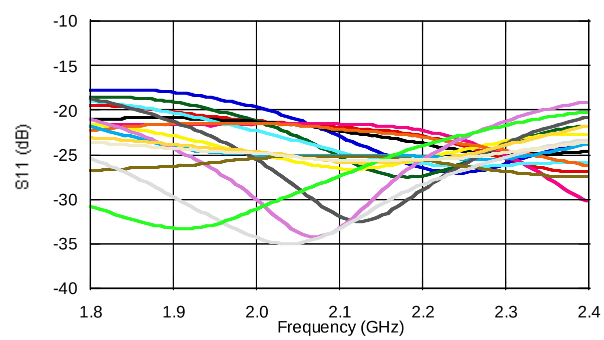
Insertion Loss vs. Frequency over Temperature at 750 pS State



Input Return Loss vs. Frequency (+85°C)



Output Return Loss vs. Frequency (+85°C)



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Measurement

The simplest way to measure the delay steps is with a vector network analyzer (VNA). For taking S-Parameter data, perform a standard calibration and measure the parameters for the given state.

Below is a description of how to see the delay accurately. M/A-COM recommends the following measurement procedure:

Set the delay line to the reference or insertion delay state. With the two ports of the VNA connected to the “in” and “out” on the test board, measuring S21, set display→ memory, and display data/memory. This will normalize your data to the reference insertion state.

Next, switch the measurement format to phase. This should be flat and zero due to the normalization. Switch in the first delay line. (50ps). The display will not remain on zero, but will have an offset. Under the Scale/Reference menu, select electrical delay, and dial that up until the data reads zero again, across the band of interest. That electrical delay will be 50ps.

Continue to switch in the delay lines, dialing in more delay each time.

Other methods are possible, but this is the most straightforward approach. We do not recommend using the ‘delay’ format in the VNA. The VNA’s method of measuring this results in a noisy response, and is less accurate than the method outlined above.

Upon request, M/A-COM can provide a test control board to ease stepping through the states.

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