## Features

## - 6 Bit Phase Shifter

- $360^{\circ}$ Coverage, LSB $=5.6^{\circ}$
- TTL Control Inputs
- MSAG ${ }^{\text {™ }}$ Process


## Description

The MAPCGM0002-Die is a 6-bit Phase Shifter with Parallel TTL Input Control. This product is fully matched to 50 ohms on both the input and output. The
 part has $360^{\circ}$ of phase coverage with LSB of $5.6^{\circ}$.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate MESFET Process, each device is $100 \%$ RF tested on wafer to ensure performance compliance.

## Primary Applications

- Satellite Communication
- Phased Array Radar

M/A-COM's MSAG ${ }^{\text {TM }}$ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Electrical Characteristics: $\mathrm{T}_{\mathrm{B}}=40^{\circ} \mathrm{C}^{1}, \mathrm{Z}_{0}=50 \Omega, \mathrm{~V}_{\mathrm{EE}}=-5 \mathrm{~V}$

| Parameter | Symbol | Typical | Units |
| :---: | :---: | :---: | :---: |
| Bandwidth | f | $3.5-6.0$ | GHz |
| Insertion Loss, Reference State | IL | 6 | dB |
| Input VSWR, All States | VSWR | $1.5: 1$ |  |
| Output VSWR, All States | VSWR | $1.7: 1$ | $\circ$ |
| RMS Phase Error | $\phi_{\text {RMS }}$ | 8 | $\circ$ |
| RMS Phase Error, Calibrated | $\phi_{\text {RMS }}$ | 3 | dB |
| Peak to Peak Gain Variation, All States | $\Delta \mathrm{G}$ | mA |  |
| Current | $\mathrm{I}_{\text {EE }}$ | c | dBO |
| Input Third Order Intercept | P1dB | 26 | dBm |
| Input 1-dB Compression Point |  | 2 |  |

## 1. $\mathrm{T}_{\mathrm{B}}=$ MMIC Base Temperature

- Asia/Pacific Tel: 81.44.844.8296/Fax: 81.44.844.8298

Visit www.macom.com for additional data sheets and product information.

## Maximum Operating Conditions ${ }^{1}$

| Parameter | Symbol | Absolute Maximum | Units |
| :---: | :---: | :---: | :---: |
| Input Power | $\mathrm{P}_{\mathrm{IN}}$ | 31 | dBm |
| Source Supply Voltage | $\mathrm{V}_{\mathrm{EE}}$ | -6.0 | V |
| Junction Temperature | $\mathrm{T}_{J}$ | 180 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {STG }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. Operation outside of these ranges may reduce product reliability. Operation at other than the typical values may result in performance outside the guaranteed limits.

## Recommended Operating Conditions

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Source Voltage | $\mathrm{V}_{\mathrm{EE}}$ | -5.2 | -5 | -4.8 | V |
| Control Voltage | $\mathrm{V}_{\text {control pads }}$ |  |  |  |  |
| Logic High |  | 3 | 5 | 5 | V |
| Logic Low | 0 | 0 | 0.4 | V |  |

## Operating Instructions

This device is static and light sensitive. Digital circuit operation can be impaired under high intensity light, e.g. microscope light. Please handle with care. To operate the device, follow these steps.

1. Power Up: Apply $\mathrm{V}_{\mathrm{EE}}=-5 \mathrm{~V}$.
2. Apply Logic Voltages to control Circuits as listed in Recommended Operating Conditions
3. Power Down: Set $\mathrm{V}_{\mathrm{EE}}=0$



Figure 1. Reference State Insertion Loss, Input and Output VSWR vs. Frequency


Figure 2. Phase Shifter Figures of Merit: Average Error vs Reference State, RMS Error and Calibrated RMS Error over All States

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- Europe Tel: 44.1908.574.200 / Fax: 44.1908.574.300
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Figure 3. Relative Phase vs. Phase Shifter State


Figure 4. Relative Gain Change vs. Phase Shifter State


Figure 5. Input VSWR vs. Phase Shifter State


Figure 6. Output VSWR vs. Phase Shifter State

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## Mechanical Information

Chip Size: $3.816 \times 1.354 \times 0.075 \mathrm{~mm} \quad(150 \times 53 \times 3$ mils)


Figure 7. Die Layout

## Bond Pad Dimensions

| Pad | Size $(\mu \mathrm{m})$ | Size (mils) |
| :---: | :---: | :---: |
| RF In and Out | $100 \times 200$ | $4 \times 8$ |
| DC Supply Voltage VEE | $125 \times 125$ | $5 \times 5$ |
| DC Control Voltage VC | $125 \times 125$ | $5 \times 5$ |



Figure 8. Recommended bonding diagram for pedestal mount.
Support circuitry typical of MMIC characterization.

## Assembly Instructions:

Die attach: Low thermal conductivity silver epoxies are acceptable for die attach of this MMIC. Follow the manufacturer's instructions. If solder is employed, use AuSn (80/20) 1-2 mil preform solder. Limit time @ $300^{\circ} \mathrm{C}$ to less than 5 minutes.

Wirebonding: Bond @ $160^{\circ} \mathrm{C}$ using standard ball or thermal compression wedge bond techniques. For DC and RF pad connections, use either ball or wedge bonds. For best performance, especially above 10 GHz , wedge bonds of shortest length employed on the RF interconnects is preferred over ball bonds.

