19-1700; Rev 1; 6/05

EVALUATION KIT AVAILABLE

Upstream CATV Amplifier

General Description

The MAX3509 is a programmable power amplifier for use in CATV upstream applications. The device outputs up to 66dBmV QPSK through a 1:1 transformer. It features variable gain controlled by a 3-wire digital serial bus. Gain control is available in 1dB steps. The device operates over a 5MHz to 65MHz frequency range.

The MAX3509 offers a transmit-disable mode, which places the device in a high-isolation state for use between bursts in TDMA systems. In this mode, all analog functions are shut down, minimizing output noise and power consumption. When entering and leaving transmit-disable mode, transients are kept to 25mV nominal at full gain. In addition, supply current is reduced to 7.8mA.

An additional power-down mode is available. Shutdown mode disables all circuitry and reduces current consumption to less than 1µA.

The MAX3509 is available in a 20-pin TSSOP-EP package for the extended-industrial temperature range (-40°C to +85°C).

Applications

Telephony-Over-Cable
OPENCATV Set-Top Boxes
Cable Modems
CATV Status Monitors
CATV Infrastructures

Features

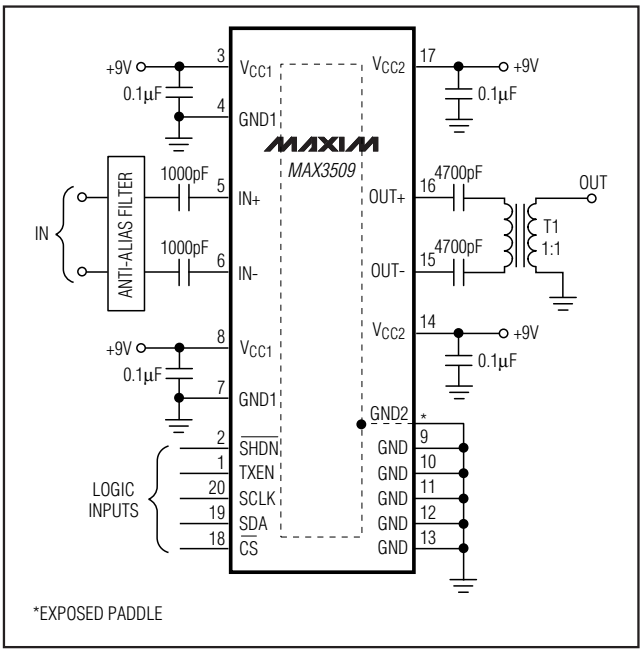
- **Ultra-Low Power-Up/Down Transients, 25mV (typ) at 66dBmV Output**
- **Single-Supply Operation**
- **Output Level Ranges from <12dBmV to 67dBmV (QPSK)**
- **Gain Programmable in 1dB Steps**
- **Low Transmit Output Noise Floor: -41dBmV (160kHz BW)**
- **Low Transmit-Disable Output Noise: -70dBmV**
- **Shutdown Mode**

Ordering Information

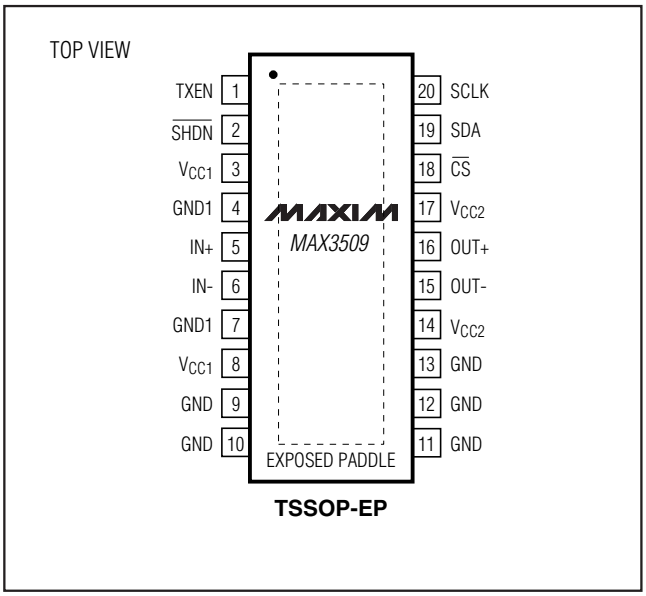
PART	TEMP RANGE	PIN-PACKAGE
MAX3509EUP	-40°C to +85°C	20 TSSOP-EP*
MAX3509EUP+	-40°C to +85°C	20 TSSOP-EP*

*EP = Exposed paddle.
+Denotes lead-free package.

Typical Operating Circuit



Pin Configuration



TSSOP-EP

†Covered by U.S. Patent numbers 5,748,027 and 5,994,955.

ABSOLUTE MAXIMUM RATINGS

V_{CC1}, V_{CC2} to GND, GND1 .....-0.3V to +10.0V
SCLK, SDA, $\overline{CS}$, TXEN, $\overline{SHDN}$ to GND and GND1 .....-0.3V to +5.5V
Continuous Input Voltage (IN+, IN-).....$2V_{P-P}$
Continuous Current (OUT+, OUT-) 80mA

Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP-EP (derate at 27mW/°C above +70°C).....2200mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC1} = V_{CC2} = 8.5V to 9.5V, TXEN = $\overline{SHDN}$ = high, D7 = 1, T_A = -40°C to +85°C, unless otherwise noted. No input signal applied. Typical parameters are at T_A = +25°C.) (Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		8.5		9.5	V
Supply Current Transmit Mode	I_{CC}			84	115	mA
Supply Current Transmit-Disable Mode	I_{CC}	TXEN = low or D7 = 0		7.8	10	mA
Supply Current Shutdown Mode	I_{CC}	$\overline{SHDN}$ = low, TXEN = low		10		µA
Input High Voltage	V_{INH}		2.0			V
Input Low Voltage	V_{INL}				0.8	V
Input High Current	I_{BIASH}				100	µA
Input Low Current	I_{BIASL}		-100			µA

AC ELECTRICAL CHARACTERISTICS

(MAX3509 EV kit, V_{CC1} = V_{CC2} = 8.5V to 9.5V, TXEN = $\overline{SHDN}$ = high, D7 = 1, V_{INPUT} = 34dBmV differential, output impedance = 75Ω through a 1:1 transformer, T_A = -40°C to +85°C, unless otherwise noted. Typical parameters are at T_A = +25°C.) (Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Gain	A_V	T_A = +25°C, f_{INPUT} = 42MHz, gain-control word = 63	33			dB
		T_A = +25°C, f_{INPUT} = 42MHz, gain-control word = 0			-22	
		T_A = +25°C, f_{INPUT} = 42MHz, gain-control word = 50	22.8	24.2	26.7	
		f_{INPUT} = 42MHz, gain-control word = 63			31	
		f_{INPUT} = 42MHz, gain-control word = 0	-21			
		f_{INPUT} = 42MHz, gain-control word = 50	21.3	24.2	26.7	
Gain Fariness (note 1)		V_{OUTPUT} = 60dBmV, f_{INPUT} = 5MHz to 42MHz		0.1	0.4	dB
		V_{OUTPUT} = 60dBmV, f_{INPUT} = 5MHz to 65MHz		0.3	0.9	
Gain Step Size		f_{INPUT} = 5MHz to 65MHz, A_V = -20dB to +33dB	0.7	1	1.3	dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX3509 EV kit, V_{CC1} = V_{CC2} = 8.5V to 9.5V, TXEN = $\overline{SHDN}$ = high, D7 = 1, V_{INPUT} = 34dBmV differential, output impedance = 75Ω through a 1:1 transformer, T_A = -40°C to +85°C, unless otherwise noted. Typical parameters are at T_A = +25°C.) (Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Transmit Mode Noise (Note 1)		BW = 160kHz, A_V = 32dB				-85	dBc
		BW = 160kHz, A_V = -20dB, T_A = +25°C			-41	-39.5	dBmV
		BW = 160kHz, A_V = -20dB, T_A = +85°C				-38.5	
Transmit-Disable Mode Noise Floor		TXEN = low, BW = 160kHz, A_V = +32dB, f_{INPUT} = 5MHz to 65MHz (Note 1)				-70	dBmV
TXEN Enable Transient Duration		TXEN rise time <0.1µs, T_A = +25°C (Note 1)			1.4	2	µs
TXEN Disable Transient Duration		TXEN fall time <0.1µs, T_A = +25°C (Note 1)			1	1.5	µs
TXEN Transient Step Size (Note 1)		A_V = 32dB, T_A = +25°C			25	100	mV_{P-P}
		A_V = 2dB or lower, T_A = +25°C			1.5	9	
Input Impedance	$\lvert Z_{INPUT} \rvert$	f_{INPUT} = 5MHz to 65MHz, single-ended, T_A = +25°C (Note 1)			1.2		kΩ
Output Impedance in Transmit Mode	$\lvert Z_{OUTPUT} \rvert$	f_{INPUT} = 5MHz to 65MHz, T_A = +25°C (Note 1)			1.2		Ω
Output Impedance in Transmit-Disable Mode	$\lvert Z_{OUTPUT} \rvert$	TXEN = low, f_{INPUT} = 5MHz to 65MHz, T_A = +25°C (Note 1)			170		Ω
Two-Tone Third-Order Distortion	IM3	Input tones at 65MHz and 65.2MHz, V_{INPUT} = 31dBmV/tone, A_V = 32dB (Note 1)			-53		dBc
2nd Harmonic Distortion	HD2	f_{INPUT} = 33MHz	V_{OUTPUT} = +60dBmV		-56	-53	dBc
			V_{OUTPUT} = +66dBmV		-56	-50	
		f_{INPUT} = 65MHz (Note 1)	V_{OUTPUT} = 66dBmV		-56	-50	
3rd Harmonic Distortion	HD3	f_{INPUT} = 22MHz	V_{OUTPUT} = +60dBmV		-56	-53	dBc
			V_{OUTPUT} = +66dBmV		-53	-48.5	
		f_{INPUT} = 65MHz (Note 1)	V_{OUTPUT} = 66dBmV		-43	-40	
Output 1dB Compression Point	P1dB	A_V = 32dB, 65MHz (Note 1)			26		dBm
AM to AM	AM/AM	A_V = 32dB, V_{INPUT} swept from 34dBmV to 38dBmV (Note 1)			0.1		dB
AM to PM	AM/PM	A_V = 32dB, V_{INPUT} swept from 34dBmV to 38dBmV (Note 1)			1.7		degrees

TIMING CHARACTERISTICS

(V_{CC1} = V_{CC2} = 8.5V to 9.5V, TXEN = $\overline{SHDN}$ = high, D7 = 1, T_A = +25°C, unless otherwise noted.) (Note 1.)

PARAMETER	SYMBOL	COMMENT	MIN	TYP	MAX	UNITS
$\overline{CS}$ to SCK Rise Setup Time	t_{SENS}		10			ns
$\overline{CS}$ to SCK Rise Hold Time	t_{SENH}		20			ns
SDA to SCK Setup Time	t_{SDAS}		10			ns
SDA to SCK Hold Time	t_{SDAH}		20			ns
SDA Pulse-Width High	t_{DATAH}		50			ns
SDA Pulse-Width Low	t_{DATAL}		50			ns
SCK Pulse-Width High	t_{SCKH}		50			ns
SCK Pulse-Width Low	t_{SCKL}		50			ns

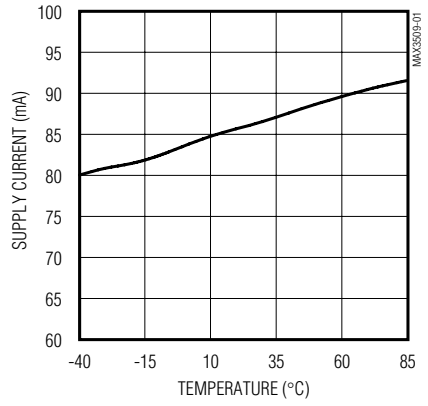
Note 1: Guaranteed by design and characterization.

Note 2: Tested parameters specified from -40°C to +85°C are guaranteed by design and characterization to ±3 sigma for temperatures less than 25°C.

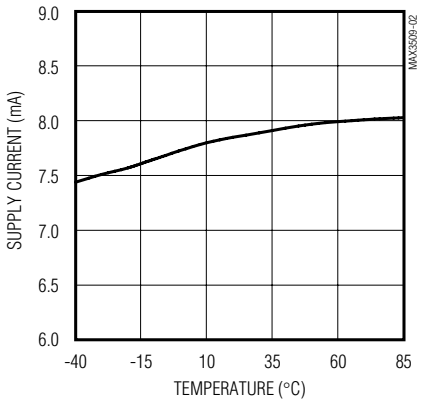
Typical Operating Characteristics

(MAX3509 EV kit, V_{CC1} = V_{CC2} = +9V, V_{IN} = +34dBmV, TXEN = $\overline{SHDN}$ = high, D7 = 1, f_{INPUT} = 10MHz, Z_{LOAD} = 75Ω through a 1:1 transformer, T_A = +25°C, unless otherwise noted.)

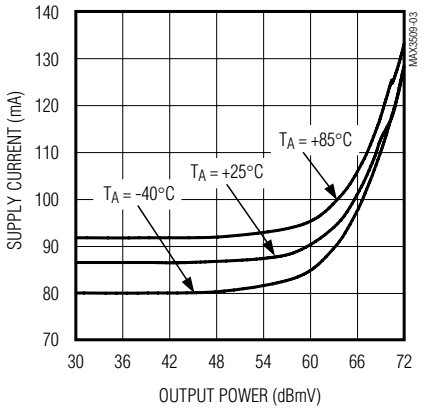
SUPPLY CURRENT vs. TEMPERATURE TRANSMIT ENABLE



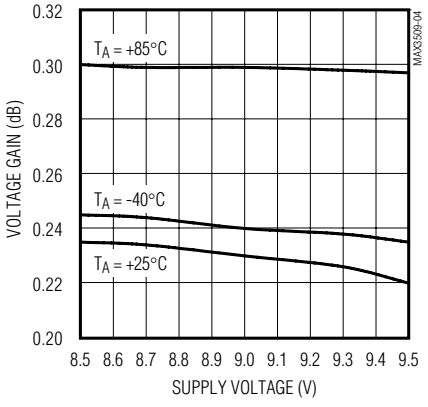
SUPPLY CURRENT vs. TEMPERATURE TRANSMIT DISABLE



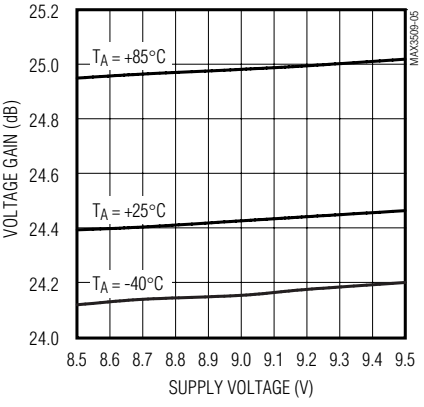
SUPPLY CURRENT vs. OUTPUT POWER



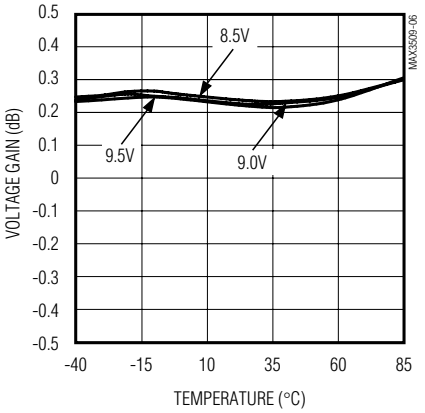
VOLTAGE GAIN vs. SUPPLY VOLTAGE (CONTROL WORD = 25)



VOLTAGE GAIN vs. SUPPLY VOLTAGE (CONTROL WORD = 50)



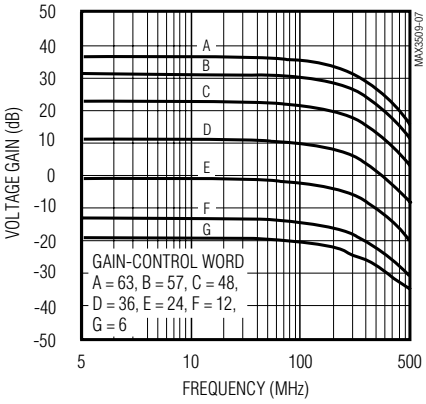
VOLTAGE GAIN vs. TEMPERATURE (CONTROL WORD = 25)



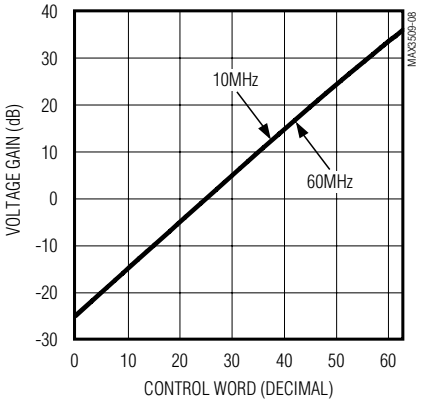
Typical Operating Characteristics (continued)

(MAX3509 EV kit, V_{CC1} = V_{CC2} = +9V, V_{IN} = +34dBmV, TXEN = $\overline{SHDN}$ = high, D7 = 1, f_{INPUT} = 10MHz, Z_{LOAD} = 75Ω through a 1:1 transformer, T_A = +25°C, unless otherwise noted.)

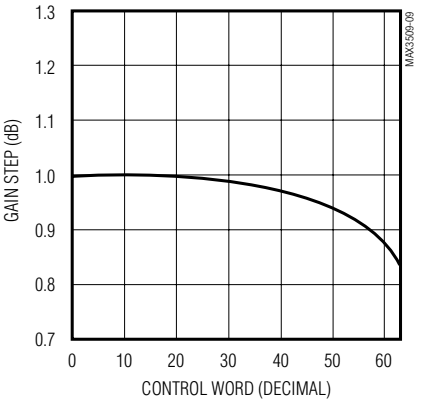
VOLTAGE GAIN vs. FREQUENCY



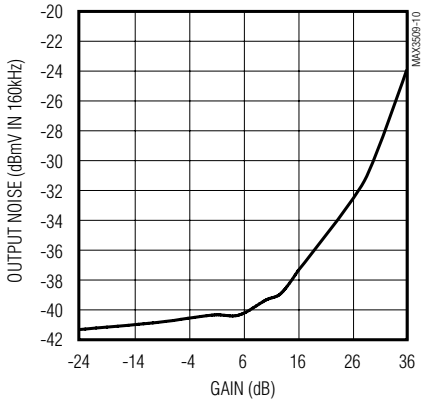
VOLTAGE GAIN vs. CONTROL WORD



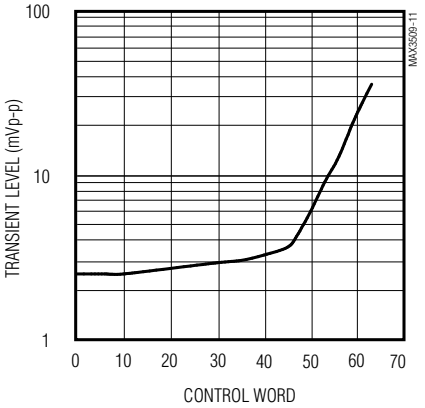
GAIN STEP vs. CONTROL WORD



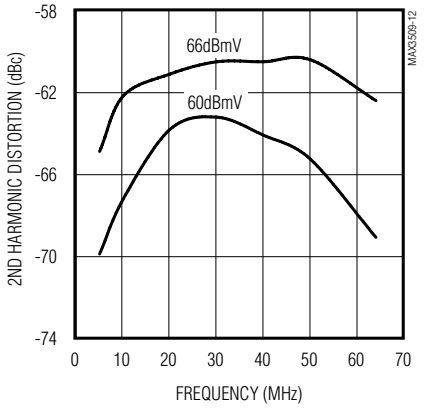
TRANSMIT OUTPUT NOISE vs. GAIN



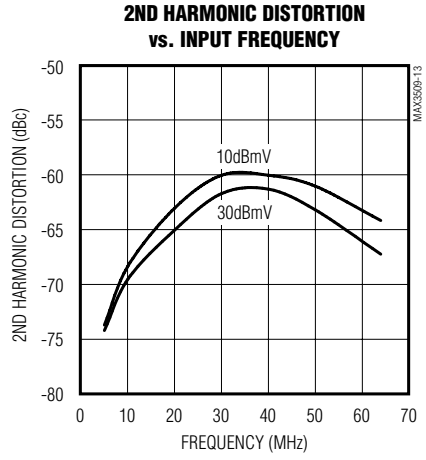
POWER-UP/DOWN TRANSIENTS vs. CONTROL WORD



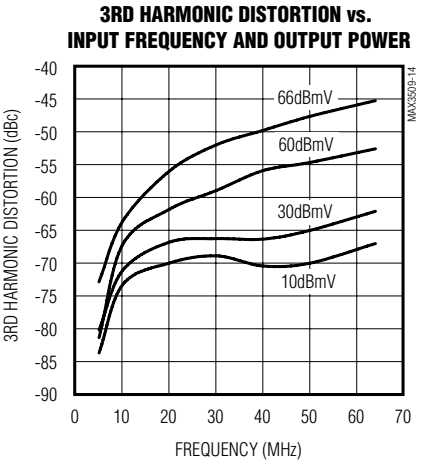
2ND HARMONIC DISTORTION vs. INPUT FREQUENCY



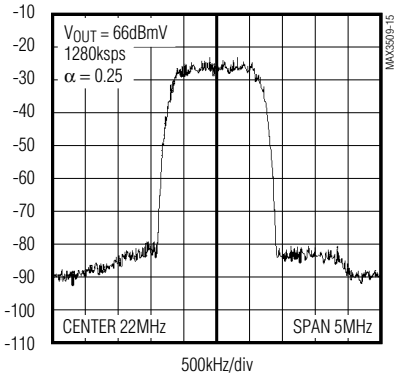
2ND HARMONIC DISTORTION vs. INPUT FREQUENCY



3RD HARMONIC DISTORTION vs. INPUT FREQUENCY AND OUTPUT POWER



QPSK OUTPUT SPECTRUM

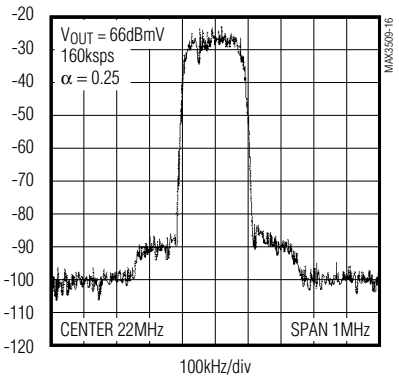


Upstream CATV Amplifier

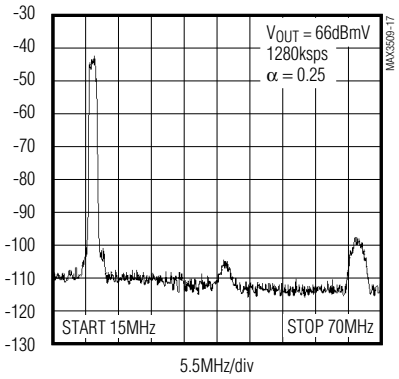
Typical Operating Characteristics (continued)

(MAX3509 EV kit, V_{CC1} = V_{CC2} = +9V, V_{IN} = +34dBmV, TXEN = $\overline{SHDN}$ = high, D7 = 1, f_{INPUT} = 10MHz, Z_{LOAD} = 75Ω through a 1:1 transformer, T_A = +25°C, unless otherwise noted.)

QPSK OUTPUT SPECTRUM



OUTPUT SPECTRUM



Pin Description

PIN	NAME	FUNCTION
1	TXEN	Transmit Enable. To disable the MAX3509 and provide high input/output isolation, drive TXEN low. Drive TXEN high for normal operation.
2	$\overline{SHDN}$	Shutdown. To enable low-power shutdown, drive $\overline{SHDN}$ low. Drive $\overline{SHDN}$ high for normal operation.
3, 8	V_{CC1}	Programmable-Gain Amplifier (PGA) +9V Supply. Bypass to GND1 with a 0.1µF decoupling capacitor as close to the part as possible.
4, 7	GND1	PGA Ground. Connect to ground with a low inductance path.
5	IN+	Noninverting PGA Input. Along with IN-, this port forms a high-impedance differential input to the PGA. Driving this port differentially increases the rejection of second-order distortion at low output levels.
6	IN-	Inverted PGA Input. When not used, AC-coupled to ground. See IN+.
9–13	GND	Ground
14,17	V_{CC2}	Power Amplifier Bias +9V Supply. Bypass to GND2 (exposed paddle) with a 0.1µF decoupling capacitor as close to the part as possible.
15	OUT-	Inverted Output. AC-couple to output transformer. Used in conjunction with OUT+.
16	OUT+	Noninverted Output. See *OUT-*.
18	$\overline{CS}$	Serial-Interface Enable. TTL-compatible input. See the *Serial Interface* section.
19	SDA	Serial-Interface Data. TTL-compatible input. See the *Serial Interface* section.
20	SCLK	Serial-Interface Clock. TTL-compatible input. See the *Serial Interface* section.
Exposed Paddle	GND2	Power Amplifier Bias Ground. Connect to ground with a low inductance path. Ensure a low thermal resistive path to PC board. See *Layout Issues*.

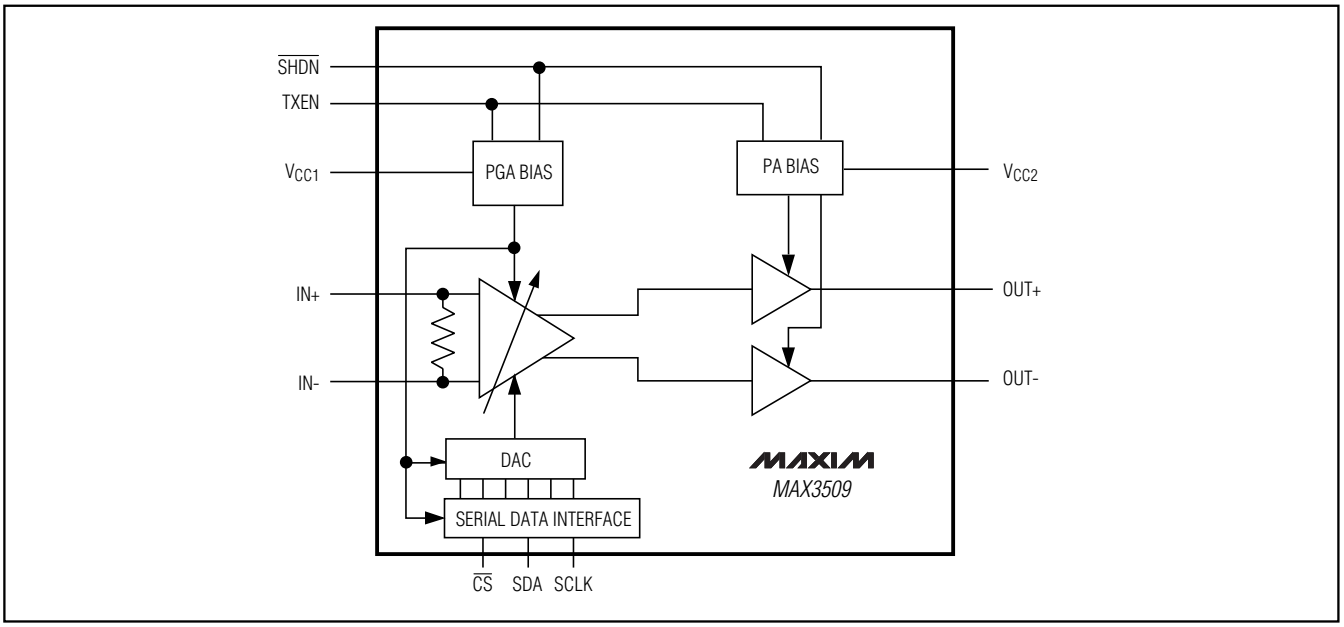


Figure 1. MAX3509 Functional Diagram

Detailed Description

The following sections describe the blocks shown in the functional diagram (Figure 1).

Programmable-Gain Amplifier

The PGA consists of the variable-gain amplifier (VGA) and the digital-to-analog converter (DAC), which provide better than 55dB of output level control in 1dB steps.

The PGA is implemented as a programmable Gilbert-cell attenuator. It uses a differential architecture to achieve maximum linearity. The gain of the PGA is determined by a 6-bit word (D5–D0) programmed through the serial data interface (Tables 1 and 2).

Specified performance is achieved when the input is driven differentially. The device may be driven single ended; however, a slight increase in even-order distortion may result at low output levels. To drive the device in this manner, one of the input pins must be capacitively coupled to ground. Use a capacitor value large enough to allow for a low-impedance path to ground at the lowest frequency of operation.

Power Amplifier

The power amplifier has two current-feedback amplifiers in an instrumentation amplifier configuration. This architecture provides superior even-order distortion performance but requires an external transformer to convert to a single-ended output. In transmit-disable mode, bias to the power amplifier is reduced to a minimal level, which provides high input to output isolation and low output noise.

Serial Interface

The serial interface has an active-low enable ($\overline{CS}$) to bracket the data, with data clocked in MSB first on the rising edge of SCLK. Data is stored in the storage latch on the rising edge of $\overline{CS}$. The serial interface controls the state of the PGA. Tables 1 and 2 show the register format. Serial-interface timing is shown in Figure 2.

PGA Bias Cell

The bias cell in the MAX3509 is controlled by the logic levels present at TXEN and $\overline{SHDN}$, as well as the program state of D7, the MSB of the 8-bit program word. Transmit-disable mode is actuated when the TXEN pin is driven to a logic low or when D7 = 0. In this mode, current to the PGA and power amps is reduced significantly while maintaining normal current flow to the serial data interface and DAC. This preserves the program stored in the serial data interface.

A logic low at the $\overline{SHDN}$ pin overrides the state of the TXEN pin or D7. In shutdown mode, the current to the PGA, power amp, serial data interface, and DAC is cut off, allowing only leakage currents to flow. The stored gain control program is lost in this mode.

Upstream CATV Amplifier

Power Amp Bias Cell

The power amp bias cell is used to enable and disable bias to the output power amplifier. This is controlled by TXEN and $\overline{SHDN}$.

Functional Modes

The MAX3509 has three functional modes controlled through the serial interface or external pins (Table 2): transmit mode, transmit-disable mode, and shutdown.

Transmit Mode

Transmit mode is the normal active mode of the MAX3509. Drive TXEN and $\overline{SHDN}$ high, and set D7 = 1 to activate transmit mode.

Transmit-Disable Mode

When in transmit-disable mode, all analog circuitry is shut down. This mode is activated by driving TXEN low or setting D7 = 1 while keeping $\overline{SHDN}$ high. This mode is typically used between bursts in TDMA systems. Transients are controlled by the transformer balance.

Shutdown Mode

In normal operation, the shutdown pin ($\overline{SHDN}$) is held high. When $\overline{SHDN}$ is driven low, all circuits within the IC are disabled. Only leakage currents flow in this mode. Data stored within the serial-data interface latches will be lost upon entering this mode. Current draw is reduced to 1µA (typ) in shutdown mode.

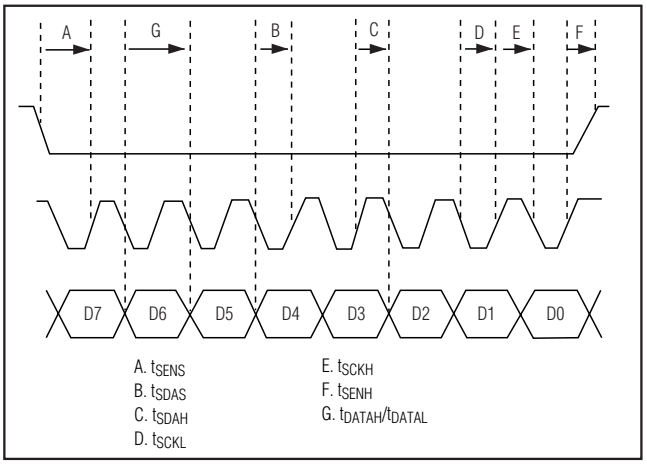


Figure 2. Serial-Interface Timing Diagram

Table 1. Serial-Interface Control Word

BIT	MNEMONIC	DESCRIPTION
MSB 7	D7	Transmit Disable
6	D6	Not used
5	D5	Gain Control, Bit 5
4	D4	Gain Control, Bit 4
3	D3	Gain Control, Bit 3
2	D2	Gain Control, Bit 2
1	D1	Gain Control, Bit 1
LSB 0	D0	Gain Control, Bit 0

Table 2. Truth Table

$\overline{SHDN}$	TXEN	D7	D6	D5	D4	D3	D2	D1	D0	GAIN CONTROL WORD	STATE
0	X	X	X	X	X	X	X	X	X	X	Shutdown Mode
1	0	X	X	X	X	X	X	X	X	X	Transmit-Disable Mode
1	X	0	X	X	X	X	X	X	X	X	Transmit-Disable Mode
1	1	1	X	X	X	X	X	X	X	X	Transmit Mode
1	1	1	X	0	0	0	0	0	0	0	Gain = -25dB*
1	1	1	X	0	0	0	0	0	1	1	Gain = -24dB*
1	1	1	X	—	—	—	—	—	—	—	—
1	1	1	X	0	1	1	0	0	1	25	Gain = 0dB*
1	1	1	X	—	—	—	—	—	—	—	—
1	1	1	X	1	1	1	1	1	0	62	Gain = 35dB*
1	1	1	X	1	1	1	1	1	1	63	Gain = 36dB*

**Typical gain at +25°C and V_{CC} = +9V.*

Applications Information

Transformer

To maintain rated performance into a 75Ω load, a 1:1 impedance ratio output transformer with adequate bandwidth is required. A step-up transformer with a 1:1.5 impedance ratio will increase gain and output voltage swing nominally by 1.7dB, but output noise performance will increase by the same amount.

Input Circuit

To achieve rated performance, the input of the MAX3509 must be driven differentially with 34dBmV or lower input level. The MAX3509 can be driven from a single-ended source. A slight degradation in even-order distortion at a 10W output level will result. The differential input impedance is approximately 1.2kΩ.

Most applications require a differential lowpass filter preceding the MAX3509. The filter design dictates a terminating resistance of a specified value. Place this resistance across the AC-coupled inputs (see *Typical Operating Circuit*).

The MAX3509 has sufficient gain to produce an output level of 66dBmV when driven with a 34dBmV input signal. Rated performance is achieved with this input level. When a lower input level is present, the maximum output level will be reduced proportionally and output linearity will improve. If an input level greater than 34dBmV is used, distortion performance degrades.

If a single-ended source drives the MAX3509, one of the input terminals must be capacitively coupled to ground (IN+ or IN-). The value of this capacitor must be large enough to look like a short circuit at the lowest frequency of interest. For operation at 5MHz with a 50Ω source impedance, a value of 0.1µF will suffice.

A typical model for the MAX3509 input impedance is shown in Figure 3.

Layout Issues

A well-designed PC board is an essential part of an RF circuit. For best performance, pay attention to power-supply layout issues, as well as the output circuit layout.

Exposed Paddle Thermal Considerations

The exposed paddle (EP) of the MAX3509's 20-pin TSSOP-EP package provides a low thermal resistance path to the die. It is important that the PC board on which the MAX3509 is mounted be designed to conduct heat from this contact. In addition, the EP should be provided with a low inductance path to electrical ground.

It is recommended that the EP be soldered to a ground plane on the PC board, either directly or through an array of plated via holes.

Output Circuit Layout

The differential implementation of the MAX3509's output has the benefit of reducing even-order distortion, the most significant of which is second-harmonic distortion. The degree of distortion cancellation depends on the amplitude and phase balance of the overall circuit. It is important that the traces that lead from the output pins be the same length.

Power-Supply Layout

To achieve minimal coupling between different sections of the IC, the ideal power-supply layout is a star configuration. This configuration has a large-value decoupling capacitor at the central power-supply node. The power-supply traces branch out from this node, each going to a separate power-supply node in the MAX3509 circuit. At the end of each of these traces is a decoupling capacitor that provides a very low impedance at the frequency of interest. This arrangement provides local power-supply decoupling at each power-supply pin.

The power-supply traces must be made as thick as practical to keep resistance well below 1Ω.

Ground inductance degrades distortion performance. Therefore, ground plane connections to GND, GND1, and GND2 should be made with multiple vias if possible.

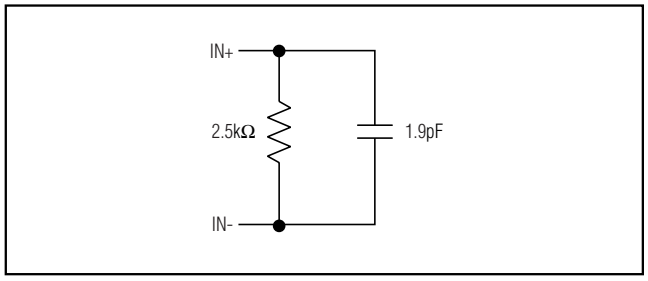


Figure 3. Typical Equivalent Input Circuit

Chip Information

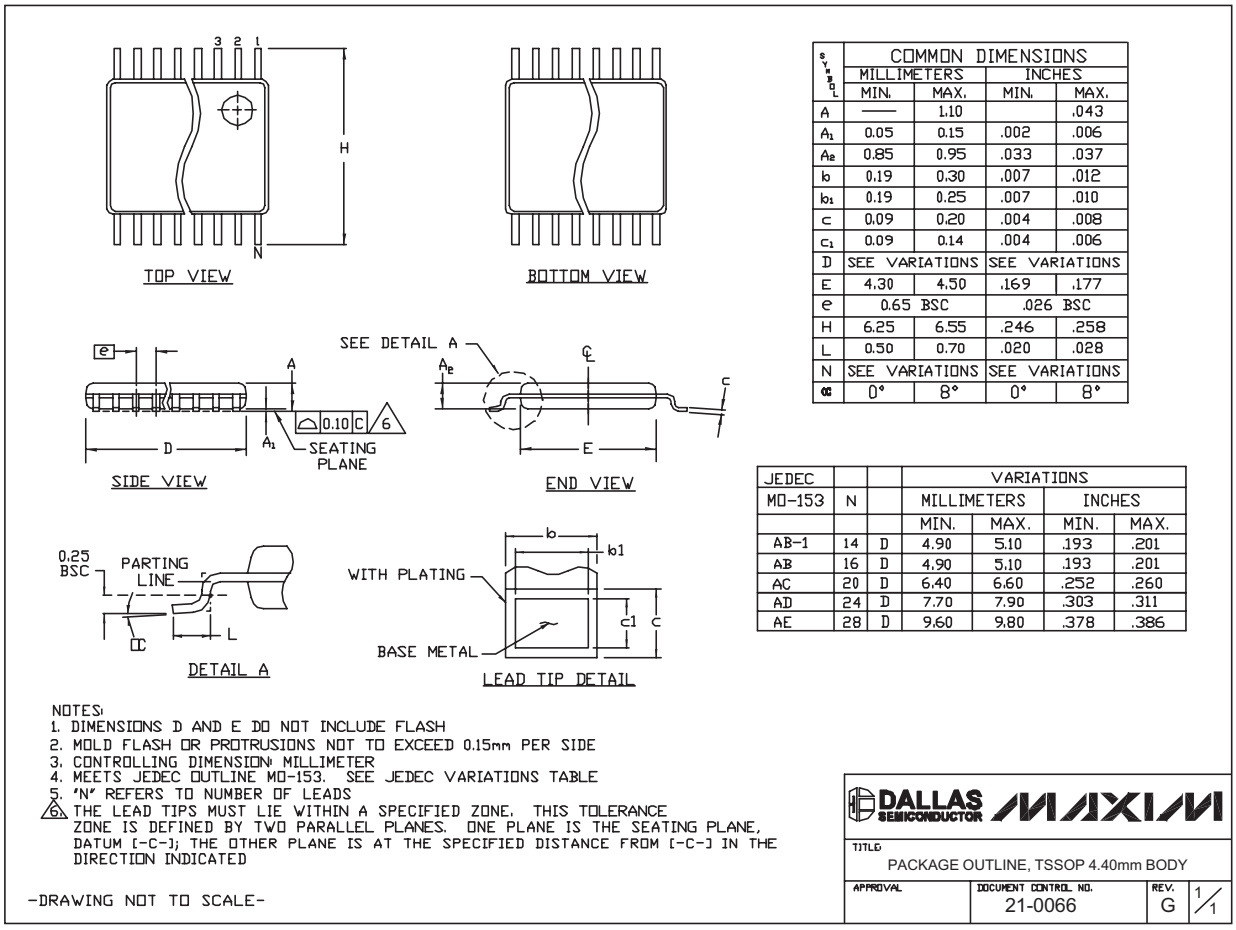
TRANSISTOR COUNT: 1085

Upstream CATV Amplifier

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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