RELIABILITY REPORT

FOR

MAX803TEXR

PLASTIC ENCAPSULATED DEVICES

July 29, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX803T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX803T is a microprocessor (µP) supervisory circuit used to monitor the power supplies in µP and digital systems. It provides excellent circuit reliability and low cost by eliminating external components and adjustments when used with 5V-powered or 3V-powered circuits.

This circuit performs a single function. It asserts a reset signal whenever the V_{CC} supply voltage declines below the preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. The MAX803T has an open-drain output stage. The open-drain /Reset ouput require a pull-up resistor than can be connected to VCC. The reset comparator is designed to ignore fast transients on V_{CC}. Reset thresholds suitable for operation with a variety of supply voltages are available.

Low supply current makes the MAX803T ideal for use in portable equipment. This device comes in a 3-pin SC-70 package.

B. Absolute Maximum Ratings

Item	Rating
Terminal Voltage (with respect to GND)	
V_{CC}	-0.3V to 6.0V
RESET (open drain)	-0.3V to 6.0V
Input Current, V_{CC}	20mA
Output Current, RESET	20mA
Rate of Rise, V_{CC}	100V/µs
Operating Temperature Range	-40°C to +105°C
Storage Temp.	-65◦C to +160◦C
Lead Temp. (10 sec.)	+300◦C
Power Dissipation	
3-Lead SC70	174mW
Derates above +70◦C	
3-Lead SC70	2.17mW/◦C

II. Manufacturing Information

A. Description/Function:	3-Pin Microprocessor Reset Circuit
B. Process:	S8 Standard .8 micron silicon gate CMOS
C. Number of Device Transistors:	380
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	January, 2000

III. Packaging Information

A. Package Type:	**3 Lead SC70**
B. Lead Frame:	Alloy 42
C. Lead Finish:	Solder Plate
D. Die Attach:	Non-Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-1601-0082
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	30 x 30 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	TiW/AlCu/TiWN
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 400 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 2.71 \times 10^{-9}$ $\lambda = 2.71$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5033) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The MS42-2 die type has been found to have all pins able to withstand a transient pulse of $\pm$800V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm$250mA and/or $\pm$20V.

Table 1
Reliability Evaluation Test Results

MAX803TEXR

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135◦C Biased Time = 192 hrs.	DC Parameters & functionality		400	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121◦C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SC70	77	0
85/85	Ta = 85◦C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65◦C/150◦C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Process/Package Data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

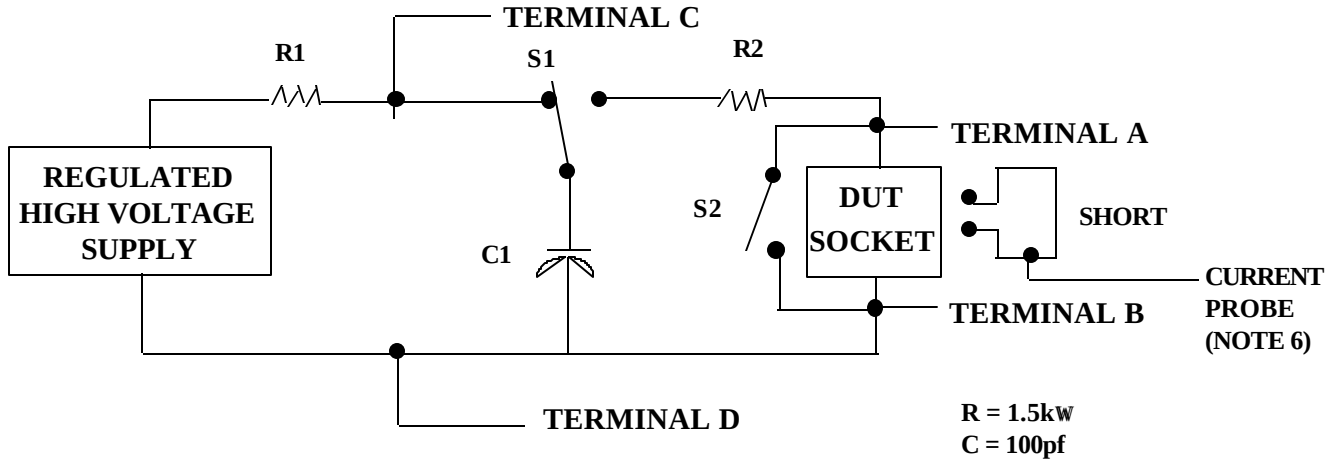
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

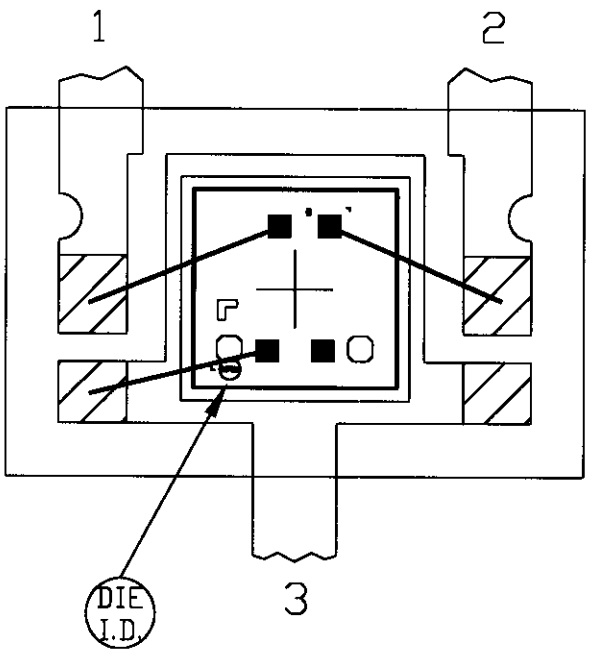
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





SCALE: 40x

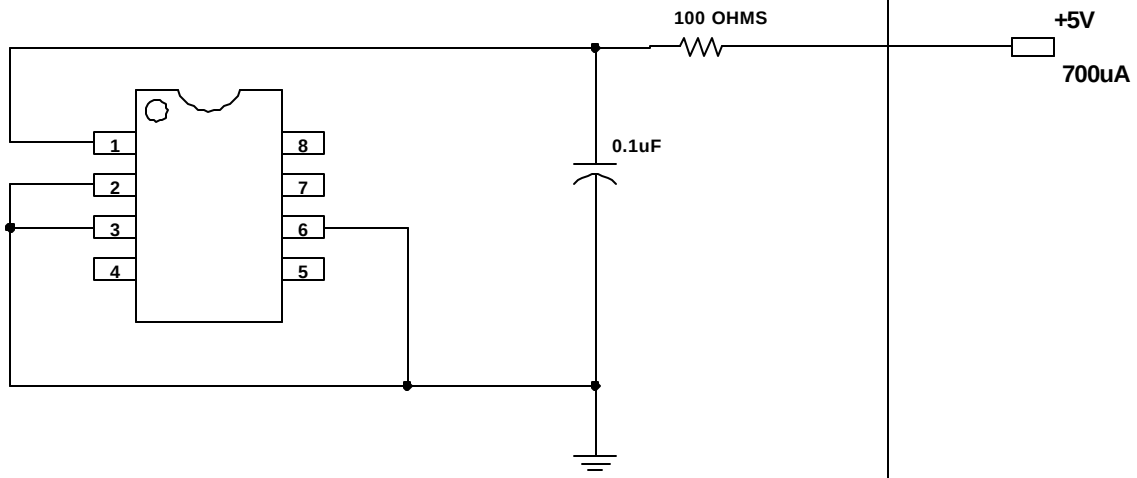
CAVITY DOWN

BONDABLE AREA

PKG.CODE: X3-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 34x35	PKG. DESIGN			BUILDSHEET NUMBER: 05-1601-0082 / REV.: A

ONCE PER SOCKET

ONCE PER BOARD



8-DIP

DEVICES: MAX 941/809/810/823/824/825/803
MAX 6381/6835
MAX. EXPECTED CURRENT = 700uA AND 15uA

DRAWN BY: HAK TAN
NOTES: 15 uA FOR MAX 6381