RELIABILITY REPORT

FOR

MAX8521ETP

PLASTIC ENCAPSULATED DEVICES

June 29, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Reviewed by

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Conclusion

The MAX8521 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX8521 is designed to drive thermo-electric coolers (TECs) in space-constrained optical modules. The device delivers ±1.5A output current and controls the TEC current to eliminate harmful current surges. On-chip FETs minimize external components and high switching frequency reduces the size of external components.

The MAX8521 operates from a single supply and bias the TEC between the outputs of two synchronous buck regulators. This operation allows for temperature control without "dead zones" or other nonlinearities at low current. This arrangement ensures that the control system does not hunt when the set point is very close to the natural operating point, requiring a small amount of heating or cooling. An analog control signal precisely sets the TEC current.

The device features accurate, individually adjustable heating current limit and cooling current limit, along with maximum TEC voltage limit to improve the reliability of optical modules. An analog output signal monitors the TEC current. A unique ripple cancellation scheme helps reduce noise.

The MAX8521 is also available in a 5mm x 5mm thin QFN, as well as a space-saving 3mm x 3mm UCSP™, with a pin-selectable switching frequency of 500kHz or 1MHz.

B. Absolute Maximum Ratings

Item	Rating
VDD to GND	-0.3V to +6V
SHDN, MAXV, MAXIP, MAXIN, CTLI to GND	-0.3V to +6V
COMP, FREQ, OS1, OS2, CS, REF, ITEC to GND	-0.3V to (VDD + 0.3V)
PVDD1, PVDD2 to GND	-0.3V to (VDD + 0.3V)
PVDD1, PVDD2 to VDD	-0.3V to +0.3V
PGND1, PGND2 to GND	-0.3V to +0.3V
COMP, REF, ITEC Short to GND	Indefinite
LX Current (Note 1)	±2.25A LX Current
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
20-Pin 5mm x 5mm x 0.9mm QFN (Note 2)	1670mW
Derates above +70°C	
20-Pin 5mm x 5mm x 0.9mm QFN (Note 2)	20.8mW/°C

Note 1: LX has internal clamp diodes to PGND and PVDD. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.
Note 2: Solder underside metal slug to PC board ground plane.

II. Manufacturing Information

A. Description/Function:	Smallest TEC Power Drivers for Optical Modules
B. Process:	B8 (Standard 0.8 micron silicon gate CMOS)
C. Number of Device Transistors:	3007
D. Fabrication Location:	California, USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	October, 2002

III. Packaging Information

A. Package Type:	**20-Pin QFN (5x5)**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (2.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0102
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1

IV. Die Information

A. Dimensions:	120 x 120 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.62 \times 10^{-9}$

$\lambda = 22.62$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6077) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PM83-1 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA.

Table 1
Reliability Evaluation Test Results

MAX8521ETP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

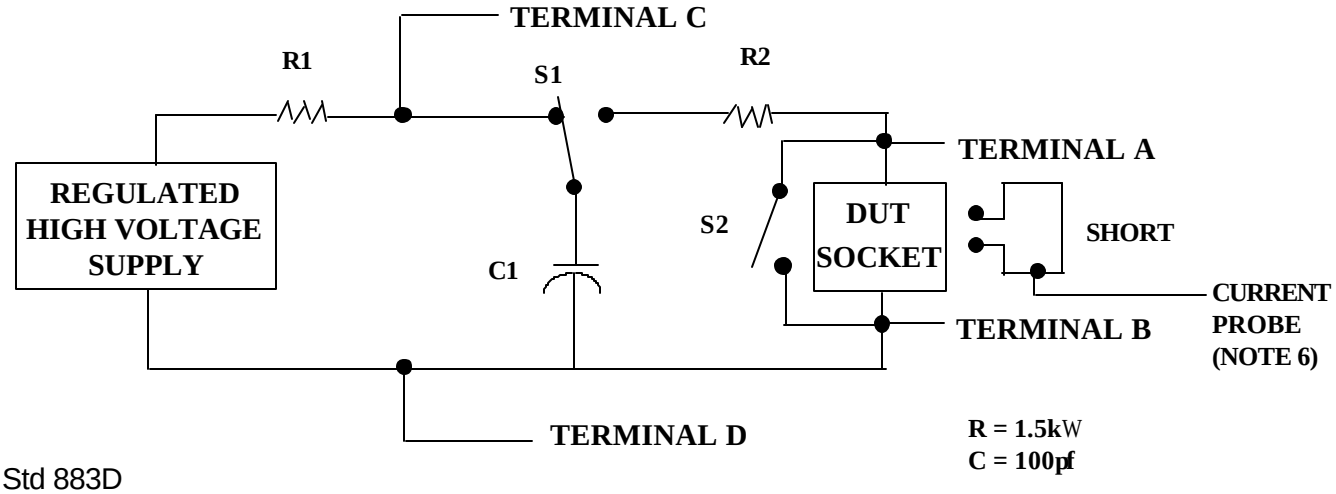
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

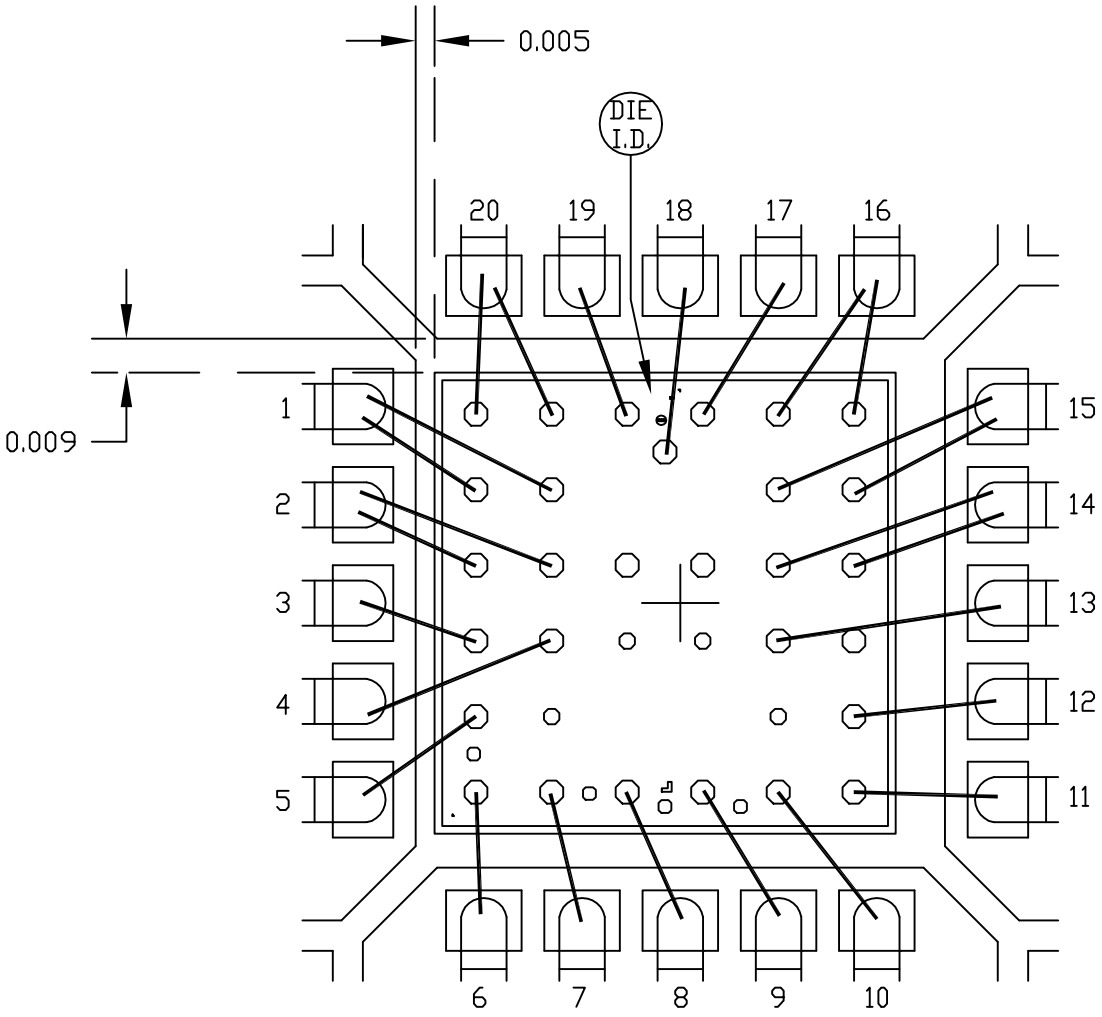
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8

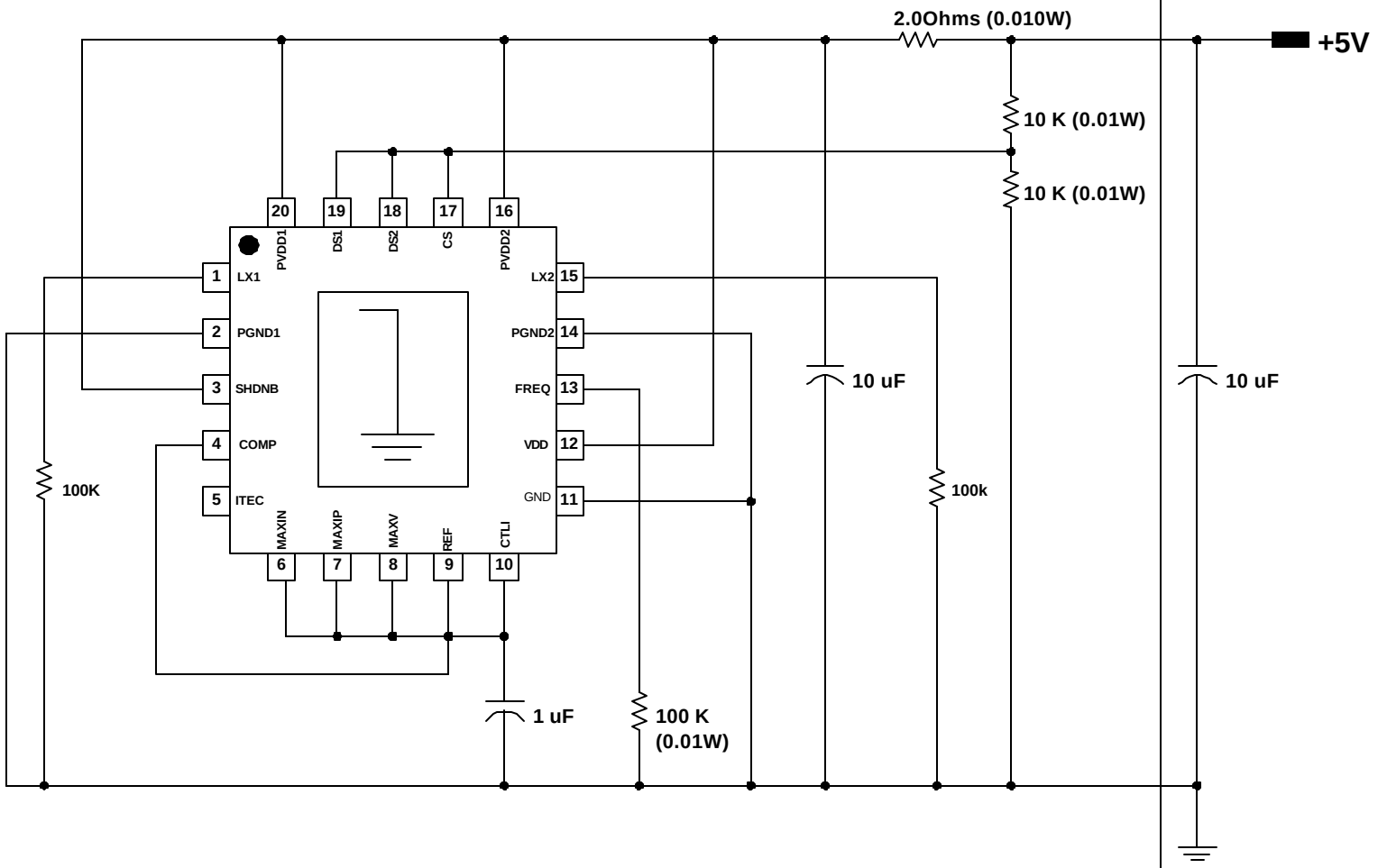
5x5x0.8 MM QFN THIN PKG. EXPOSED PAD PKG.



PKG. CODE: T2055-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 138x138	PKG.			BOND DIAGRAM #: 05-9000-0102 REV: A
	DESIGN			

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 8520
PACKAGE: 20-QFN
MAX. EXPECTED CURRENT = 25mA

DRAWN BY: TEK TAN
NOTES: