19-3769; Rev 0; 9/05

EVALUATION KIT AVAILABLE

25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

General Description

The MAX9709 stereo/mono, Class D audio power amplifier delivers up to 2 x 25W into an 8Ω stereo mode and 1 x 50W into a 4Ω load in mono mode while offering up to 87% efficiency. The MAX9709 provides Class AB amplifier performance with the benefits of Class D efficiency, eliminating the need for a bulky heatsink and conserving power. The MAX9709 operates from a single +10V to +22V supply, driving the load in a BTL configuration.

The MAX9709 offers two modulation schemes: a fixed-frequency modulation (FFM) mode, and a spread-spectrum modulation (SSM) mode that reduces EMI-radiated emissions. The MAX9709 can be synchronized to an external clock from 600kHz to 1.2MHz. A synchronized output allows multiple units to be cascaded in the system.

Features include fully differential inputs, comprehensive click-and-pop suppression, and four selectable-gain settings (22dB, 25dB, 29.5dB, and 36dB). A pin-programmable thermal flag provides seven different thermal warning thresholds. Short-circuit and thermal-overload protection prevent the device from being damaged during a fault condition.

The MAX9709 is available in 56-pin TQFN (8mm x 8mm x 0.8mm) and 64-pin TQFP (10mm x 10mm x 1.4mm) packages, and is specified over the extended -40°C to +85°C temperature range.

Applications

LCD TVs

PDP TVs

Automotive

PC/HiFi Audio Solutions

Pin Configurations appear at end of data sheet.

Features

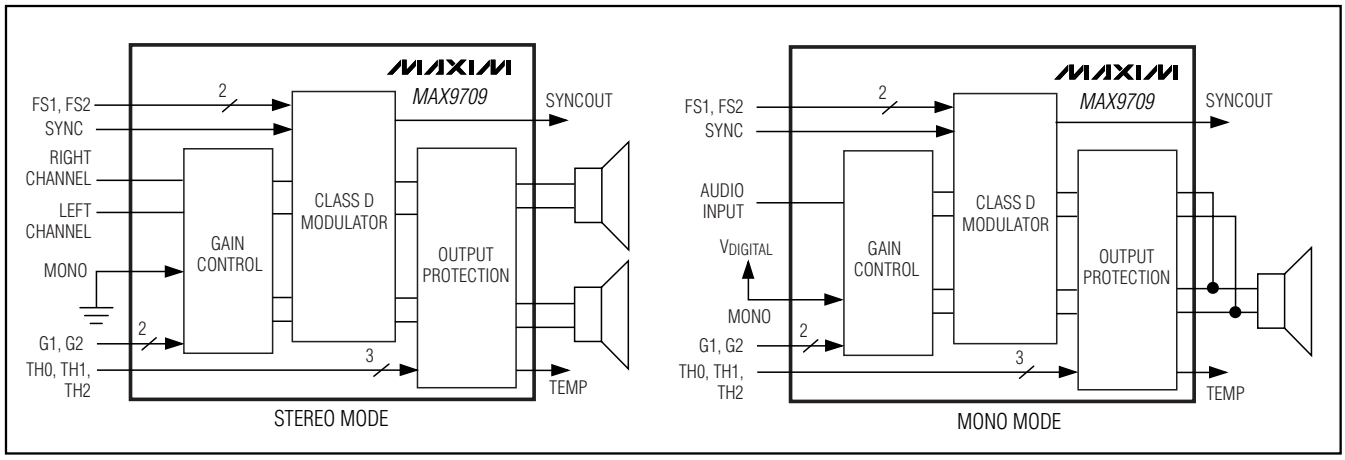
- **2 x 25W Output Power in Stereo Mode (8Ω, THD = 10%)**
- **1 x 50W Output Power in Mono Mode (4Ω, THD = 10%)**
- **High Efficiency: Up to 87%**
- **Filterless Class D Amplifier**
- **Unique Patented Spread-Spectrum Mode**
- **Programmable Gain (+22dB, +25dB, +29.5dB, +36dB)**
- **High PSRR (90dB at 1kHz)**
- **Differential Inputs Suppress Common-Mode Noise**
- **Shutdown and Mute Control**
- **Integrated Click-and-Pop Suppression**
- **Low 0.1% THD+N**
- **Current Limit and Thermal Protection**
- **Programmable Thermal Flag**
- **Clock Synchronization Input and Output**
- **Available in Thermally Efficient, Space-Saving Packages: 56-Pin TQFN and 64-Pin TQFP**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9709ETN+	-40°C to +85°C	56 TQFN-EP**	T5688-3
MAX9709ECB+*	-40°C to +85°C	64 TQFP-EP**	C64E-6

+Denotes lead-free package.
**Future product—Contact factory for availability.*
***EP = Exposed paddle.*

Simplified Block Diagram



25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

ABSOLUTE MAXIMUM RATINGS

PV_{DD}, V_{DD} to PGND, GND .....-0.3 to +30V
PV_{DD} to V_{DD} .....-0.3V to +0.3V
OUTR+, OUTR-, OUTL+,
OUTL- to PGND, GND.....-0.3V to (PV_{DD} + 0.3V)
C1N to GND .....-0.3V to (PV_{DD} + 0.3V)
C1P to GND.....(PV_{DD} - 0.3V) to (CPV_{DD} + 0.3V)
CPV_{DD} to GND .....(PV_{DD} - 0.3V) to +40V
All Other Pins to GND.....-0.3V to +12V
Continuous Input Current (except PV_{DD}, V_{DD}, OUTR+,
OUTR-, OUTL+, and OUTL-) 20mA

Continuous Power Dissipation (T_A = +70°C)
56-Pin Thin QFN (derate 47.6mW/°C above +70°C) 3.81W
64-Pin TQFP (derate 43.5mW/°C above +70°C).....3.48W
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Thermal Resistance (θ_{JC})
56-Pin Thin QFN… .....0.6°C/W
64-Pin TQFP…….....2°C/W
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(PV_{DD} = V_{DD} = +20V, PGND = GND = 0V, C_{SS} = 0.47µF, C_{REG} = 0.01µF, C1 = 0.1µF, C2 = 1µF, R_{LOAD} = ∞, MONO = low (stereo mode), $\overline{SHDN}$ = $\overline{MUTE}$ = high, G1 = low, G2 = high (A_V = 22dB), FS1 = FS2 = high (SSM), SYNCIN = low. All load resistors (R_L) are connected between OUT_+ and OUT_-, unless otherwise stated. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Inferred from PSRR test		10		22	V
Shutdown Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = low			0.1	1	µA
Shutdown to Full Operation	t_{SON}				100		ms
Mute to Full Operation	t_{MUTE}				100		ms
Input Impedance	R_{IN}	G1 = 0, G2 = 1		50	85	125	kΩ
		G1 = 1, G2 = 1		40	63	90	
		G1 = 1, G2 = 0		25	43	60	
		G1 = 0, G2 = 0		12	21	30	
Output Pulldown Resistance		$\overline{SHDN}$ = GND			600		kΩ
Output Offset Voltage	V_{OS}	AC-coupled input, measured between OUT_+ and OUT_-			3	±40	mV
Power-Supply Rejection Ratio	PSRR	PV_{DD} = 10V to 22V		67	90		dB
		200mV_{P-P} ripple (Note 2)	f_{RIPPLE} = 1kHz		90		
			f_{RIPPLE} = 20kHz		52		
Common-Mode Rejection Ratio	CMRR	DC, input referred		49	70		dB
		f = 20Hz to 20kHz, input referred			60		
Switch On-Resistance	R_{DS}	One power switch			0.3	0.6	Ω
Switching Frequency	f_{SW}	FS1	FS2				kHz
		0	0	180	200	220	
		1	1 (SSM)		200		
		1	0		160		
		0	1		250		
Oscillator Spread Bandwidth		FS1 = FS2 = high (SSM)			±2		%
SYNCIN Lock Range		Equal to f_{SW} x 4		600		1200	kHz

ELECTRICAL CHARACTERISTICS (continued)

(PV_{DD} = V_{DD} = +20V, PGND = GND = 0V, C_{SS} = 0.47µF, C_{REG} = 0.01µF, C1 = 0.1µF, C2 = 1µF, R_{LOAD} = ∞, MONO = low (stereo mode), $\overline{SHDN}$ = $\overline{MUTE}$ = high, G1 = low, G2 = high (A_V = 22dB), FS1 = FS2 = high (SSM), SYNCIN = low. All load resistors (R_L) are connected between OUT_+ and OUT_-, unless otherwise stated. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Gain	A_V	G1 = 0, G2 = 1			21.6	22.0	22.3	dB
		G1 = 1, G2 = 1			24.9	25.0	25.6	
		G1 = 1, G2 = 0			29.2	29.5	29.9	
		G1 = 0, G2 = 0			35.9	36.0	36.6	
$\overline{TEMP}$ Flag Threshold	T_{FLAG}	TH2	TH1	TH0				°C
		0	0	0		80		
		0	0	1		90		
		0	1	0		100		
		0	1	1		110		
		1	0	0		120		
		1	0	1		129		
		1	1	0		139		
		1	1	1				
$\overline{TEMP}$ Flag Accuracy		From +80°C to +140°C					±6	°C
$\overline{TEMP}$ Flag Hysteresis						2		°C
STEREO MODE (R_{LOAD} = 8Ω, Note 3)								
Quiescent Current		$\overline{MUTE}$ = 1, R_{LOAD} = ∞				20	33	mA
		$\overline{MUTE}$ = 0				6.5	13	
Output Power	P_{OUT}	f = 1kHz, THD = 10%, T_A = +25°C		P_{VDD} = 20V	25			W
				P_{VDD} = 22V		29		
				P_{VDD} = 12V, R_{LOAD} = 4Ω		15		
Total Harmonic Distortion Plus Noise	THD+N	f = 1kHz, BW = 22Hz to 22kHz, P_{OUT} = 12W				0.1		%
Signal-to-Noise Ratio	SNR	P_{OUT} = 10W		22Hz to 22kHz		91		dB
				A-weighted		96		
Efficiency	η	P_{OUT} = 25W + 25W, f = 1kHz				87		%
Left-Right Channel Gain Matching		R_{LOAD} = ∞				0.2		%

25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

ELECTRICAL CHARACTERISTICS (continued)

(PV_{DD} = V_{DD} = +20V, PGND = GND = 0V, C_{SS} = 0.47µF, C_{REG} = 0.01µF, C1 = 0.1µF, C2 = 1µF, R_{LOAD} = ∞, MONO = low (stereo mode), $\overline{SHDN}$ = $\overline{MUTE}$ = high, G1 = low, G2 = high (A_V = 22dB), FS1 = FS2 = high (SSM), SYNCIN = low. All load resistors (R_L) are connected between OUT_+ and OUT_-, unless otherwise stated. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Short-Circuit Current Threshold	I_{SC}	R_{LOAD} = 0Ω			3		A
Click-and-Pop Level	K_{CP}	Peak voltage, 32 samples/second, A-weighted (Notes 2, 5)	Into shutdown		-63		dBV
			Out of shutdown		-55		
MONO MODE (R_{LOAD} = 4Ω, MONO = HIGH) (Note 6)							
Quiescent Current		$\overline{MUTE}$ = 1, R_{LOAD} = ∞			20		mA
		$\overline{MUTE}$ = 0			6.5		
Output Power	P_{OUT}	f = 1kHz, THD = 10%	R_{LOAD} = 8Ω		25		W
			R_{LOAD} = 4Ω		50		
Total Harmonic Distortion Plus Noise	THD+N	f = 1kHz, BW = 22Hz to 22kHz, P_{OUT} = 22W			0.09		%
Signal-to-Noise Ratio	SNR	P_{OUT} = 10W	20Hz to 20kHz		91		dB
			A-weighted		95		
Efficiency	η	P_{OUT} = 54W, f = 1kHz			86		%
Output Short-Circuit Current Threshold	I_{SC}	R_{LOAD} = 0Ω			6		A
Click-and-Pop Level	K_{CP}	Peak voltage, 32 samples/second, A-weighted (Notes 2, 5)	Into shutdown		-60		dBV
			Out of shutdown		-63		
DIGITAL INPUTS ($\overline{SHDN}$, $\overline{MUTE}$, G1, G2, FS1, FS2, TH0, TH1, TH2, SYNCIN, MONO)							
Logic-Input Current	I_{IN}	0 to 12V				1	µA
Logic-Input High Voltage	V_{IH}			2.5			V
Logic-Input Low Voltage	V_{IL}					0.8	V
OPEN-DRAIN OUTPUTS ($\overline{TEMP}$, SYNCOUT)							
Open-Drain Output Low Voltage	V_{OL}	I_{SINK} = 3mA				0.4	V
Leakage Current	I_{LEAK}	V_{PULLUP} = 5.5V			0.2		µA

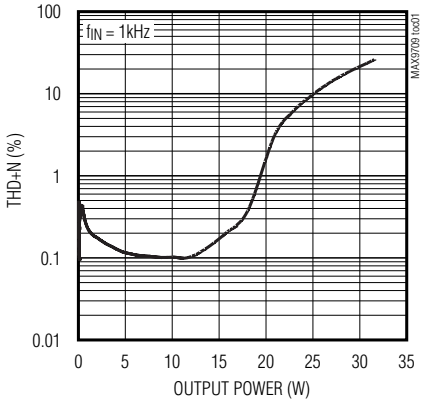
Note 1: All devices are 100% production tested at +25°C. All temperature limits are guaranteed by design.
Note 2: Inputs AC-coupled to GND.
Note 3: Testing performed with an 8Ω resistive load in series with a 68µH inductive load across the BTL outputs.
Note 4: Minimum output power is guaranteed by pulse testing.
Note 5: Testing performed with an 8Ω resistive load in series with a 68µH inductive load connected across BTL outputs. Mode transitions are controlled by $\overline{SHDN}$.
Note 6: Testing performed with a 4Ω resistive load in series with a 33µH inductive load across the BTL outputs.

25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

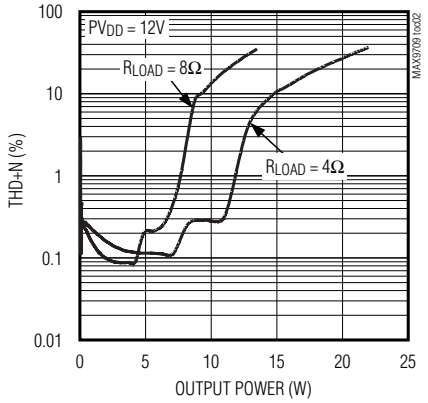
Typical Operating Characteristics

(PV_{DD} = V_{DD} = +20V, PGND = GND = 0V, C_{SS} = 0.47µF, C_{REG} = 0.01µF, C1 = 0.1µF, C2 = 1µF, R_{LOAD} = 8Ω, $\overline{SHDN}$ = high, MONO = low, $\overline{MUTE}$ = high, G1 = low, G2 = high, FS1 = FS2 = high (SSM), SYNCIN = low. All load resistors (R_L) are between OUT_+ and OUT_-, T_A = +25°C, unless otherwise stated.)

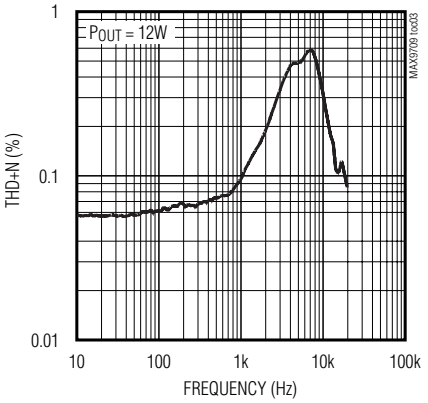
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (STEREO MODE)



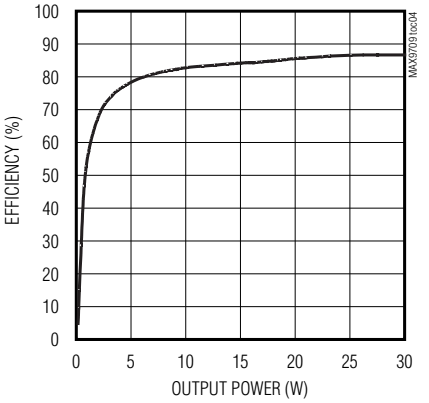
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (STEREO MODE)



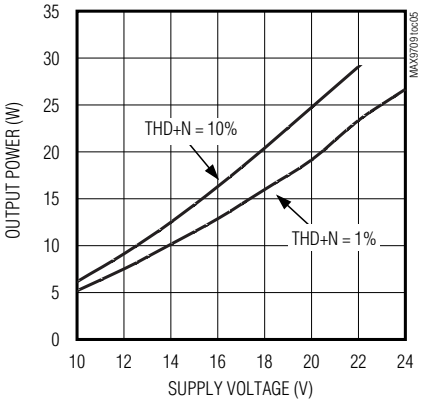
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (STEREO MODE)



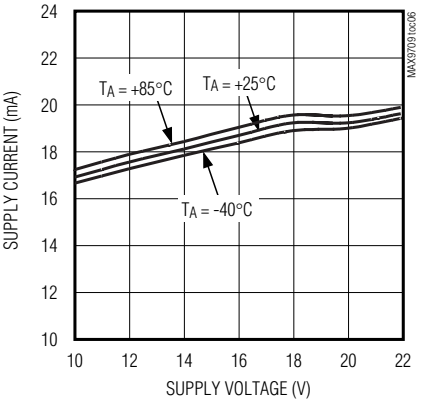
EFFICIENCY vs. OUTPUT POWER (STEREO MODE)



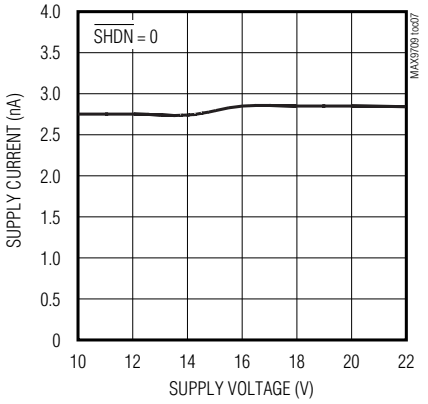
OUTPUT POWER vs. SUPPLY VOLTAGE (STEREO MODE)



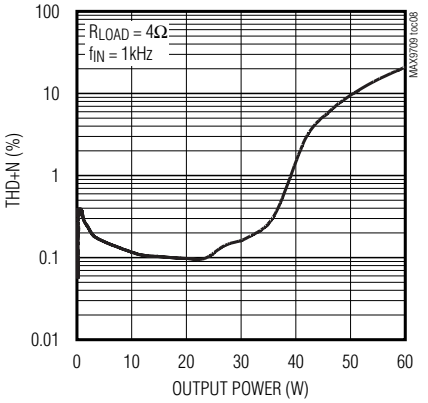
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE (STEREO MODE)



SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (MONO MODE)

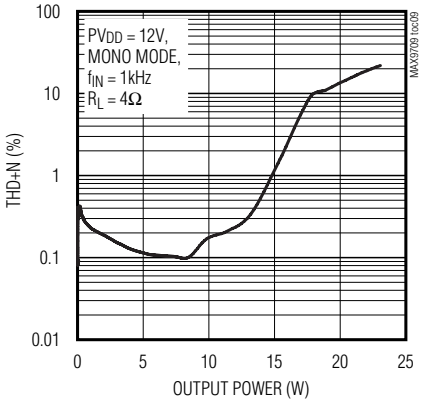


25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

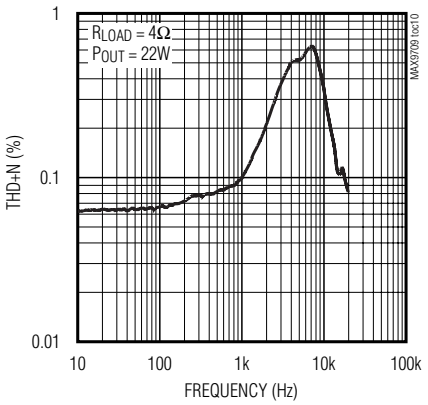
Typical Operating Characteristics (continued)

(PV_{DD} = V_{DD} = +20V, PGND = GND = 0V, C_{SS} = 0.47µF, C_{REG} = 0.01µF, C1 = 0.1µF, C2 = 1µF, R_{LOAD} = 8Ω, $\overline{SHDN}$ = high, MONO = low, $\overline{MUTE}$ = high, G1 = low, G2 = high, FS1 = FS2 = high (SSM), SYNCIN = low. All load resistors (R_L) are between OUT_+ and OUT_-, T_A = +25°C, unless otherwise stated.)

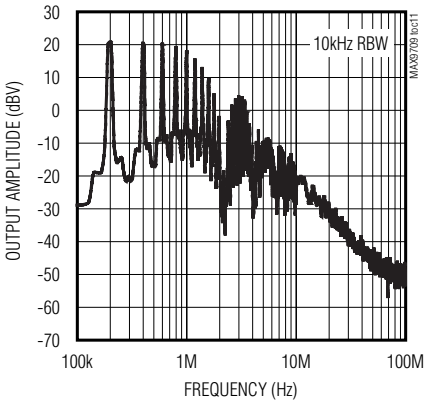
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



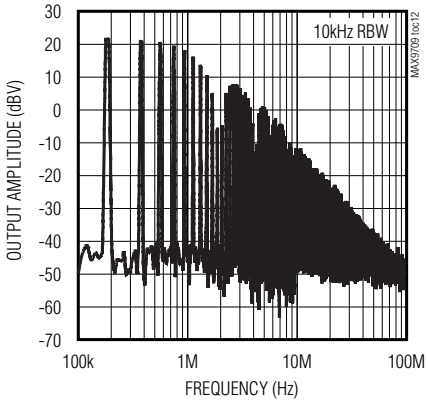
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MONO MODE)



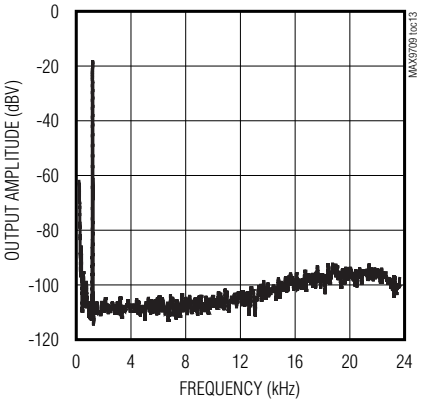
WIDEBAND OUTPUT SPECTRUM (SSM MODE)



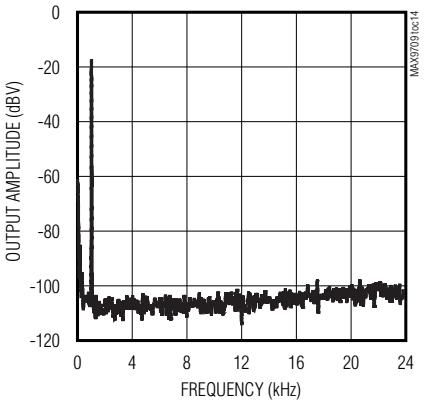
WIDEBAND OUTPUT SPECTRUM (FFM MODE)



OUTPUT FREQUENCY SPECTRUM (SSM MODE)



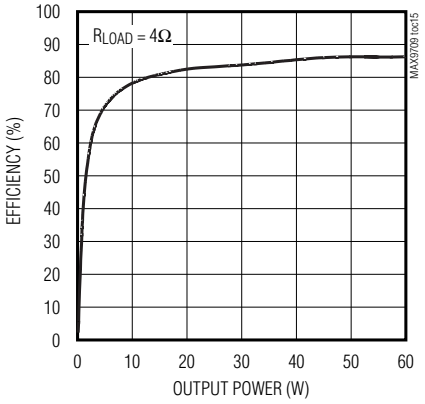
OUTPUT FREQUENCY SPECTRUM (FFM MODE)



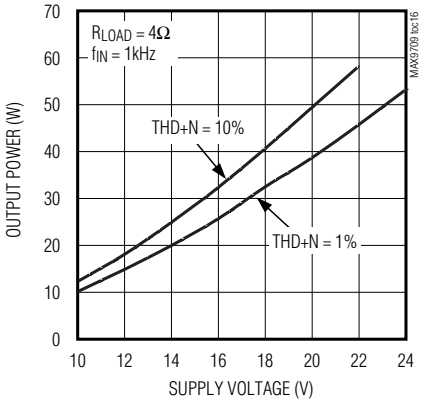
Typical Operating Characteristics (continued)

(PV_{DD} = V_{DD} = +20V, PGND = GND = 0V, C_{SS} = 0.47µF, C_{REG} = 0.01µF, C1 = 0.1µF, C2 = 1µF, R_{LOAD} = 8Ω, $\overline{SHDN}$ = high, MONO = low, $\overline{MUTE}$ = high, G1 = low, G2 = high, FS1 = FS2 = high (SSM), SYNCIN = low. All load resistors (R_L) are between OUT_+ and OUT_-, T_A = +25°C, unless otherwise stated.)

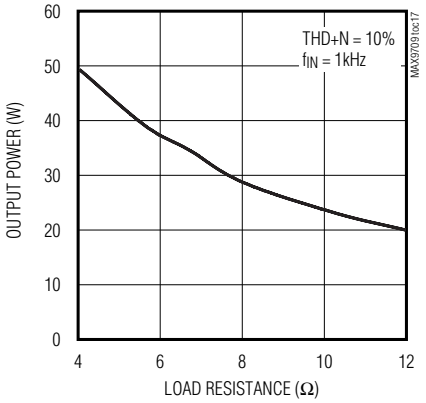
EFFICIENCY vs. OUTPUT POWER (MONO MODE)



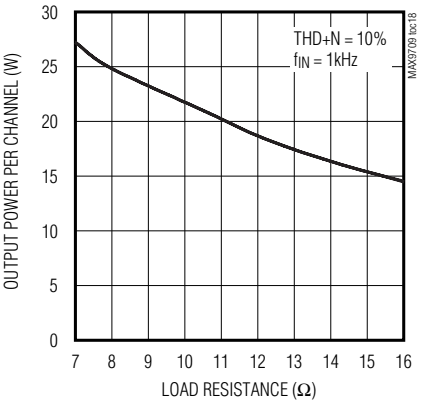
OUTPUT POWER vs. SUPPLY VOLTAGE (MONO MODE)



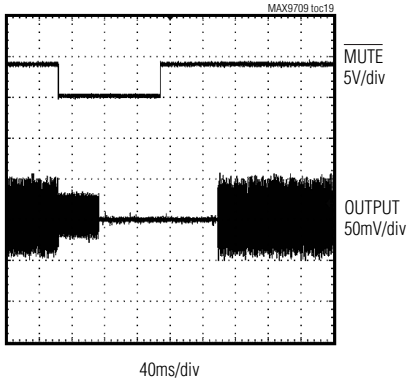
OUTPUT POWER vs. LOAD RESISTANCE (MONO MODE)



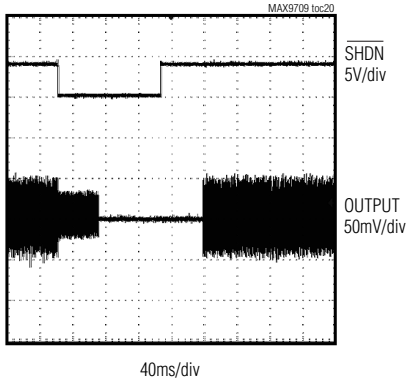
OUTPUT POWER vs. LOAD RESISTANCE (STEREO MODE)



MUTE RESPONSE



SHUTDOWN RESPONSE

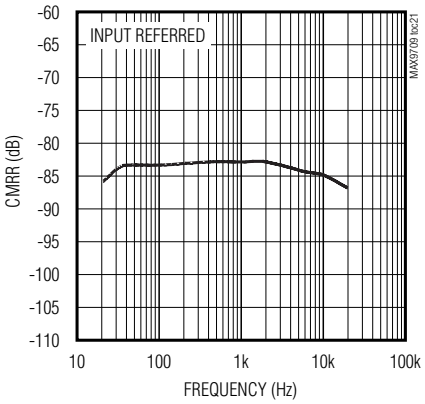


25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

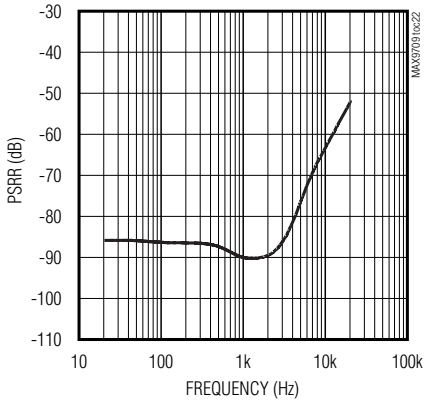
Typical Operating Characteristics (continued)

(PV_{DD} = V_{DD} = +20V, PGND = GND = 0V, C_{SS} = 0.47µF, C_{REG} = 0.01µF, C1 = 0.1µF, C2 = 1µF, R_{LOAD} = 8Ω, $\overline{SHDN}$ = high, MONO = low, $\overline{MUTE}$ = high, G1 = low, G2 = high, FS1 = FS2 = high (SSM), SYNCIN = low. All load resistors (R_L) are between OUT_+ and OUT_-, T_A = +25°C, unless otherwise stated.)

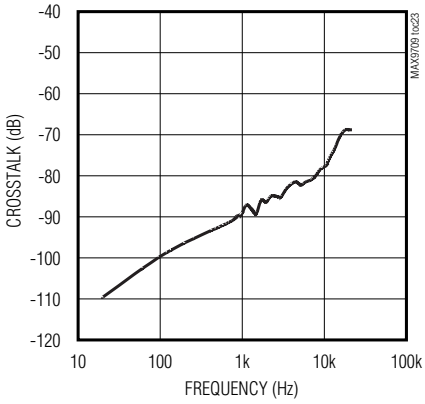
COMMON-MODE REJECTION RATIO vs. FREQUENCY



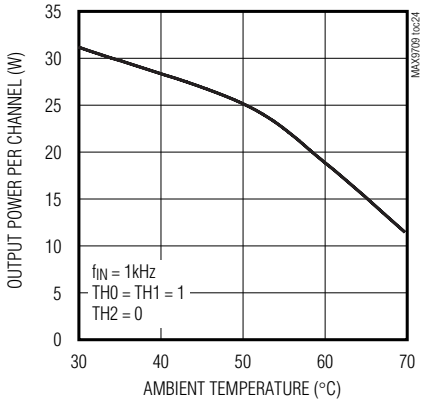
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



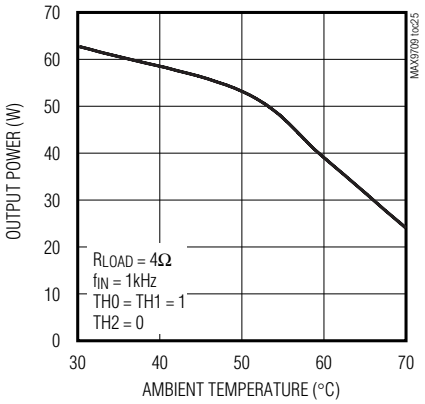
CROSSTALK vs. FREQUENCY



MAXIMUM STEADY-STATE OUTPUT POWER vs. TEMPERATURE (STEREO MODE)



MAXIMUM STEADY-STATE OUTPUT POWER vs. TEMPERATURE (MONO MODE)*



*MEASURED WITH THE MAX9709EVKIT, JUNCTION TEMPERATURE MAINTAINED AT +110°C.

Pin Description

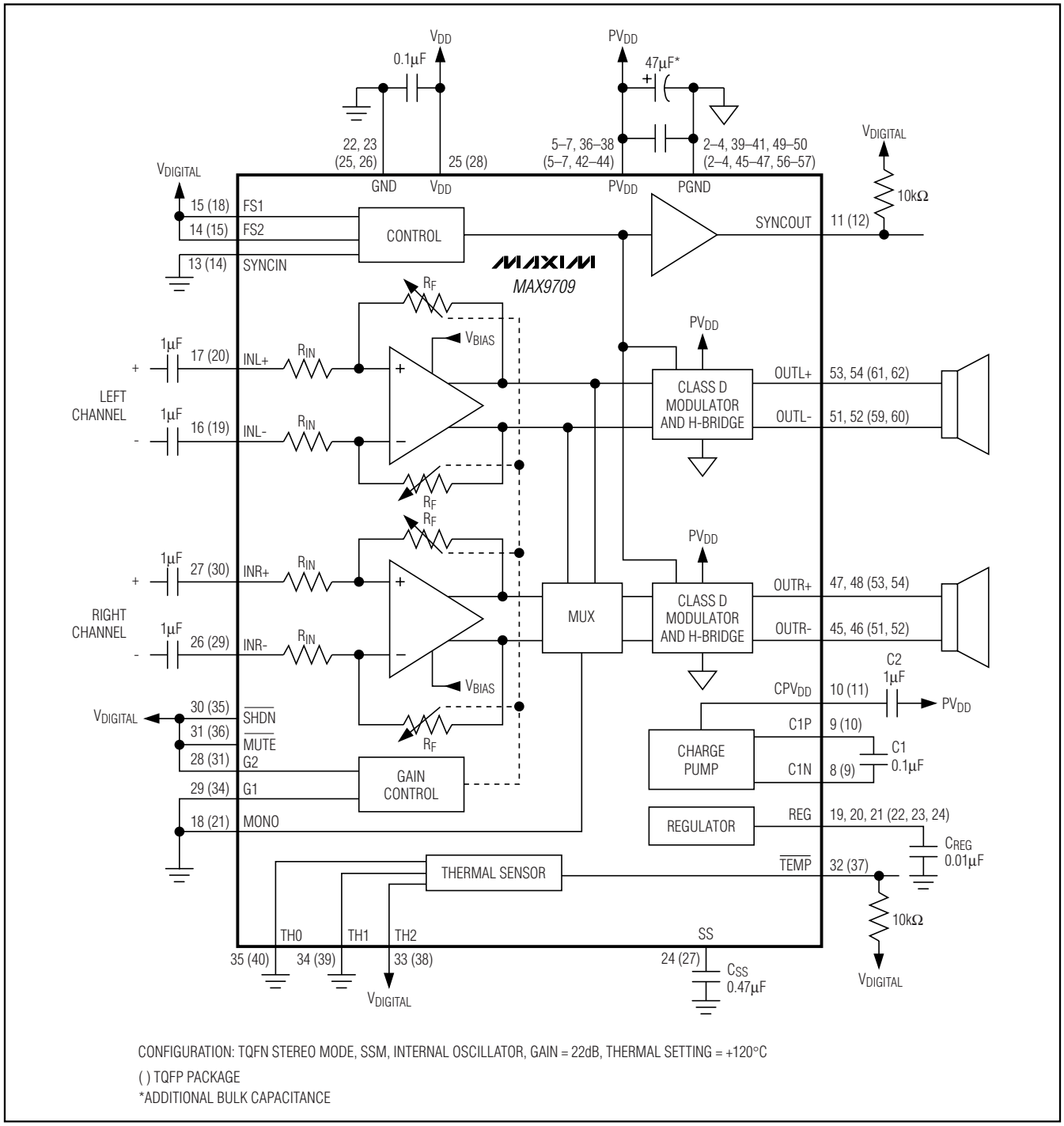
PIN		NAME	FUNCTION
TQFP	TQFN		
1, 8, 13, 16, 17, 32, 33, 41, 48, 49, 50, 55, 58, 63, 64	1, 12, 42, 43, 44, 55, 56	N.C.	No Connection. Not internally connected.
2, 3, 4, 45, 46, 47, 56, 57	2, 3, 4, 39, 40, 41, 49, 50	PGND	Power Ground
5, 6, 7, 42, 43, 44	5, 6, 7, 36, 37, 38	PV_{DD}	Positive Power Supply. Bypass to PGND with a 0.1µF and a 47µF capacitor with the smallest capacitor placed as close to pins as possible.

Pin Description (continued)

PIN		NAME	FUNCTION
TQFP	TQFN		
9	8	C1N	Charge-Pump Flying Capacitor C1, Negative Terminal
10	9	C1P	Charge-Pump Flying Capacitor C1, Positive Terminal
11	10	CPV_{DD}	Charge-Pump Power Supply. Bypass to PV_{DD} with a 1µF capacitor as close to pin as possible.
12	11	SYNCOUT	Open-Drain Slew-Rate-Limited Clock Output. Pullup with a 10kΩ to resistor to REG.
14	13	SYNCIN	Clock Synchronization Input. Allows for synchronization of the internal oscillator with an external clock.
15	14	FS2	Frequency Select 2
18	15	FS1	Frequency Select 1
19	16	INL-	Left-Channel Negative Input (Stereo Mode Only)
20	17	INL+	Left-Channel Positive Input (Stereo Mode Only)
21	18	MONO	Mono/Stereo Mode Input. Drive logic high for mono mode. Drive logic low for stereo mode.
22, 23, 24	19, 20, 21	REG	Internal Regulator Output Voltage (6V). Bypass with a 0.01µF capacitor to GND.
25, 26	22, 23	GND	Analog Ground
27	24	SS	Soft-Start. Connect a 0.47µF capacitor to GND to utilize soft-start power-up sequence.
28	25	V_{DD}	Analog Power Supply. Bypass to GND with a 0.1µF capacitor as close to pin as possible.
29	26	INR-	Right-Channel Negative Input. In mono mode, INR- is the negative input.
30	27	INR+	Right-Channel Positive Input. In mono mode, INR+ is the positive input.
31	28	G1	Gain Select input 1
34	29	G2	Gain Select input 2
35	30	$\overline{SHDN}$	Active-Low Shutdown Input. Drive $\overline{SHDN}$ high for normal operation. Drive $\overline{SHDN}$ low to place the device in shutdown mode.
36	31	$\overline{MUTE}$	Active-Low Mute Input. Drive logic low to place the device in mute. In mute mode, Class D output stage is no longer switching. Drive high for normal operation. $\overline{MUTE}$ is internally pulled up to V_{REG} with a100kΩ resistor.
37	32	$\overline{TEMP}$	Thermal Flag Output, Open Drain. Pullup with a 10kΩ resistor to REG.
38	33	TH2	Temperature Flag Threshold Select Input 2
39	34	TH1	Temperature Flag Threshold Select Input 1
40	35	TH0	Temperature Flag Threshold Select Input 0
51, 52	45, 46	OUTR-	Right-Channel Negative Output
53, 54	47, 48	OUTR+	Right-Channel Positive Output
59, 60	51, 52	OUTL-	Left-Channel Negative Output
61, 62	53, 54	OUTL+	Left-Channel Positive Output
EP	EP	GND	Exposed Paddle. Connect to GND with multiple vias for best heat dissipation.

25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

Typical Application Circuits/Functional Diagrams



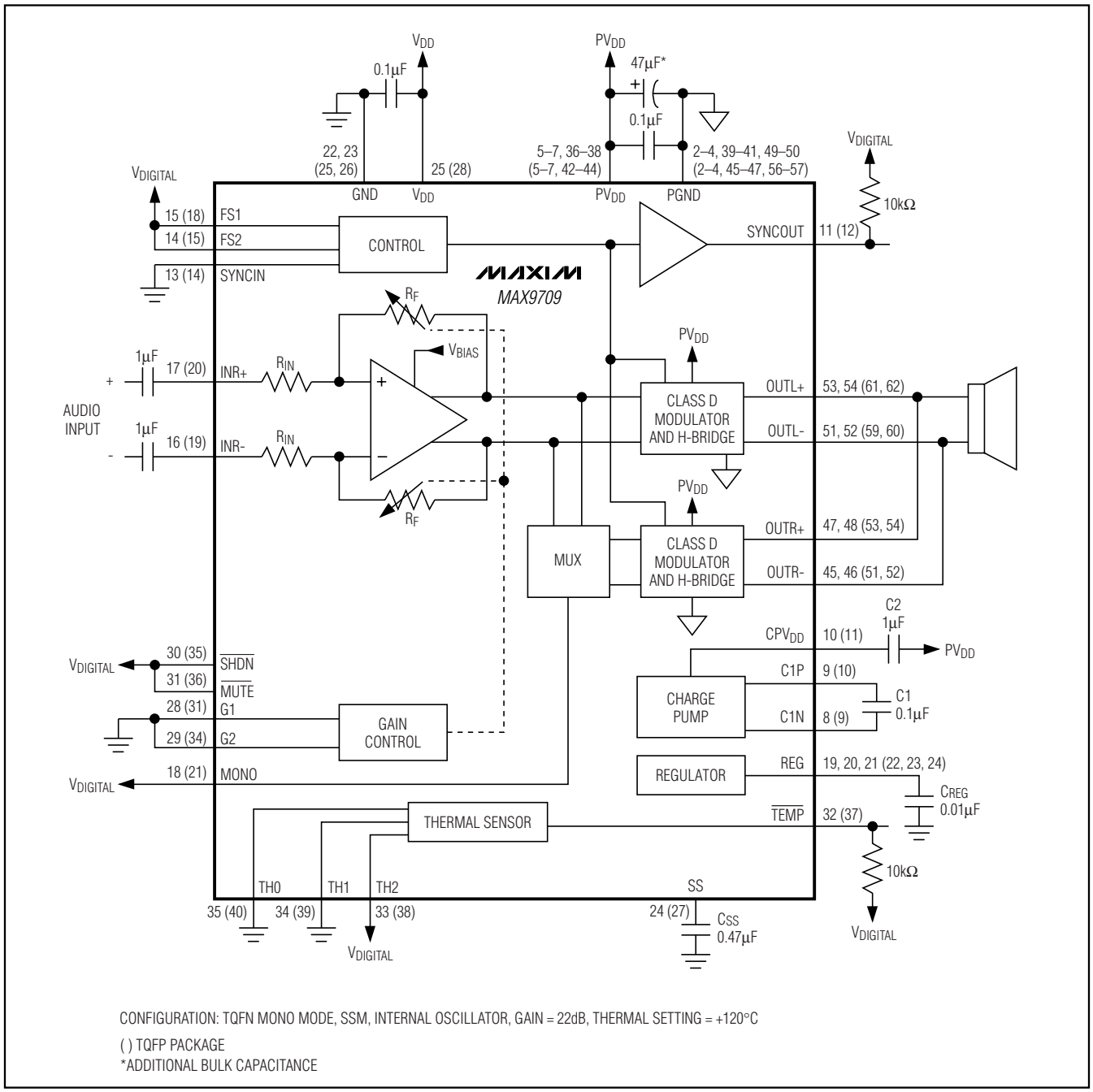
CONFIGURATION: TQFN STEREO MODE, SSM, INTERNAL OSCILLATOR, GAIN = 22dB, THERMAL SETTING = +120°C

( ) TQFP PACKAGE

*ADDITIONAL BULK CAPACITANCE

Figure 1. Typical Application and Functional Diagram in Stereo Mode

Typical Application Circuits/Functional Diagrams (continued)



CONFIGURATION: TQFN MONO MODE, SSM, INTERNAL OSCILLATOR, GAIN = 22dB, THERMAL SETTING = +120°C

( ) TQFP PACKAGE

*ADDITIONAL BULK CAPACITANCE

Figure 2. Typical Application and Functional Diagram in Mono Mode

25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

Detailed Description

The MAX9709 filterless, Class D audio power amplifier features several improvements to switch mode amplifier technology. The MAX9709 is a two-channel, stereo amplifier with 25W output power on each channel. The amplifier can be configured to output 50W output power in mono mode. The device offers Class AB performance with Class D efficiency, while occupying minimal board space. A unique filterless modulation scheme and spread-spectrum switching mode create a compact, flexible, low-noise, efficient audio power amplifier. The differential input architecture reduces common-mode noise pickup, and can be used without input-coupling capacitors. The device can also be configured as a single-ended input amplifier.

Mono/Stereo Configuration

The MAX9709 features a mono mode that allows the right and left channels to operate in parallel, achieving up to 50W of output power. The mono mode is enabled by applying logic high to MONO. In this mode, audio signal applied to the right channel (INR+/INR-) is routed to the H-bridge of both channels, while signal applied to the left channel (INL+/INL-) is ignored. OUTL+ must be connected to OUTR+ and OUTL- must be connected to OUTR- using heavy PC board traces as close to the device as possible (see Figure 2).

When the device is placed in mono mode on a PC board with outputs wired together, ensure that the MONO pin can never be driven low when the device is enabled. Driving the MONO pin low (stereo mode) while the outputs are wired together in mono mode may trigger the short-circuit or thermal protection or both, and may even damage the device.

Efficiency

Efficiency of a Class D amplifier is attributed to the region of operation of the output stage transistors. In a Class D amplifier, the output transistors act as current-steering switches and consume negligible additional power. Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent current overhead. The theoretical best efficiency of a linear amplifier is 78%; however, that efficiency is only exhibited at peak output powers. Under normal operating levels (typical music reproduction levels), efficiency falls below 30%, whereas the MAX9709 still exhibits 87% efficiency under the same conditions.

Shutdown

The MAX9709 features a shutdown mode that reduces power consumption and extends battery life. Driving $\overline{SHDN}$ low places the device in low-power (0.1µA) shutdown mode. Connect $\overline{SHDN}$ to digital high for normal operation.

Mute Function

The MAX9709 features a clickless/popless mute mode. When the device is muted, the outputs stop switching, muting the speaker. Mute only affects the output stage and does not shut down the device. To mute the MAX9709, drive $\overline{MUTE}$ to logic low. Driving $\overline{MUTE}$ low during the power-up/down or shutdown/turn-on cycle optimizes click-and-pop suppression.

Click-and-Pop Suppression

The MAX9709 features comprehensive click-and-pop suppression that eliminates audible transients on start-up and shutdown. While in shutdown, the H-bridge is pulled to GND through a 330kΩ resistor. During startup or power-up, the input amplifiers are muted and an internal loop sets the modulator bias voltages to the correct levels, preventing clicks and pops when the H-bridge is subsequently enabled. Following startup, a soft-start function gradually unmutes the input amplifiers. The value of the soft-start capacitor has an impact on the click-and-pop levels, as well as startup time.

Thermal Sensor

The MAX9709 features an on-chip temperature sensor that monitors the die temperature. When the junction temperature exceeds a programmed level, $\overline{TEMP}$ is pulled low. This flags the user to reduce power or shut down the device. $\overline{TEMP}$ may be connected to SS or $\overline{MUTE}$ for automatic shutdown during overheating. If $\overline{TEMP}$ is connected to $\overline{MUTE}$, during thermal protection mode, the audio is muted and the device is in mute mode. If $\overline{TEMP}$ is connected to SS, during thermal protection mode, the device is shut down but the thermal sensor is still active.

$\overline{TEMP}$ returns high once the junction temperature cools below the set threshold minus the thermal hysteresis. If $\overline{TEMP}$ is connected to either $\overline{MUTE}$ or SS, the audio output resumes. The temperature threshold is set by the TH0, TH1, and TH2 inputs as shown in Table 1. An RC filter may be used to eliminate any transient at the $\overline{TEMP}$ output as shown in Figure 3.

If TH2 = TH1 = TH0 = HIGH, it is likely that the MAX9709 enters thermal shutdown without tripping the thermal flag.

Gain Selection

The MAX9709 features four pin-selectable gain settings; see Table 2.

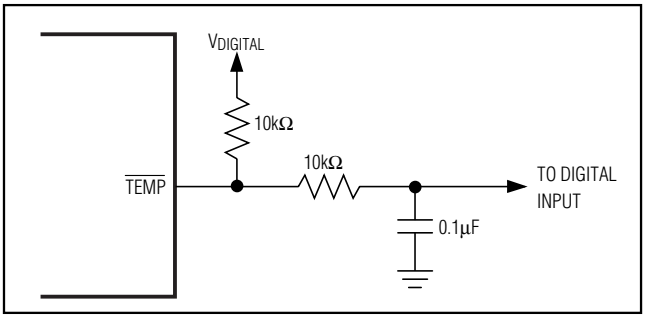


Figure 3. An RC Filter Eliminates Transient During Switching

Table 1. MAX9709 Junction Temperature Threshold Setting

JUNCTION TEMPERATURE (°C)	TH2	TH1	TH0
80	Low	Low	Low
90	Low	Low	High
100	Low	High	Low
110	Low	High	High
120	High	Low	Low
129	High	Low	High
139	High	High	Low
158	High	High	High

Table 2. MAX9709 Gain Setting

G1	G2	GAIN (dB)
Low	High	22
High	High	25
High	Low	29.5
Low	Low	36

Operating Modes

Fixed-Frequency Modulation (FFM) Mode

The MAX9709 features three switching frequencies in the FFM mode (Table 3). In this mode, the frequency spectrum of the Class D output consists of the fundamental switching frequency and its associated harmonics (see the Wideband Output Spectrum graph in the *Typical Operating Characteristics*). Select one of the three fixed switching frequencies such that the harmonics do not fall in a sensitive band. The switching frequency can be changed any time without affecting audio reproduction.

Spread-Spectrum Modulation (SSM) Mode

The MAX9709 features a unique, patented spread-spectrum (SSM) mode that flattens the wideband spectral components, improving EMI emissions that may be radiated by the speaker and cables. This mode is enabled by setting FS1 = FS2 = high. In SSM mode, the switching frequency varies randomly by ±4% around the center frequency (200kHz). The modulation scheme remains the same, but the period of the triangle waveform changes from cycle to cycle. Instead of a large amount of spectral energy present at multiples of the switching frequency, the energy is now spread over a bandwidth that increases with frequency. Above a few megahertz, the wideband spectrum looks like white noise for EMI purposes. SSM mode reduces EMI compared to fixed-frequency mode. This can also help to randomize visual artifacts caused by radiated or supply borne interference in displays.

Synchronous Switching Mode

The MAX9709 SYNCIN input allows the Class D amplifier to switch at a frequency defined by an external clock frequency. Synchronizing the amplifier with an external clock source may confine the switching frequency to a less sensitive band. The external clock frequency range is from 600kHz to 1.2MHz and can have any duty cycle, but the minimum pulse must be greater than 100ns.

SYNCOUT is an open-drain clock output for synchronizing external circuitry. Its frequency is four times the amplifier's switching frequency and it is active in either internal or external oscillator mode.

Table 3. Switching Frequencies

FS1	FS2	SYNCOUT FREQUENCY (kHz)	MODULATION
0	0	200	Fixed-frequency
0	1	250	Fixed-frequency
1	0	160	Fixed-frequency
1	1	200 ±4	Spread-spectrum

25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

Linear Regulator (REG)

The supply voltage range for the MAX9709 is from 10V to 22V to achieve high-output power. An internal linear regulator reduces this voltage to 6.3V for use with small-signal and digital circuitry that does not require high-voltage supply. Bypass a 0.01µF capacitor from REG to GND.

Applications Information

Logic Inputs

All of the digital logic inputs and output have an absolute maximum rating of +12V. If the MAX9709 is operating with a supply voltage between 10V and 12V, digital inputs can be connected to PV_{DD} or V_{DD}. If PV_{DD} and V_{DD} are greater than 12V, digital inputs and outputs must be connected to a digital system supply lower than 12V.

Input Amplifier

Differential Input

The MAX9709 features a differential input structure, making them compatible with many CODECs, and offering improved noise immunity over a single-ended input amplifier. In devices such as flat-panel displays, noisy digital signals can be picked up by the amplifier's inputs. These signals appear at the amplifiers' inputs as common-mode noise. A differential input amplifier amplifies only the difference of the two inputs, while any signal common to both inputs is attenuated.

Single-Ended Input

The MAX9709 can be configured as a single-ended input amplifier by capacitively coupling either input to GND and driving the other input (Figure 4).

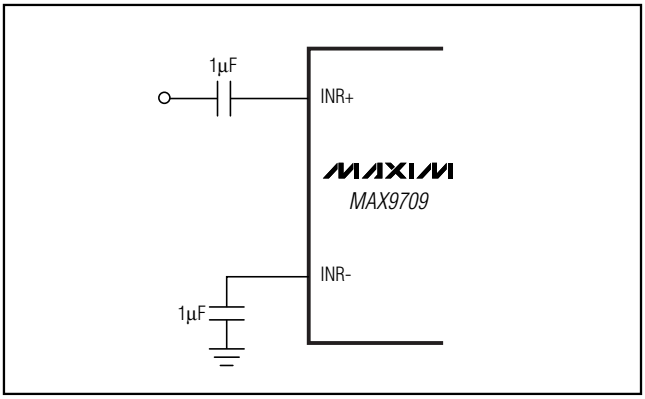


Figure 4. Single-Ended Input Connections

Component Selection

Input Filter

An input capacitor, C_{IN}, in conjunction with the input impedance of the MAX9709, forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose C_{IN} so that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the low-frequency response of the amplifier. Use capacitors with dielectrics that have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

Output Filter

The MAX9709 does not require an output filter. However, output filtering can be used if a design is failing radiated emissions due to board layout or cable length, or the circuit is near EMI-sensitive devices. See the MAX9709 evaluation kit for suggested filter topologies. The tuning and component selection of the filter should be optimized for the load. A purely resistive load (8Ω) used for lab testing requires different components than a real, complex load-speaker load.

Charge-Pump Capacitor Selection

The MAX9709 has an internal charge-pump converter that produces a voltage level for internal circuitry. It requires a flying capacitor (C1) and a holding capacitor (C2). Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range, select capacitors with an X7R dielectric. The capacitors' voltage rating must be greater than 36V.

Sharing Input Sources

In certain systems, a single audio source can be shared by multiple devices (speaker and headphone amplifiers). When sharing inputs, it is common to mute the unused device, rather than completely shutting it down. This prevents the unused device inputs from distorting the input signal. Mute the MAX9709 by driving $\overline{MUTE}$ low. Driving $\overline{MUTE}$ low turns off the Class D output stage, but does not affect the input bias levels of the MAX9709.

Frequency Synchronization

The MAX9709 outputs up to 27W on each channel in stereo mode. If higher output power or a 2.1 solution is needed, two MAX9709s can be used. Each MAX9709 is synchronized by connecting SYNCOUT from the first MAX9709 to SYNCIN of the second MAX9709 (see Figure 5).

Supply Bypassing/Layout

Proper power-supply bypassing ensures low distortion operation. For optimum performance, bypass PV_{DD} to PGND with a 0.1µF capacitor as close to each PV_{DD} pin as possible. A low-impedance, high-current power-supply connection to PV_{DD} is assumed. Additional bulk capacitance should be added, as required, depending on the application and power-supply characteristics. GND and PGND should be star-connected to system ground. For the TQFN package, solder the exposed paddle (EP) to the ground plane using multiple-plated through-hole vias. The exposed paddle must be soldered to the ground plane for rated power dissipation and good ground return. Use wider PC board traces to lower the parasitic resistance for the high-power output pins (OUTR+, OUTR-, OUTL+, OUTL-). Refer to the MAX9709 evaluation kit for layout guidance.

Thermal Considerations

Class D amplifiers provide much better efficiency and thermal performance than a comparable Class AB amplifier. However, the system's thermal performance must be considered with realistic expectations along with its many parameters.

Continuous Sine Wave vs. Music

When a Class D amplifier is evaluated in the lab, often a continuous sine wave is used as the signal source. While this is convenient for measurement purposes, it represents a worst-case scenario for thermal loading on the amplifier. It is not uncommon for a Class D amplifier to enter thermal shutdown if driven near maximum output power with a continuous sine wave. The PC board must be optimized for best dissipation (see the *PC Board Thermal Considerations* section).

Audio content, both music and voice, has a much lower RMS value relative to its peak output power. Therefore, while an audio signal may reach similar peaks as a continuous sine wave, the actual thermal impact on the Class D amplifier is highly reduced. If the thermal performance of a system is being evaluated, it is important to use actual audio signals instead of sine waves for testing. If sine waves must be used, the thermal performance is less than the system's actual capability for real music or voice.

PC Board Thermal Considerations

The exposed pad is the primary route for conducting heat away from the IC. With a bottom-side exposed pad, the PC board and its copper becomes the primary heatsink for the Class D amplifier. Solder the exposed pad to a copper polygon. Add as much copper as possible from this polygon to any adjacent pin on the Class D amplifier as well as to any adjacent components, provided these connections are at the same potential. These copper paths must be as wide as possible. Each of these paths contributes to the overall thermal capabilities of the system.

The copper polygon to which the exposed pad is attached should have multiple vias to the opposite side of the PC board, where they connect to another copper polygon. Make this polygon as large as possible within the system's constraints for signal routing.

Additional improvements are possible if all the traces from the device are made as wide as possible. Although the IC pins are not the primary thermal path out of the package, they do provide a small amount. The total improvement would not exceed about 10%, but it could make the difference between acceptable performance and thermal problems.

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Auxiliary Heatsinking

If operating in higher ambient temperatures, it is possible to improve the thermal performance of a PC board with the addition of an external heatsink. The thermal resistance to this heatsink must be kept as low as possible to maximize its performance. With a bottom-side exposed pad, the lowest resistance thermal path is on the bottom of the PC board. The topside of the IC is not a significant thermal path for the device, and therefore is not a cost-effective location for a heatsink. If an LC filter is used in the design, placing the inductor in close proximity to the IC can help draw heat away from the MAX9709.

Thermal Calculations

The die temperature of a Class D amplifier can be estimated with some basic calculations. For example, the die temperature is calculated for the below conditions:

- T_A = +40°C
- P_{OUT} = 16W
- Efficiency (η) = 87%
- θ_{JA} = 21°C/W

First, the Class D amplifier's power dissipation must be calculated:

$$P_{DISS} = \frac{P_{OUT}}{\eta} - P_{OUT} = \frac{16W}{0.87} - 16W = 2.4W$$

Then the power dissipation is used to calculate the die temperature, T_C, as follows:

$$T_C = T_A + P_{DISS} \times \theta_{JA} = 40°C + 24W \times 21°C/W = 90.4°C$$

Load Impedance

The on-resistance of the MOSFET output stage in Class D amplifiers affects both the efficiency and the peak-current capability. Reducing the peak current into the load reduces the I^2R losses in the MOSFETs, which increases efficiency. To keep the peak currents lower, choose the highest impedance speaker which can still deliver the desired output power within the voltage swing limits of the Class D amplifier and its supply voltage.

Another consideration is the load impedance across the audio frequency band. A loudspeaker is a complex electromechanical system with a variety of resonance. In other words, an 8Ω speaker usually has 8Ω impedance within a very narrow range. This often extends well below 8Ω, reducing the thermal efficiency below what is expected. This lower-than-expected impedance can be further reduced when a crossover network is used in a multidriver audio system.

Systems Application Circuit

The MAX9709 can be configured into multiple amplifier systems. One concept is a 2.1 audio system (Figure 5) where a stereo audio source is split into three channels. The left- and right-channel inputs are highpass filtered to remove the bass content, and then amplified by the MAX9709 in stereo mode. Also, the left- and right-channel inputs are summed together and lowpass filtered to remove the high-frequency content, then amplified by a second MAX9709 in mono mode.

The conceptual drawing of Figure 5 can be applied to either single-ended or differential systems. Figure 6 illustrates the circuitry required to implement a fully differential filtering system. By maintaining a fully differential path, the signal-to-noise ratio remains uncompromised and noise pickup is kept very low. However, keeping a fully differential signal path results in almost twice the component count, and therefore performance must be weighed against cost and size.

The highpass and lowpass filters should have different cutoff frequencies to ensure an equal power response at the crossover frequency. The filters should be at -6dB amplitude at the crossover frequency, which is known as a Linkwitz-Riley alignment. In the example circuit of Figure 6, the -3dB cutoff frequency for the highpass filters is 250Hz, and the -3dB cutoff frequency for the lowpass filter is 160Hz. Both the highpass filters and the lowpass filters are at a -6dB amplitude at approximately 200Hz. If the filters were to have the same -3dB cutoff frequency, a measurement of sound pressure level (SPL) vs. frequency would have a peak at the crossover frequency.

The circuit in Figure 6 uses inverting amplifiers for their ease in biasing. Note the phase labeling at the outputs has been reversed. The resistors should be 1% or better in tolerance and the capacitors 5% tolerance or better. Mismatch in the components can cause discrepancies between the nominal transfer function and actual performance. Also, the mismatch of the input resistors (R15, R17, R19, and R21 in Figure 6) of the summing amplifier and lowpass filter causes some high-frequency sound to be sent to the subwoofer.

The circuit in Figure 6 drives a pair of MAX9709 devices similar to the circuit in Figure 5. The inputs to the MAX9709 still require AC-coupling to prevent compromising the click-and-pop performance of the MAX9709.

The left and right drivers should be at an 8Ω to 12Ω impedance, whereas the subwoofer can be 4Ω to 8Ω depending on the desired output power, the available power-supply voltage, and the sensitivity of the individual speakers in the system. The four gain settings of the MAX9709 allow gain adjustments to match the sensitivity of the speakers.

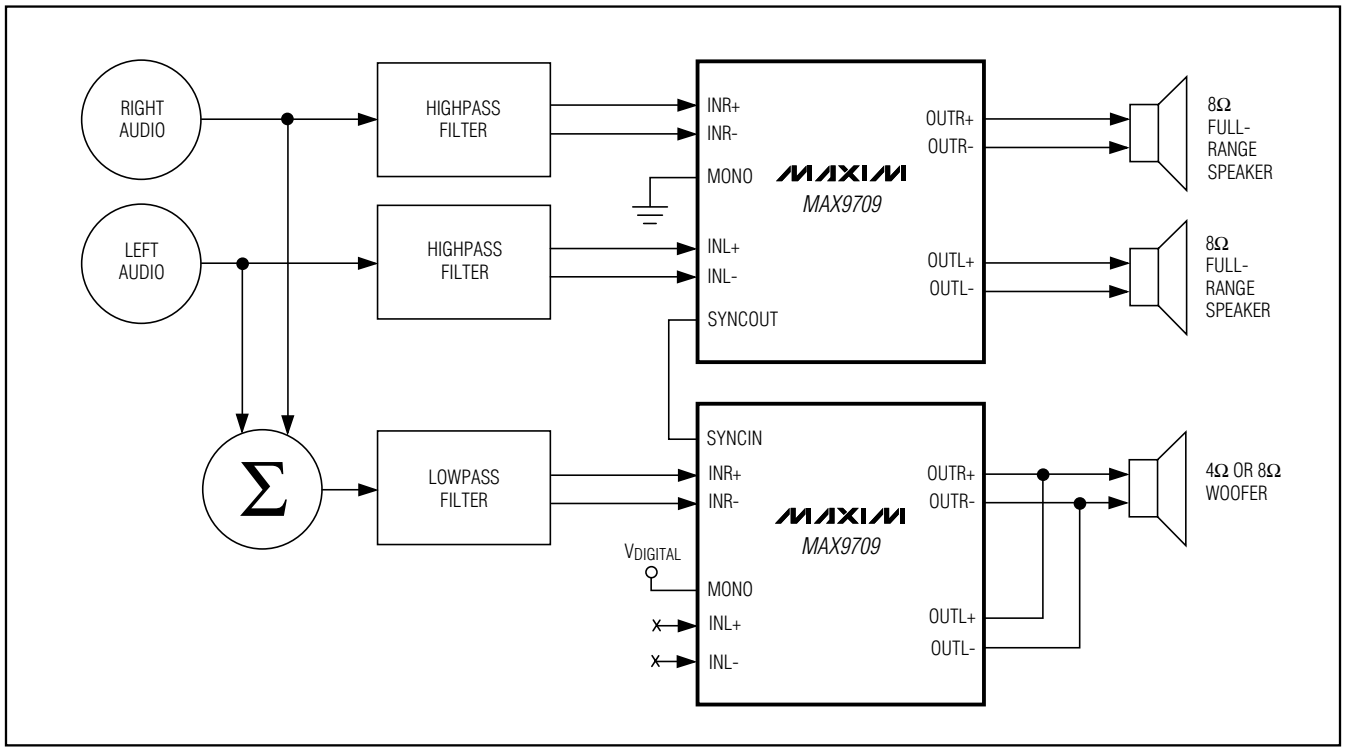


Figure 5. Multiple Amplifiers Implement a 2.1 Audio System

25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

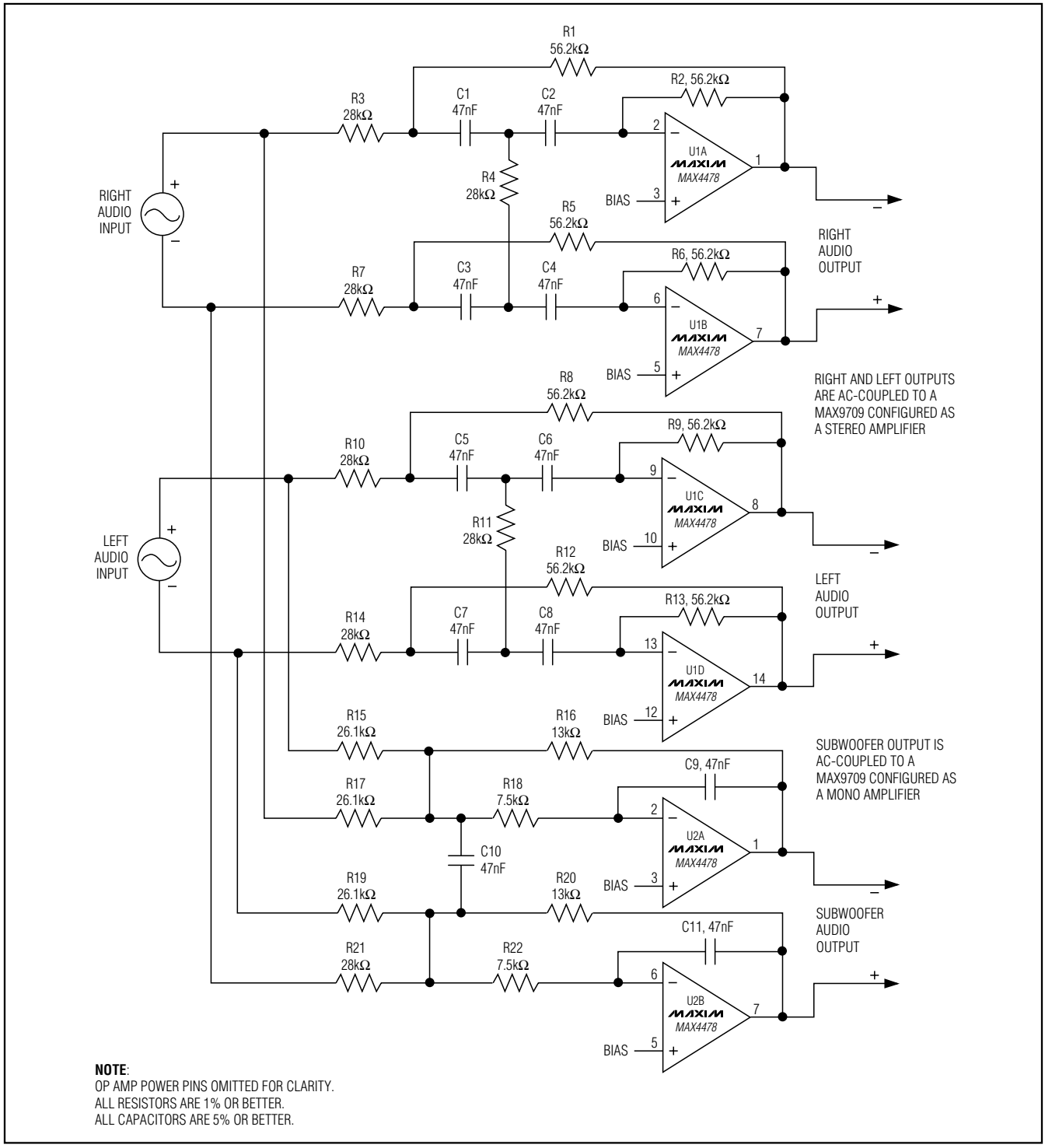
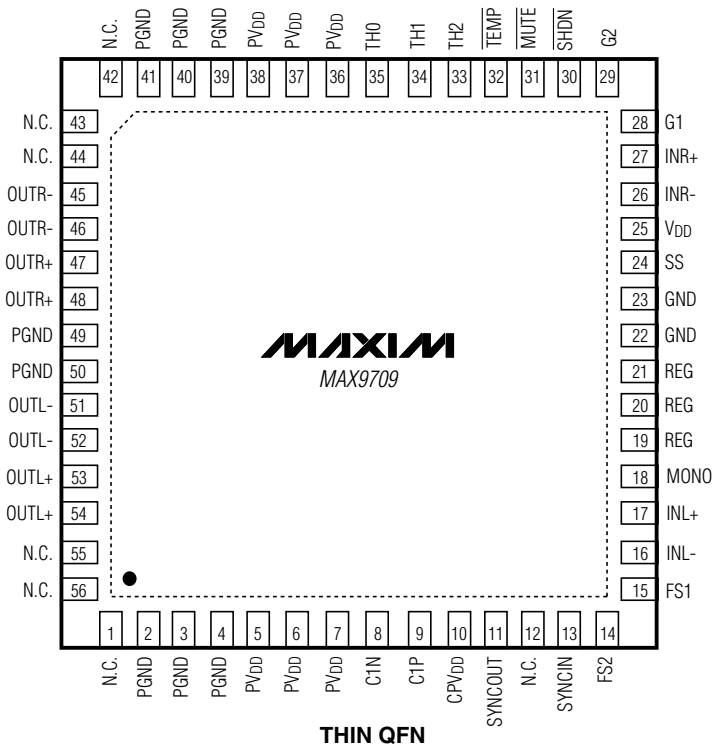


Figure 6. Fully Differential Crossover Filters

Pin Configurations

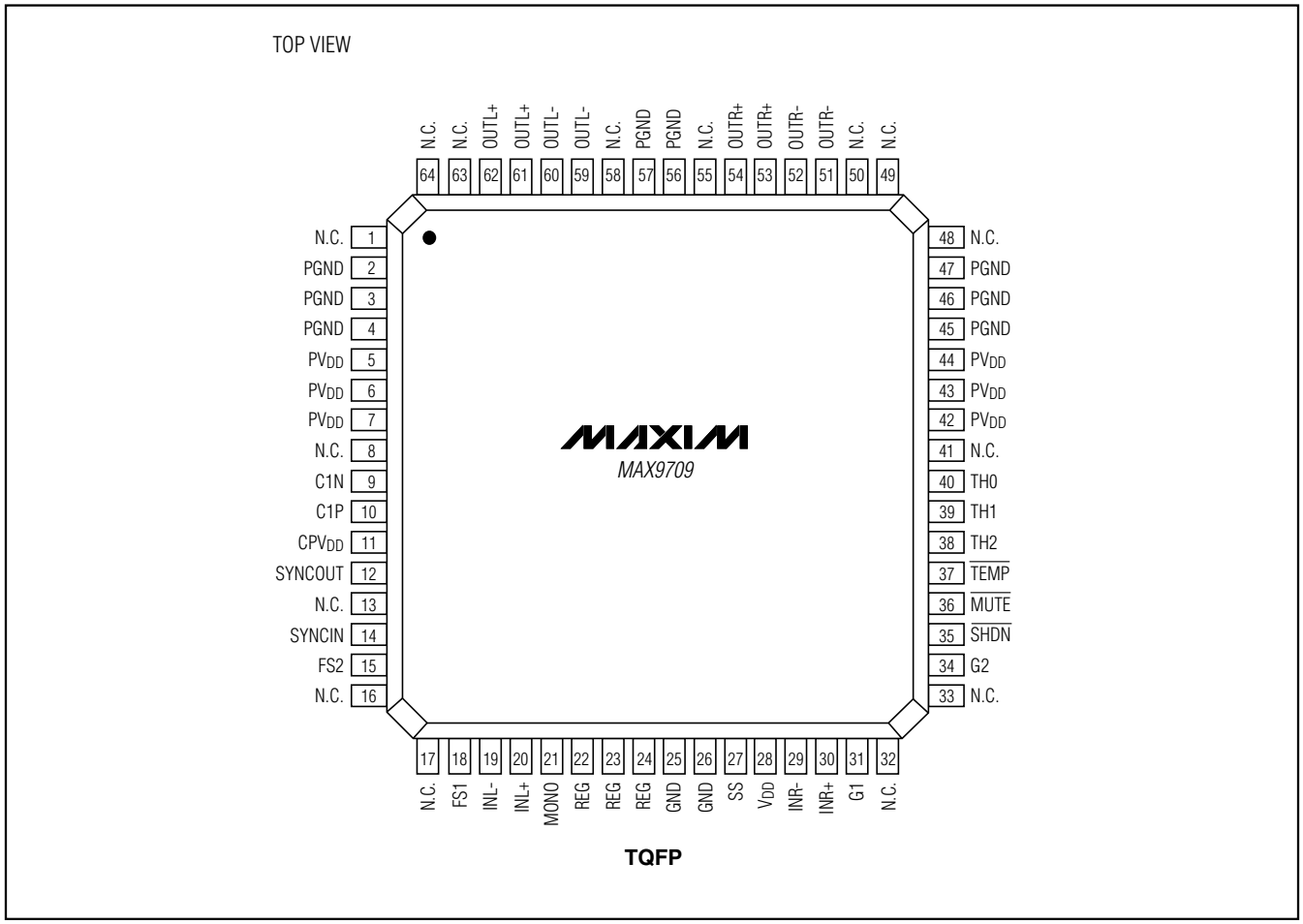
TOP VIEW



THIN QFN

25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

Pin Configurations (continued)



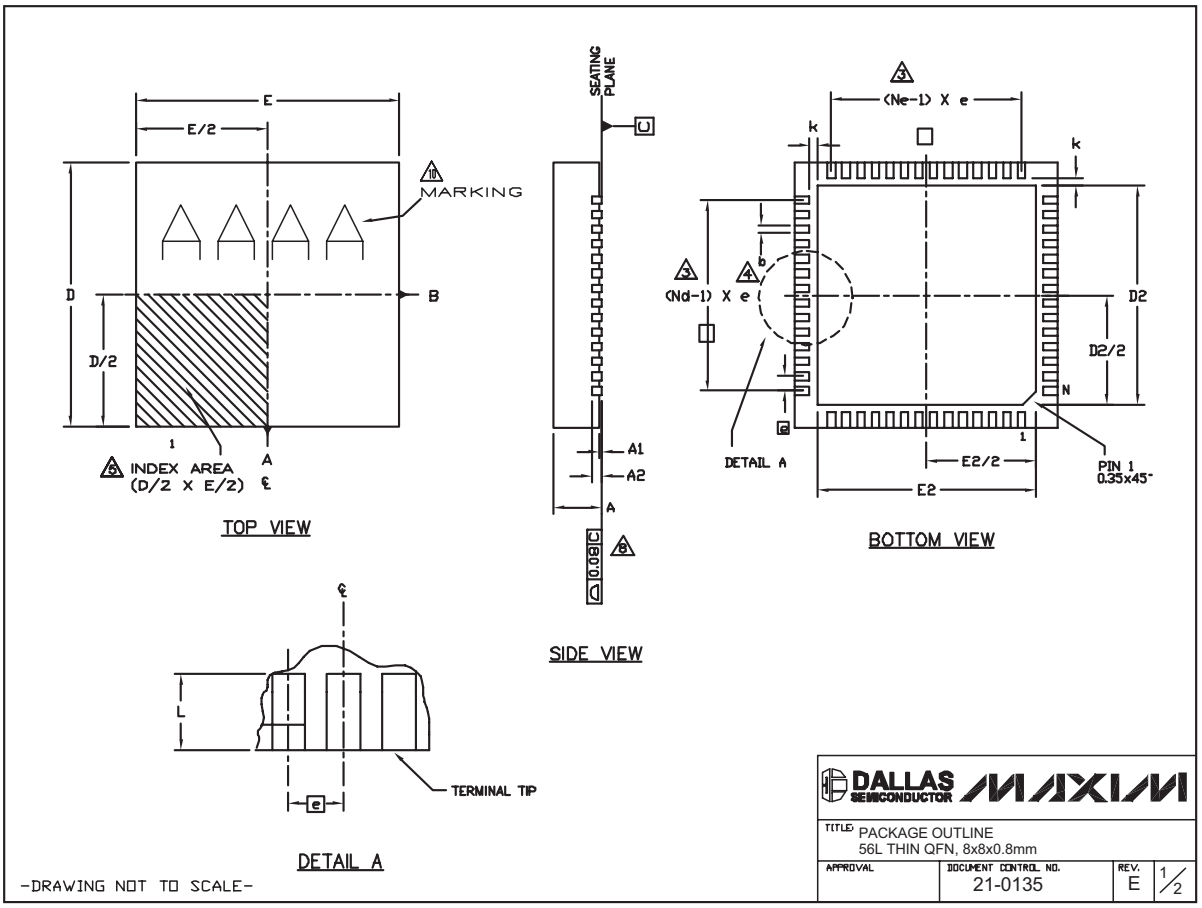
Chip Information

PROCESS: BiCMOS

25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.225mm MAXIMUM (0.009 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE WITHIN HATCHED AREA AS SHOWN.
   EITHER AN INDENTATION MARK OR INK/LASER MARK IS ACCEPTABLE.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. PACKAGE WARPAGE MAX 0.01mm.
8. APPLIES TO EXPOSED PAD AND TERMINALS.
   EXCLUDES INTERNAL DIMENSION OF EXPOSED PAD.
9. MEETS JEDEC MO220.
10. MARKING IS FOR PACKAG ORIENTATION REFERENCE ONLY
11. NUMBER OF LEADS ARE FOR REFERENCE ONLY

SYMBOL	56L 8x8			NOTE
	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	
b	0.20	0.25	0.30	4
D	7.90	8.00	8.10	
E	7.90	8.00	8.10	
e	0.50 BSC			
N	56			3
Nd	14			3
Ne	14			3
L	0.30	0.40	0.50	
A1	0.00	0.02	0.05	
A2	0.20 REF			
k	0.25	--	--	

PKG. CODE	EXPOSED PAD VARIATION						JEDEC	DOWN BONDS ALLOWED
	D2			E2				
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T5688-2	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	YES
T5688-3	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	NO

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

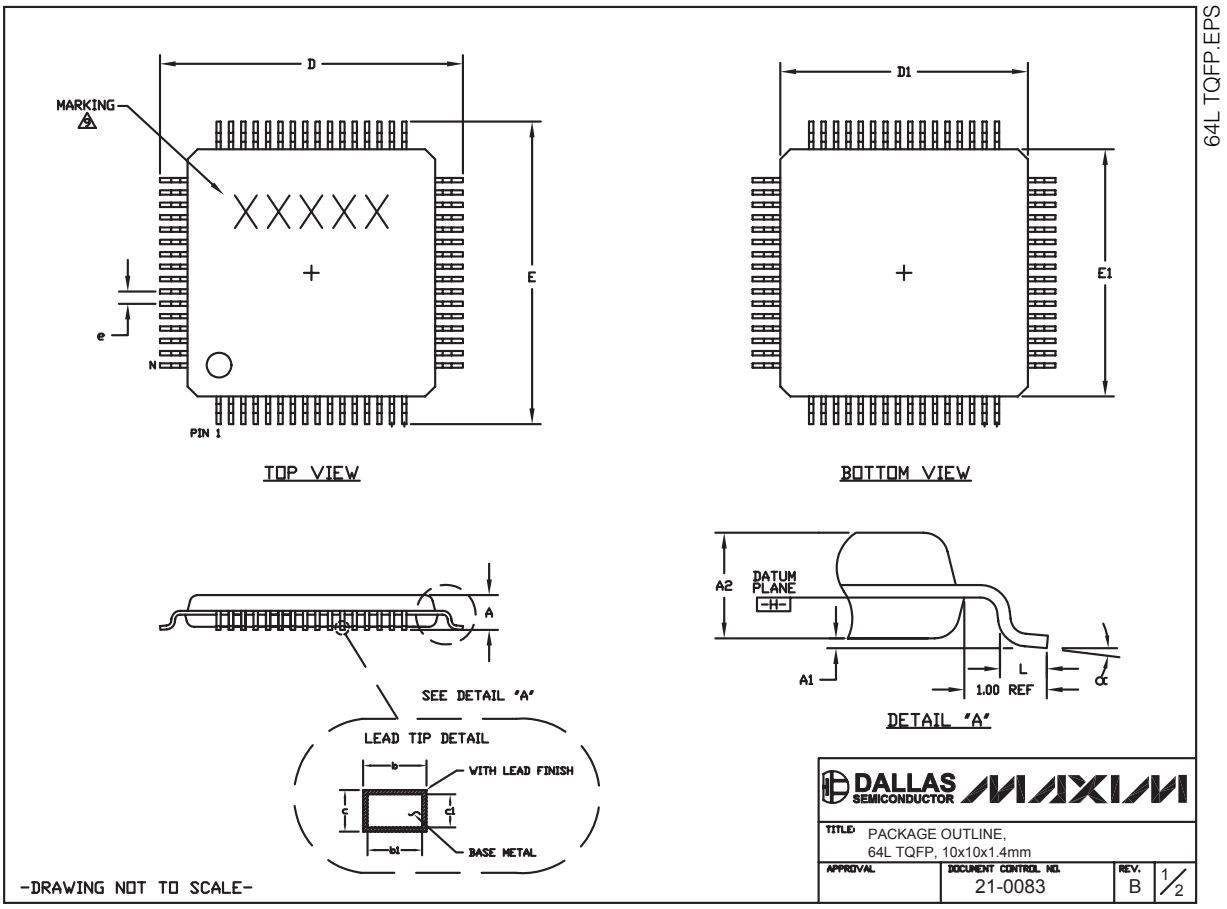
TITLE: PACKAGE OUTLINE
56L THIN QFN, 8x8x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0135	E	2/2

25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



25W/50W, Filterless, Spread-Spectrum, Stereo/Mono, Class D Amplifier

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟H⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026, VARIATION BCD.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

JEDEC VARIATION		
	BCD	
	64 LEAD	
	MIN.	MAX.
A	---	1.60
A_1	0.05	0.15
A_2	1.35	1.45
D	11.80	12.20
D_1	9.80	10.20
E	11.80	12.20
E_1	9.80	10.20
e	0.50 BSC.	
L	0.45	0.75
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
α	0°	7°

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 64L TQFP, 10x10x1.4mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0083	B	2/2