FUJITSU

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ASSP
Dual Serial Input PLL Frequency Synthesizer(Small Package)

MB15F74UV

■ DESCRIPTION

The Fujitsu MB15F74UV is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 4000MHz and a 2000MHz prescalers. A 64/65 or a 128/129 for the 4000MHz prescaler, and a 32/33 or a 64/65 for the 2000MHz prescaler can be selected for the prescaler that enables pulse swallow operation.

The latest BiCMOS process is used, as a result a supply current is typically 9.0mA typ. at 3.0V. The supply voltage range is from 2.7V to 3.6V. A refined charge pump supplies well-balanced output current with 1.5mA and 6mA selectable by serial data. The data format and the function as fast locking are same as the previous one MB15F74UL.

The new package(BCC18) decreases a mount area of MB15F74UV about 50% comparing with the former BCC20(for dual PLL, MB15F74UL).

MB15F74UV is ideally suited for wireless mobile communications, such as W-CDMA.

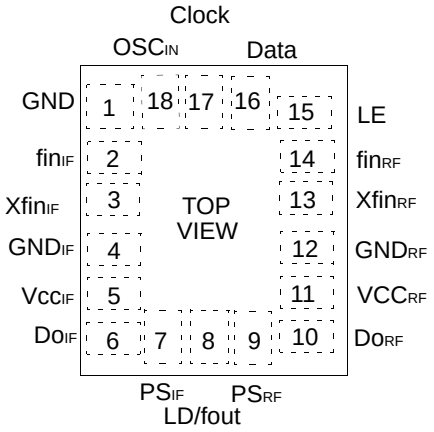
■ FEATURES

- Very small package: BCC18 (2.4*2.7*0.45mm)
- High frequency operation: RF synthesizer : 4000MHz max
  IF synthesizer : 2000MHz max
- Low power supply voltage: V_{CC} = 2.7 to 3.6 V
- Ultra Low power supply current : I_{CC} = 9.0 mA typ. (V_{CC} = 3.0V, Ta=25°C, SW=0 in RF, IF locking state)
- Direct power saving function : Power supply current in power saving mode
  Typ. 0.1 μA(Vcc=3.0V, Ta=25°C), Max. 10 μA(Vcc=3.0V)
- Dual modulus prescaler : 4000MHz prescaler(64/65 or 128/129) / 2000MHz prescaler(32/33 or 64/65)
- Serial input 14-bit programmable reference divider: R = 3 to 16,383
- Serial input programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 3 to 2,047
- On-chip phase comparator for fast lock and low noise
- On-chip phase control for phase comparator
- Operating temperature: Ta = –40 to 85°C
- Sireal data format compatible with MB15F74UL

18-pad, Plastic BCC

(LCC-18P-M05)

■ PIN ASSIGNMENT

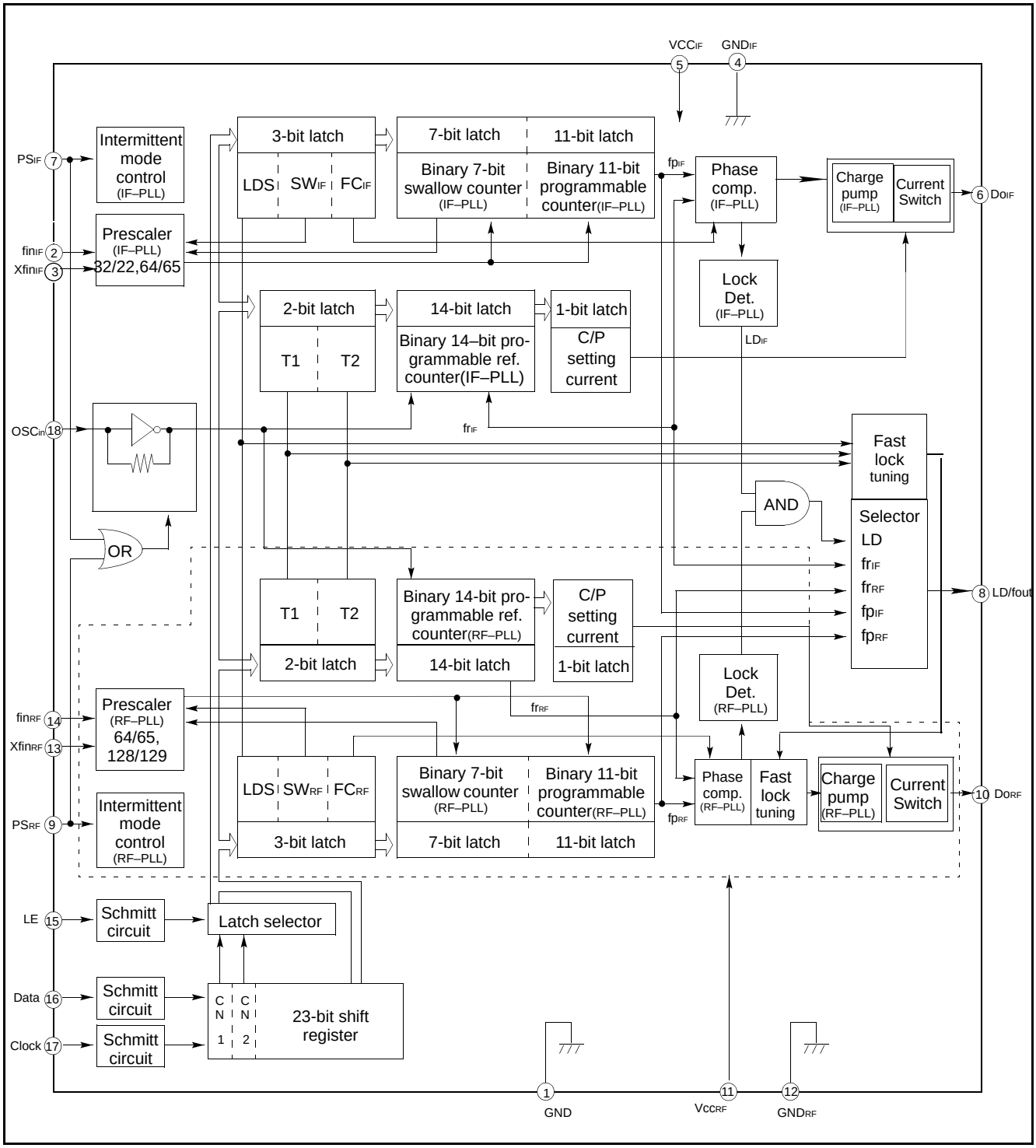


LCC-18P-M05

■ PIN DESCRIPTIONS

Pin No.	Pin name	I/O	Descriptions
1	GND	-	Ground for OSC input buffer and the shift registor circuit.
2	fin_{IF}	I	Prescaler input pin for the IF-PLL section. Connection to an external VCO should be AC coupling.
3	$Xfin_{IF}$	I	Prescaler complimentary input for the IF-PLL section. This pin should be grounded via a capacitor.
4	GND_{IF}	-	Ground for the IF-PLL section.
5	Vcc_{IF}	-	Power supply voltage input pin for the IF-PLL section(except for the charge pump circuit), the shift register and the oscillator input buffer. When power is OFF, latched data of IF-PLL is lost.
6	Do_{IF}	O	Charge pump output for the IF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
7	PS_{IF}	I	Power saving mode control for the IF-PLL section. This pin must be set at ”L” Power-ON. (Open is prohibited.) PS_{IF} = ”H” ; Normal mode PS_{IF} = ”L” ; Power saving mode
8	LD/fout	O	Lock detect signal output(LD)/ phase comparator monitoring outut (fout). The output signal is selected by a LDS bit in a serial data. LDS bit = "1" ; outputs fout signal LDS bit = "0" ; outputs LD sihnal
9	PS_{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at ”L” Power-ON. (Open is prohibited.) PS_{RF} = ”H” ; Normal mode PS_{RF} = ”L” ; Power saving mode
10	Do_{RF}	O	Charge pump output for the RF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
11	Vcc_{RF}	-	Power supply voltage input pin for the RF-PLL section(except for the charge pump circuit).
12	GND_{RF}	-	Ground for the RF-PLL section.
13	$Xfin_{RF}$	I	Prescaler complimentary input for the RF-PLL section. This pin should be grounded via a capacitor.
14	fin_{RF}	I	Prescaler input pin for the RF-PLL. Connction to an external VCO should be AC coupling.
15	LE	I	Load enable signal input (with the schmitt trigger circuit.) When LE is set "H", data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
16	Data	I	Serial data input (with the schmitt trigger circuit.) A data is transferred to the corresponding latch (IF-ref counter, IF-prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
17	Clock	I	Clock input for the 23-bit shift register (with the schmitt trigger circuit.) One bit data is shifted into the shift register on a rising edge of the clock.
18	OSC_{IN}	I	The programmable reference divider input. TCXO should be connected with a AC coupling capacitor.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	–0.5 to +4.0	V	
Input voltage	V_I	–0.5 to V_{CC} +0.5	V	
Output voltage	V_O	GND to V_{CC}	V	LD/fout
	V_{DO}	GND to V_{CC}	V	Do
Storage temperature	T_{stg}	–55 to +125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	$V_{CCRF} = V_{CCIF}$
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	T_a	–40	–	+85	°C	

Handling Precautions

(1) V_{CCRF} and,V_{CCIF} must supply equal voltage.
Even if either RF-PLL or IF-PLL is not used, power must be supplied to both V_{CCRF} and V_{CCIF} to keep them equal. It is recommended that the non-use PLL is controlled by power saving function.

(2) To protect against damage by electrostatic discharge, note the following handling precautions:
-Store and transport devices in conductive containers.
-Use properly grounded workstations, tools, and equipment.
-Turn off power before inserting or removing this device into or from a socket.
-Protect leads with conductive sheet, when transporting a board mounted device.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 to 3.6 V, Ta = –40 to +85°C)

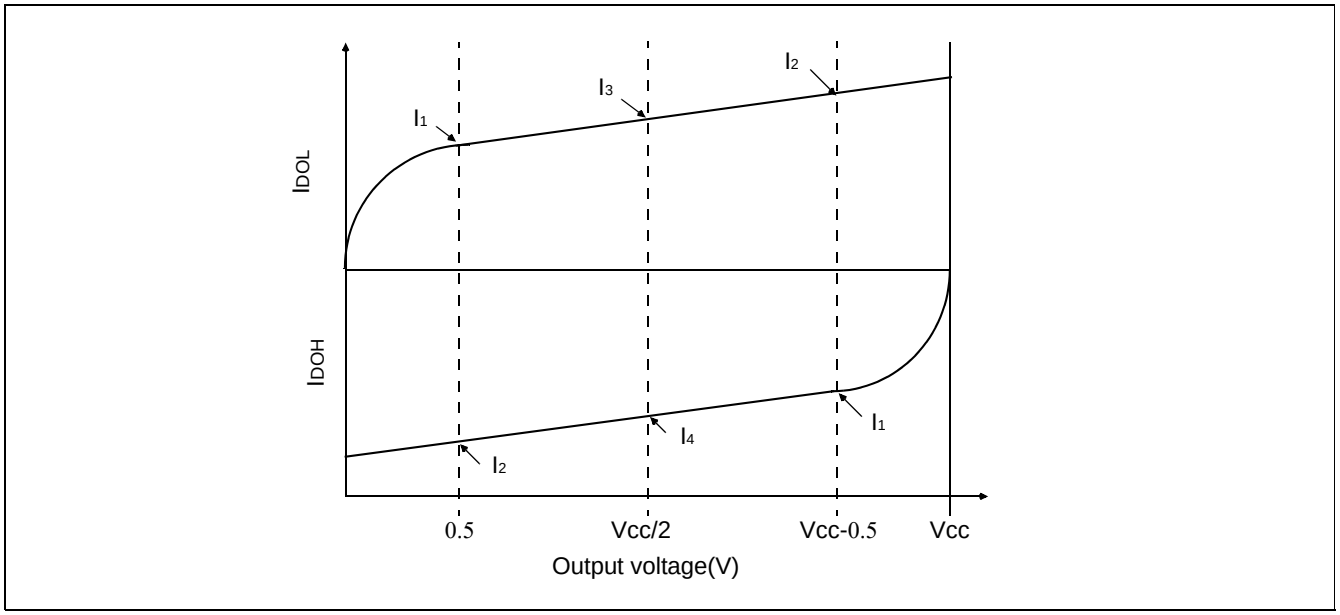
Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current*1		I_{CCIF}	fin_{IF}=2000MHz Vcc_{IF}=3.0V	2.1	2.5	3.2	mA
		I_{CCRF}	fin_{RF}=2500MHz Vcc_{RF}=3.0V	5.7	6.5	8.4	mA
Power saving current*9		I_{PSIF}	PS_{IF}=PS_{RF}= ”L”	–	0.1*2	10	μA
		I_{PSRF}	PS_{IF}=PS_{RF}= ”L”	–	0.1*2	10	μA
Operating frequency	fin_{IF}*3	fin_{IF}	IF PLL	200	–	2000	MHz
	fin_{RF}*3	fin_{RF}	RF PLL	2000	–	4000	MHz
	OSC_{IN}	fosc	–	3	–	40	MHz
Input sensitivity	fin_{IF}	$Pfin_{IF}$	IF PLL, 50 Ω system	-15	–	+2	dBm
	fin_{RF}	$Pfin_{RF}$	RF PLL, 50 Ω system	-10	–	+2	dBm
	OSC_{IN}	V_{OSC}	–	0.5	–	1.5	Vp-p
"H" level Input voltage	Data, Clock, LE	V_{IH}	Schmitt trigger input	Vcc × 0.7+0.4	–	–	V
"L" level Input voltage		V_{IL}	Schmitt trigger input	–	–	Vcc× 0.3-0.4	
"H" level Input voltage	PS	V_{IH}	–	Vcc× 0.7	–	–	V
"L" level Input voltage		V_{IL}	–	–	–	Vcc× 0.3	
"H" level Input current	Data, Clock, LE, PS	I_{IH}*4	–	–1.0	–	+1.0	μA
"L" level Input current		I_{IL}*4	–	–1.0	–	+1.0	
"H" level output voltage	LD/fout	V_{OH}	V_{CC}=2.7V, I_{OH}=–1mA	Vcc – 0.4	–	–	V
"L" level output voltage		V_{OL}	V_{CC}=2.7V, I_{OL}=1mA	–	–	0.4	
"H" level output voltage	Do_{IF} Do_{RF}	V_{DOH}	V_{CC}=2.7V, I_{DOH}=-0.5mA	Vcc – 0.4	–	–	V
"L" level output voltage		V_{DOL}	V_{CC}=2.7V, I_{DOL}=0.5mA	–	–	0.4	
High impedance cutoff current	Do_{IF} Do_{RF}	I_{OFF}	V_{CC}=2.7V, V_{OFF}=0.5V to V_p–0.5V	–	–	2.5	nA
"H"level Output current	LD/fout	I_{OH}*4	V_{CC} = 2.7V	–	–	-1.0	mA
"L" level Output current		I_{DOL}	V_{CC} = 2.7V	1.0	–	–	

(Continued)

(V_{CC} = 2.4 to 3.6 V, Ta = –40 to +85°C)

Parameter		Symbol	Condition		Value			Unit
					Min.	Typ.	Max.	
"H"level Output current	DO_{TX}*8 DO_{RX}	I_{DOH}*4	V_{CC}=2.7 V V_{DOH}=V_{CC} /2 Ta= 25°C	CS bit ="1"	-8.2	-6.0	-4.1	mA
				CS bit ="0"	-2.2	-1.5	-0.8	
"L" level Output current		I_{DOL}	V_{CC}=2.7 V V_{DOL}=V_{CC}/2 Ta= 25°C	CS bit ="1"	4.1	6.0	8.2	
				CS bit ="0"	0.8	1.5	2.2	
Charge pump current rate	I_{DOL}/I_{DOH}	I_{DOMT}*5	V_{DO}=V_{CC}/2		–	3	–	%
	vs V_{DO}	I_{DOVD}*6	0.5V ≤ V_{DO} ≤ V_{CC}-0.5V		–	10	–	%
	vs Ta	I_{DOTA}*7	-40°C ≤ Ta ≤ 85 °C, V_{DO}=V_{CC}/2		–	5	–	%

*1: Conditions; fosc=12.8MHz, Ta = 25°C, SW="L" in locking state.
*2: Vcc=2.7V, fosc=12.8MHz, Ta = 25°C, in power saving mode.
*3: AC coupling. 1000pF capacitor is connected under the condition of min. operating frequency.
*4: The symbol "-"(minus) means direction of current flow.
*5: Vcc=3.0V, Ta=25°C $(||I_3| - |I_4||) / [(|I_3| + |I_4|)/2]$ x 100(%)
*6: Vcc=3.0V, Ta=25°C $[(||I_2| - |I_1||) /2] / [(|I_1| + |I_2|)/2]$ x 100(%) (Applied to each I_{DOL}, I_{DOH})
*7: Vcc=3.0V, $[(||I_{DO(85C)}| - |I_{DO(-40C)}||) /2] / [(|I_{DO(85C)}| + |I_{DO(-40C)}|) /2]$ x 100(%) (Applied to each I_{DOL}, I_{DOH})
*8: When Charge pump current is measured, set LDS="0", T1="0" and T2="1".
*9: PS_{IF}=PS_{RF}=GND (VIL=GND and VIH=Vcc for Clock, Data, LE)



■ FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(P \times N) + A\} \times f_{OSC} \div R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
P: Preset divide ratio of dual modulus prescaler (32 or 64 for IF-PLL, 64 or 128 for RF-PLL)
N: Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, condition;$A < N$)
f_{OSC}: Reference oscillation frequency
R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections, programmable reference dividers of IF/RF-PLL sections are controlled individually.
Serial data of binary data is entered through Data pin.
On a rising edge of clock, one bit of serial data is transferred into the shift register. On a rising edge of load enable signal , the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Table1. Control Bit

Control bit		Destination of serial data
CN1	CN2	
0	0	The programmable reference counter for the IF-PLL.
1	0	The programmable reference counter for the RF-PLL.
0	1	The programmable counter and the swallow counter for the IF-PLL
1	1	The programmable counter and the swallow counter for the RF-PLL

Shift Register Configuration

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	T1	T2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	CS	X	X	X	X

CN1, 2 : Control bit [Table. 1]
R1 to R14 : Divide ratio setting bits for the programmable reference counter (3 to 16,383) [Table. 2]
T1, 2 : LD/fout output setting bit [Table. 3]
CS : Charge pump current select bit [Table. 8]
X : Dummy bits(Set "0" or "1")
NOTE: Data input with MSB first.

Programmable Counter

LSB ← Data Flow → MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	LDS	$SW_{IF/RF}$	$FC_{IF/RF}$	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CN1, 2 : Control bit [Table. 1]
N1 to N11 : Divide ratio setting bits for the programmable counter (3 to 2,047) [Table. 4]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table. 5]
$SW_{IF/RF}$: Divide ratio setting bit for the prescaler (32/33 or 64/65 for the SW_{IF}, 64/65 or 128/129 for the SW_{RF}) [Table. 6]
$FC_{IF/RF}$: Phase control bit for the phase detector(IF : FC_{IF}, RF : FC_{RF}) [Table. 7]
LDS : LD/fout signal select bit [Table. 3]

NOTE: Data input with MSB first.

Table2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio (R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 3 is prohibited.

Table.3 LD/fout output Selectable Bit Setting

LD/fout pin state		LDS	T1	T2
LD output		0	0	0
		0	1	0
		0	1	1
fout output	fr_{IF}	1	0	0
	fr_{RF}	1	1	0
	fp_{IF}	1	0	1
	fp_{RF}	1	1	1

Table.4 Binary 11-bit Programmable Counter Data Setting

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 3 is prohibited.

Table.5 Binary 7-bit Swallow Counter Data Setting

Divide ratio (N)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: • Divide ratio (A) range = 0 to 127

Table. 6 Prescaler Data Setting

		SW = ”1”	SW = ”0”
Prescaler divide ratio	**IF-PLL**	32/33	64/65
	RF-PLL	64/65	128/129

Table. 7 Phase Comparator Phase Switching Data Setting

	$FC_{IF,RF}$ = 1	$FC_{IF,RF}$ = 0
	$DO_{IF,RF}$	
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO polarity	1	2

Note: • Z = High–impedance
• Depending upon the VCO and LPF polarity, FC bit should be set.

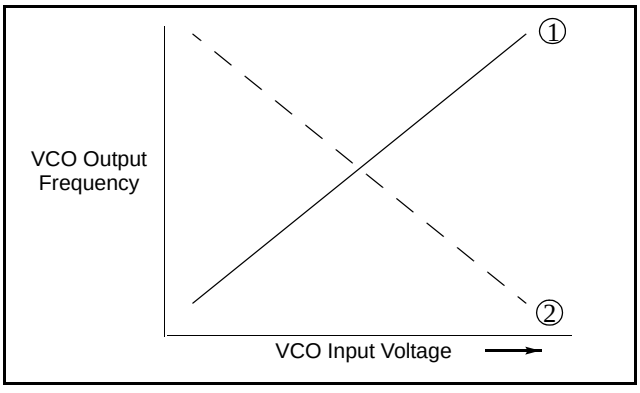


Table. 8 Charge Pump Current Setting

CS	Current value
1	± 6.0 mA
0	± 1.5 mA

4. Power Saving Mode (Intermittent Mode Control Circuit)

Table 9. PS Pin Setting

PS pin	Status
H	Normal mode
L	Power saving mode

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

For the single PLL, the lock detector, LD, remains high, indicating a locked condition.

For the dual PLL, the lock detector, LD, is as shown in the LD Output Logic table.

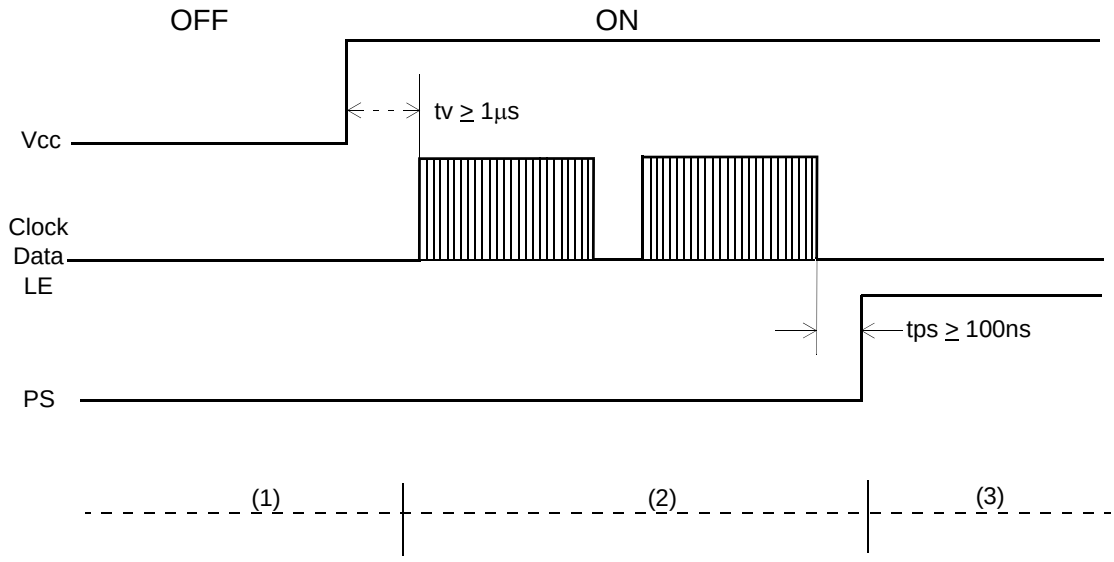
Setting the PS pin high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (fp) and the reference frequency (fr) which can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lockup time.

To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

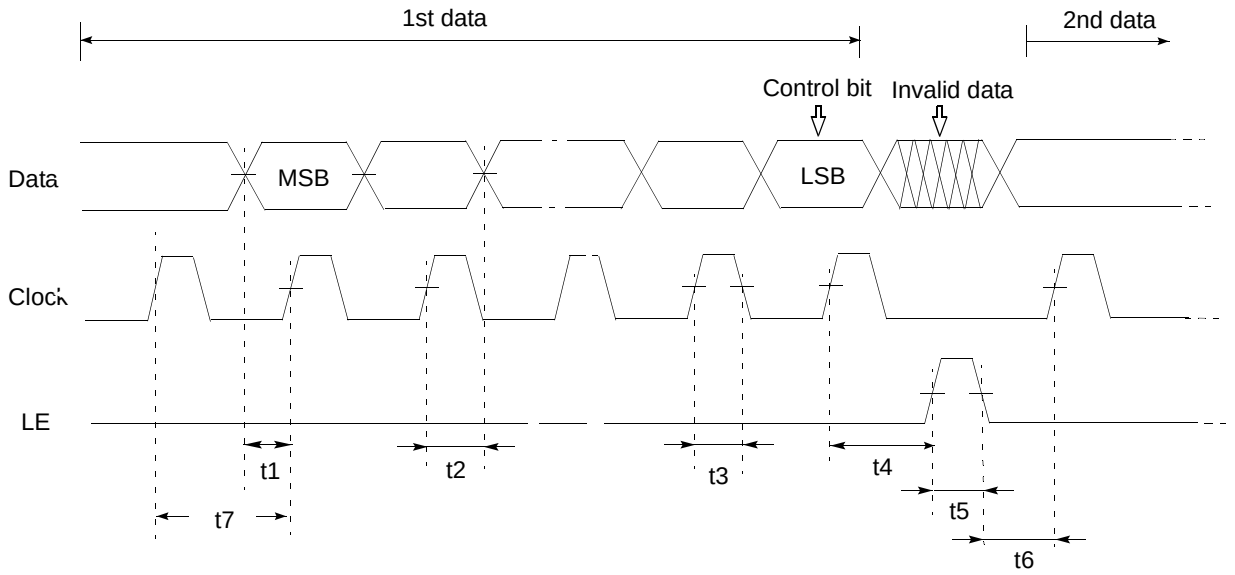
Note: When power (V_{CC}) is first applied, the device must be in standby mode.

Note: • PS pin must be set at “L” for Power ON.



(1) PS = L (power saving mode) at Power ON
(2) Set serial data 1μs later after power supply remains stable(Vcc ≥ 2.2V).
(3) Relase power saving mode (PS: L → H) 100nS later after setting serial data.

■ SERIAL DATA INPUT TIMING



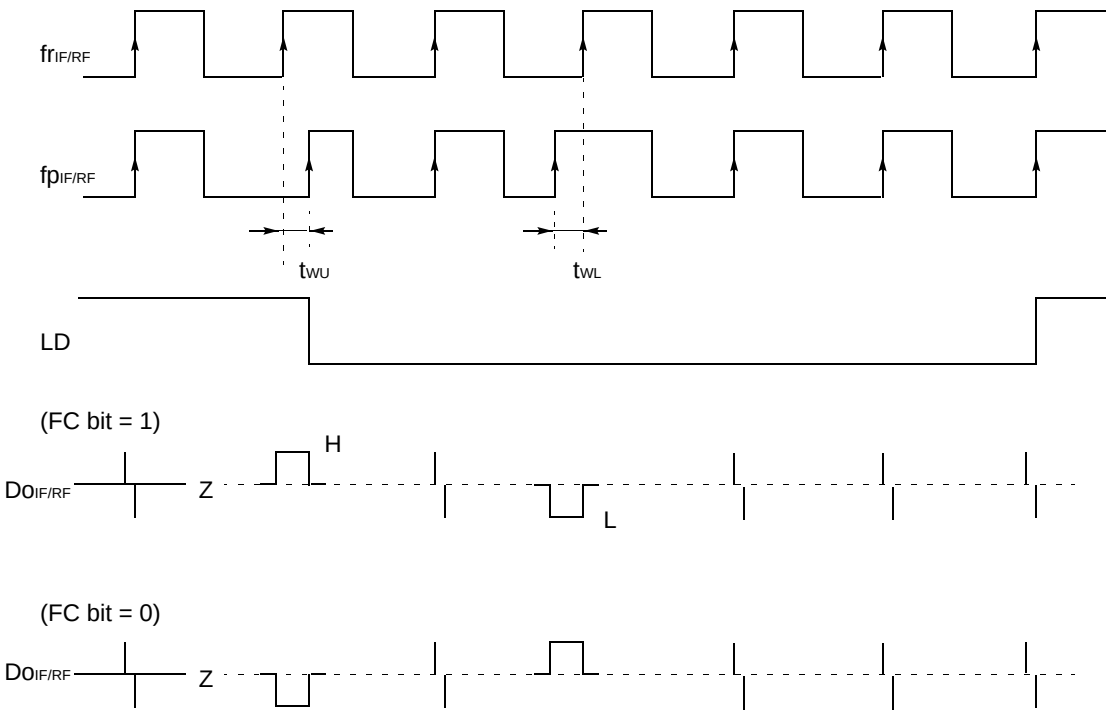
On the rising edge of the clock, one bit of data is transferred into the shift register.

Parameter	Min.	Typ.	Max.	Unit
t1	20	–	–	ns
t2	20	–	–	ns
t3	30	–	–	ns
t4	30	–	–	ns

Parameter	Min.	Typ.	Max.	Unit
t5	100	–	–	ns
t6	20	–	–	ns
t7	100	–	–	ns

Note: LE should be "L" when the data is transferred into the shift register.

■ PHASE DETECTOR OUTPUT WAVEFORM

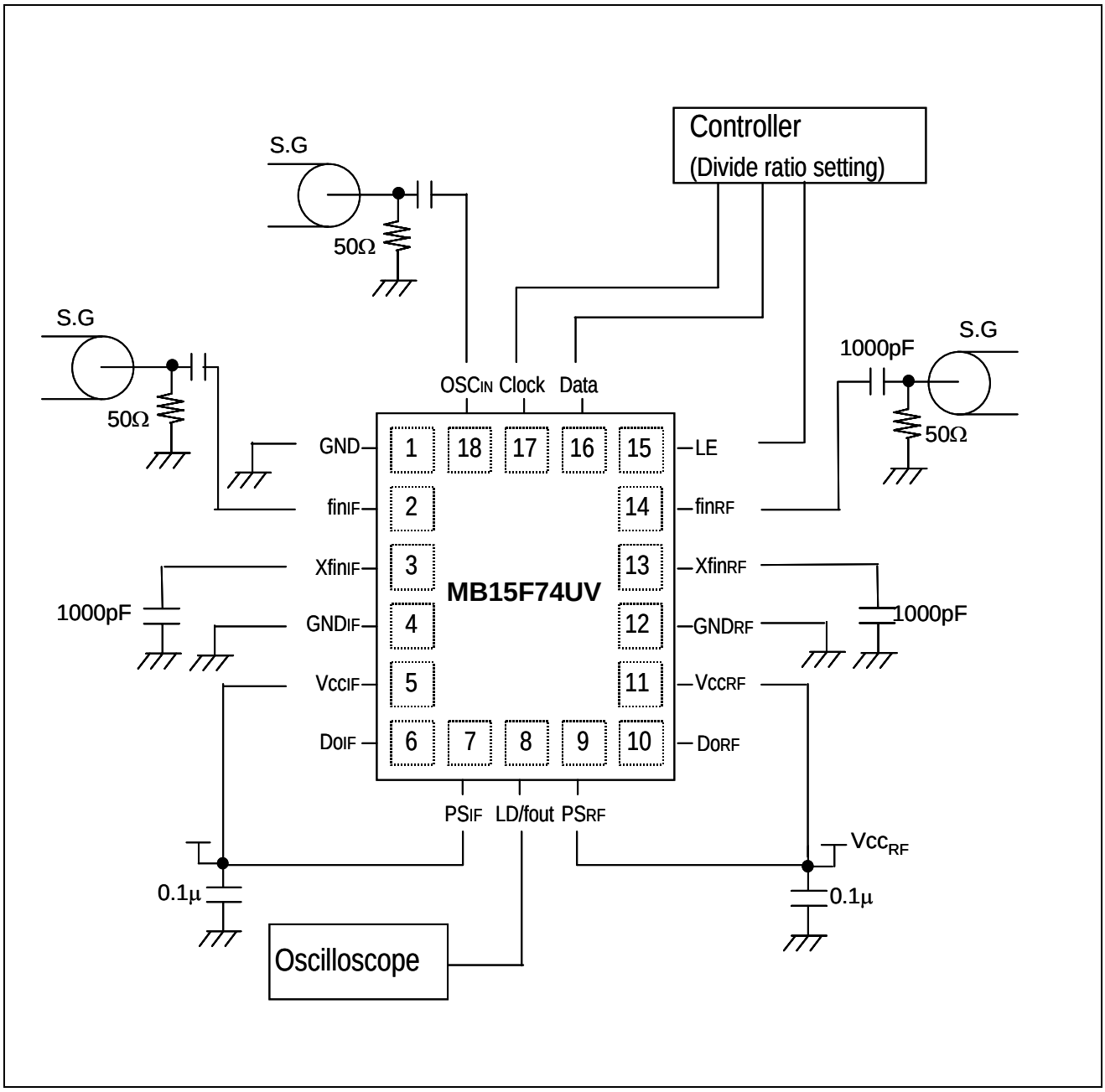


LD Output Logic Table

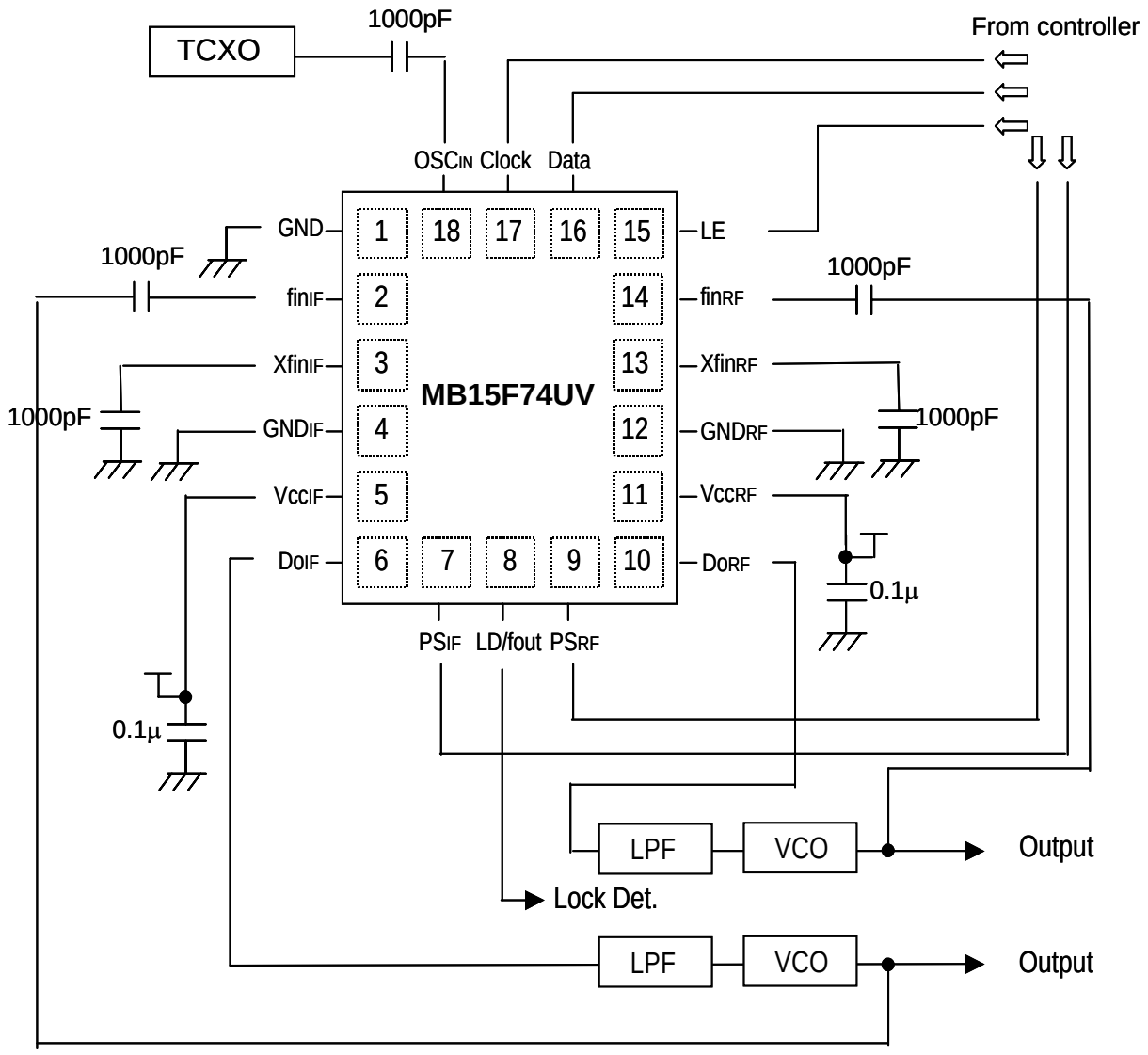
IF–PLL section	RF–PLL section	LD output
Locking state / Power saving state	Locking state / Power saving state	H
Locking state / Power saving state	Unlocking state	L
Unlocking state	Locking state / Power saving state	L
Unlocking state	Unlocking state	L

Note:
- Phase error detection range = -2π to $+2\pi$
- Pulses on $Do_{IF/RF}$ signals are output to prevent dead zone.
- LD output becomes low when phase error is t_{WU} or more.
- LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSCin input frequency as follows.
  $t_{WU} \geq 2/fosc$: i.e. $t_{WU} \geq 156.3ns$ when foscin = 12.8 MHz
  $t_{WL} \leq 4/fosc$: i.e. $t_{WL} \leq 312.5ns$ when foscin = 12.8 MHz

■ **TEST CIRCUIT (for Measuring Input Sensitivity fin/OSCin)**



■ APPLICATION EXAMPLE



Clock, Data, LE: Schmitt trigger circuit is provided (insert a pull-down or pull-up resistor to prevent oscillation when open-circuited in the input).

■ PACKAGE DIMENSION

BCC18(LCC-18P-M05)