

Data 10-bit bus transceiver (3-State)

MB2861

DESCRIPTION

The MB2861 bus transceiver provides high performance bus interface buffering for wide data/address paths of buses carrying parity. The MB2861 10-bit bus transceiver has NOR-ed transmit and receive output enables for maximum control flexibility.

buffering for wide data/address paths or buses carrying parity

- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Output capability: +64mA/-32mA
- Power-up 3-State

- Live insertion/extraction permitted
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

FEATURES

- Provides high performance bus interface

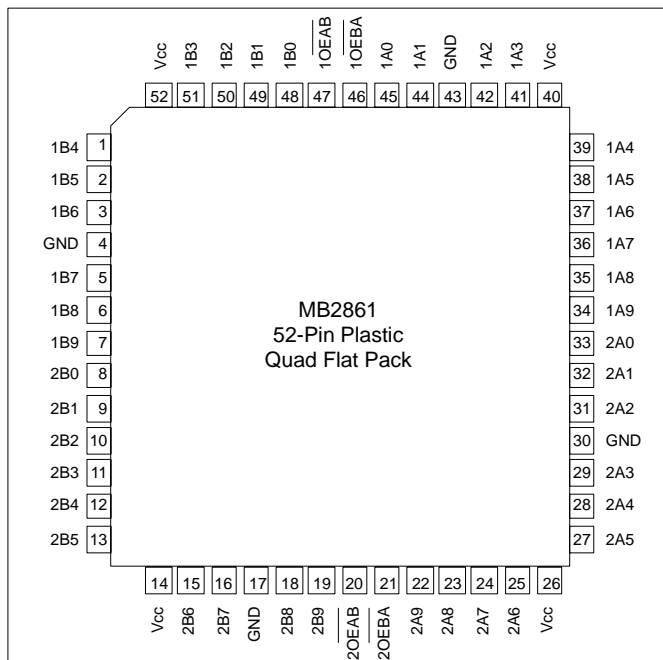
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C; GND = 0V$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	$C_L = 50pF; V_{CC} = 5V$	3.4	ns
C_{IN}	Input capacitance	$V_I = 0V$ or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	$V_O = 0V$ or V_{CC} ; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5V$	500	nA

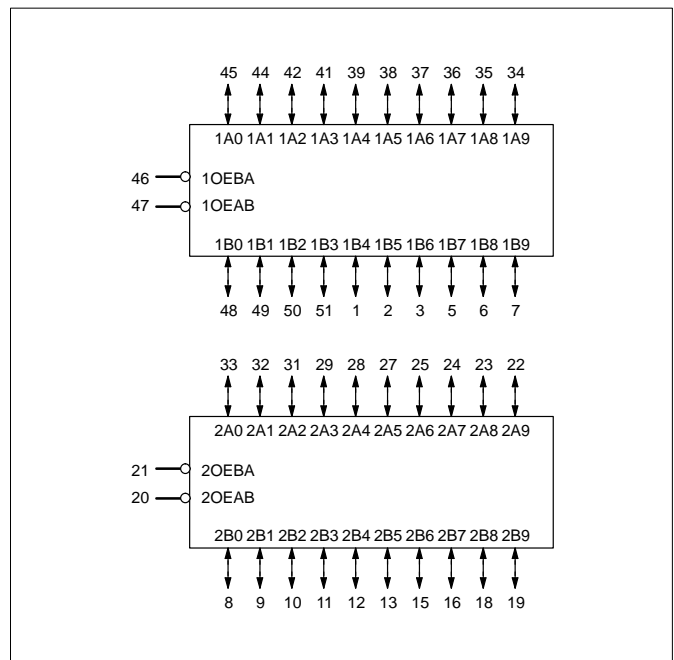
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
52-Pin Plastic Quad Flat Pack	-40°C to +85°C	MB2861BB	1418B

PIN CONFIGURATION



LOGIC SYMBOL



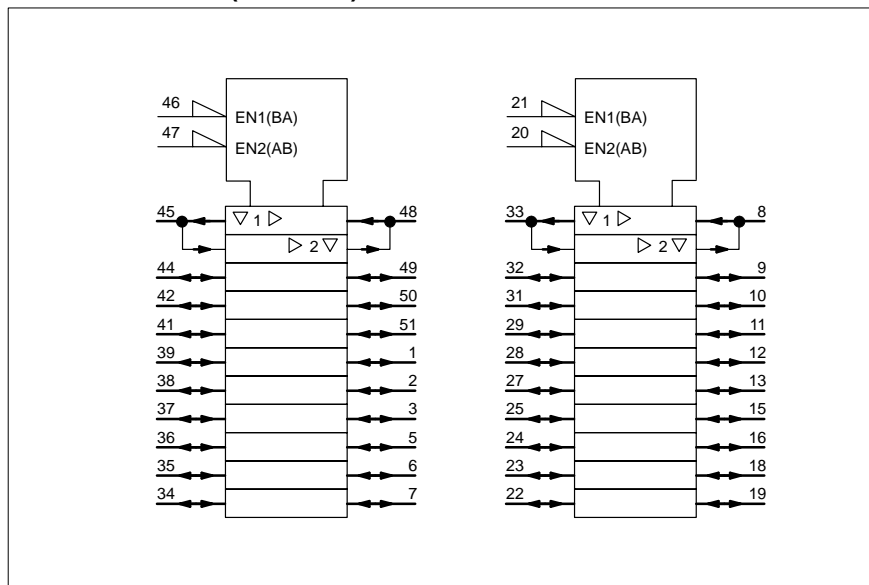
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MB2861

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 20	$\overline{1OEAB}$, $2OEAB$	A side to B side output enable inputs (active-Low)
45, 44, 42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24, 23, 22	1A0-1A9, 2A02nA9	Data inputs/outputs (A side)
48, 49, 50, 51, 1, 2, 3, 5, 6, 7 8, 9, 10, 11, 12, 13, 15, 16, 18, 19	1B0-1B9, 2B02nB9	Data outputs/outputs (B side)
46, 21	$\overline{1OEBA}$, $2OEBA$	B side to A side output enable inputs (active-Low)
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	V _{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)

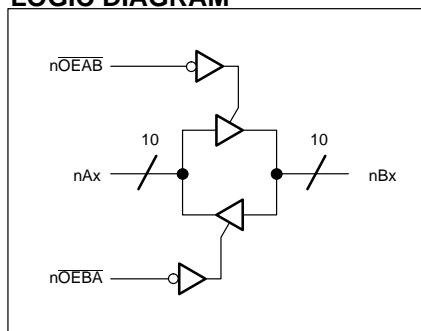


FUNCTION TABLE

INPUTS		OPERATING MODE
nOEAB	nOEBA	
L	H	A data to B bus
H	L	B data to A bus
H	H	Z

H = High voltage level
 L = Low voltage level
 X = Don't care
 Z = High impedance "off" state

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage ³		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA		-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
I _I	Input leakage current	Control pins V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins V _{CC} = 5.5V; V _I = GND or 5.5V		±5	±100		±100	µA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	µA
I _{PD/PD}	Power-up/down 3-State output current ³	V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = Don't care		±5.0	±50		±50	µA
I _{IH} + I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		5.0	50		50	µA
I _{IL} + I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		-5.0	-50		-50	µA
I _{CEx}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	µA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	-50	-80	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		65	250		250	µA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		45	72		72	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		65	250		250	µA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		0.5	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1 to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

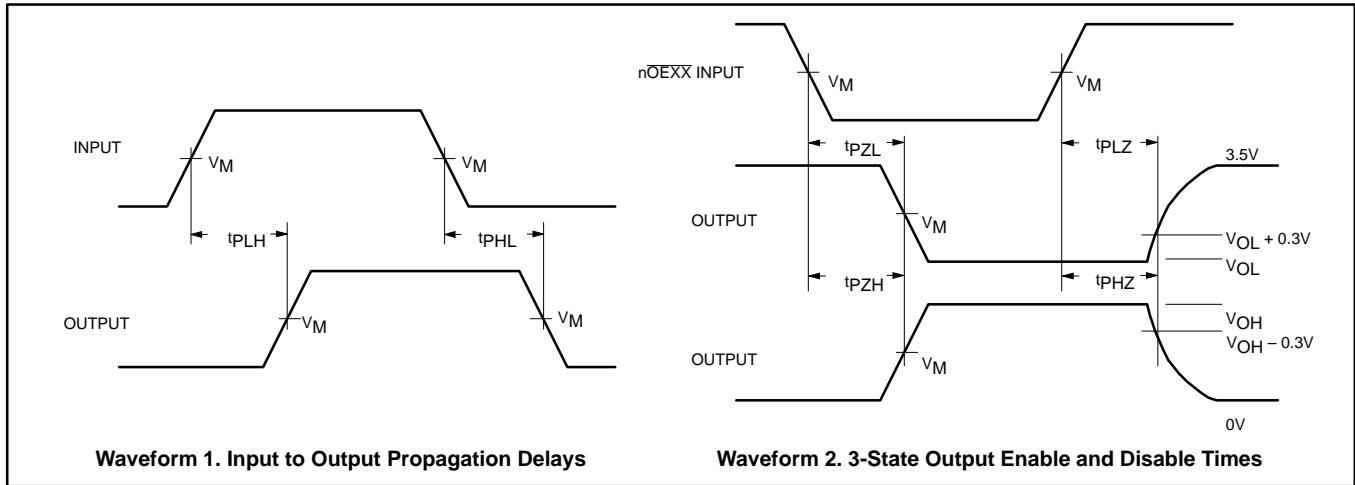
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	1.4 1.5	2.9 2.9	4.1 4.1	1.4 1.5	4.6 4.6	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.5 2.0	3.0 3.6	3.9 4.8	1.5 2.0	4.6 5.3	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.2 1.7	3.6 3.1	4.8 4.3	1.2 1.7	5.3 4.8	ns

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AC WAVEFORMS

$V_M = 1.5V$, $V_{IN} = GND$ to $3.0V$



TEST CIRCUIT AND WAVEFORM

