8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89820 Series

MB89821/823R/825/P825/PV820

■ DESCRIPTION

MB89820 series is a line of single-chip microcontrollers using the F²MC-8L* CPU core which can operate at low voltage but at high speed. In addition to an LCD controller/driver allowing 200-pixel display the microcontrollers contain a variety of peripheral functions such as timers, a UART, a serial interface, and an external interrupt. The configuration of the MB89820 series is therefore best suited to control of LCD display panels.

* : F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- Minimum execution time : 0.8 μs/5 MHz (Vcc = +5.0 V)
- F²MC-8L family CPU core

              Instruction set optimized for controllers
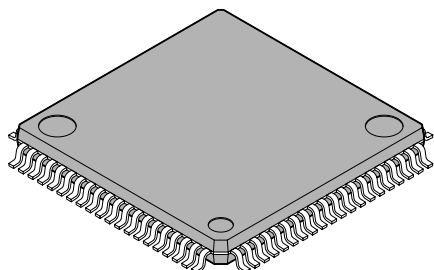   Multiplication and division instructions
                 16-bit arithmetic operations
                 Test and branch instructions
                 Bit manipulation instructions, etc.

- LCD controller/driver
  Max 50 segments × 4 commons
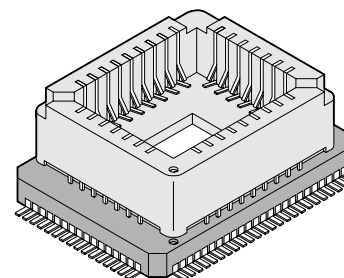 Divided resistor for LCD power supply

(Continued)

■ PACKAGES

80 Pin Plastic QFP

(FTP-80P-M11)

80 Pin Plastic MQFP

(MQP-80C-P01)

FUJITSU

(Continued)

- Three types of timers
  8-bit PWM timer (also usable as a reload timer)
  8-bit pulse width count timer (also usable as a reload timer)
  20-bit time-base timer

- Two serial interfaces
  8-bit synchronous serial interface (Switchable transfer direction allows communication with various equipment.)
  UART (5-, 7-, 8-bit transfer capable)

- External interrupt : 2 channels
  Capable of wake-up from low-power consumption modes (with an edge detection function)

- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)

■ PRODUCT LINEUP

Part number Parameter	MB89821	MB89823R	MB89825	MB89P825	MB89PV820
Classification	Mass production product (mask ROM products)			One-time PROM product	Piggyback/evaluation product for evaluation and development
ROM size	4 K × 8 bits (internal mask ROM)	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal PROM, programming with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	128 × 8 bits	256 × 8 bits			1024 × 8 bits
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.8 µs/5 MHz (V_{CC} = 5.0 V) Interrupt processing time: 7.2 µs/5 MHz (V_{CC} = 5.0 V)				
Ports	I/O ports (N-ch open-drain): 16 (All also serve as segment pins.)[*1] I/O ports (N-ch open-drain): 6 I/O ports (CMOS): 6 (5 ports also serve as peripheral I/O.) Input ports: 4 (1 port also serves as an external interrupt input.) Total: 32 (Max)				
8-bit PWM timer	8-bit reload timer operation (toggled output capable) 8-bit resolution PWM operation Operating clock (pulse width count timer output: 0.8 µs, 12.8 µs, 51.2 µs/5 MHz)				
8-bit pulse width count timer	8-bit reload timer operation 8-bit pulse width count operation (continuous measurement capable "H" width, "L" width, or single-cycle measurement capable) Operating clock (0.8 µs, 3.2 µs, 25.6 µs/5 MHz)				

(Continued)

(Continued)

Part number / Parameter	MB89821	MB89823R	MB89825	MB89P825	MB89PV820
8-bit serial I/O	8 bits One clock selectable from four transfer clocks (one external shift clock, three internal shift clock, three internal shift clocks: 1.6 μs, 6.4 μs, 25.6 μs/5 MHz) LSB first/MSB first selectability				
UART	5-, 7-, 8-bit transfer capable Internal baud-rate generator (Max 78125 bps/5 MHz)				
LCD controller/ driver	Common output: 4 Segment output: 50 (Max) Operating mode: 1/2 bias, 1/2 duty; 1/3 bias, 1/3 duty; 1/3 bias, 1/4 duty LCD display RAM size: 50 $\times$ 4 bits Dividing resistor for LCD driving: Built-in (An external resistor selectable)				
External interrupt	2 channels (edge selectable) (1 channel also serves as a pulse width count timer input)				
Standby mode	Sleep mode, stop mode				
Process	CMOS				
Operating voltage*2	2.2 V*3 to 6.0 V			2.7 V to 6.0 V	
EPROM for use					MBM27C256A-20TV (LCC package)

*1: The function is selected by the mask option.
*2: Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")
*3: The operation at less than 2.2 V is assured separately. Please contact FUJITSU LIMITED.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89821 MB89823R MB89825 MB89P825	MB89PV820
FPT-80P-M11	○	×
MQP-80C-P01	×	○

○ : Available   × : Not available

Note: For more information about each package, see section "■ Package Dimensions."

MB89820 Series

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89821, the register bank address upper than 0140_H cannot be used. On the MB89823R, MB89825 and MB89P825, each register bank addresses upper than 0180_H can be used.

- On the MB89P825, addresses $BFF0_H$ to $BFF6_H$ comprise the option setting area, option settings can be read by reading these addresses.

- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- In the case of the MB89PV820, add the current consumed by the EPROM which is connected to the top socket.

- However, the current consumption in sleep/stop modes is the same. (For more information, see section "■ Electrical Characteristics.")
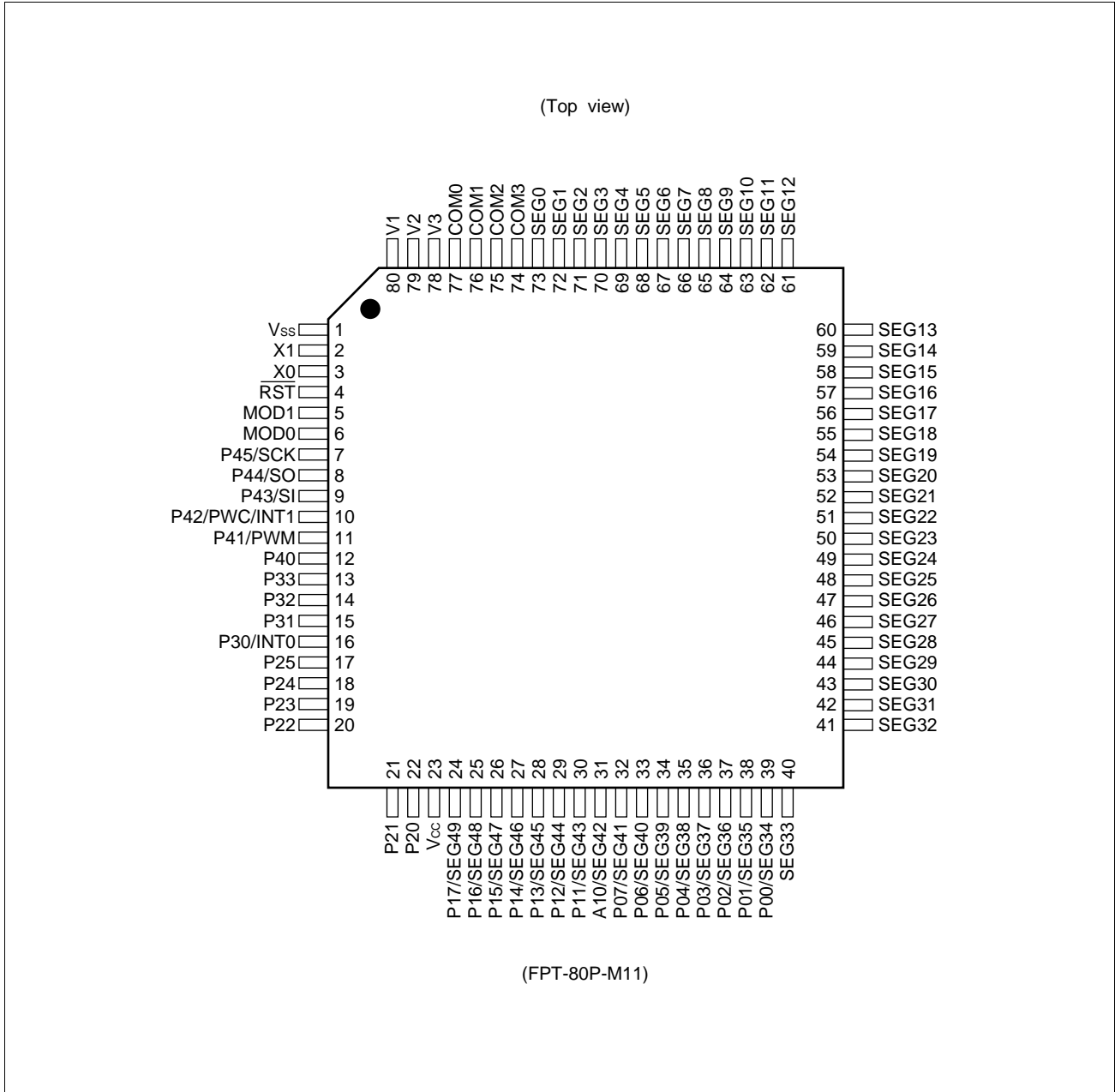
3. Mask Options

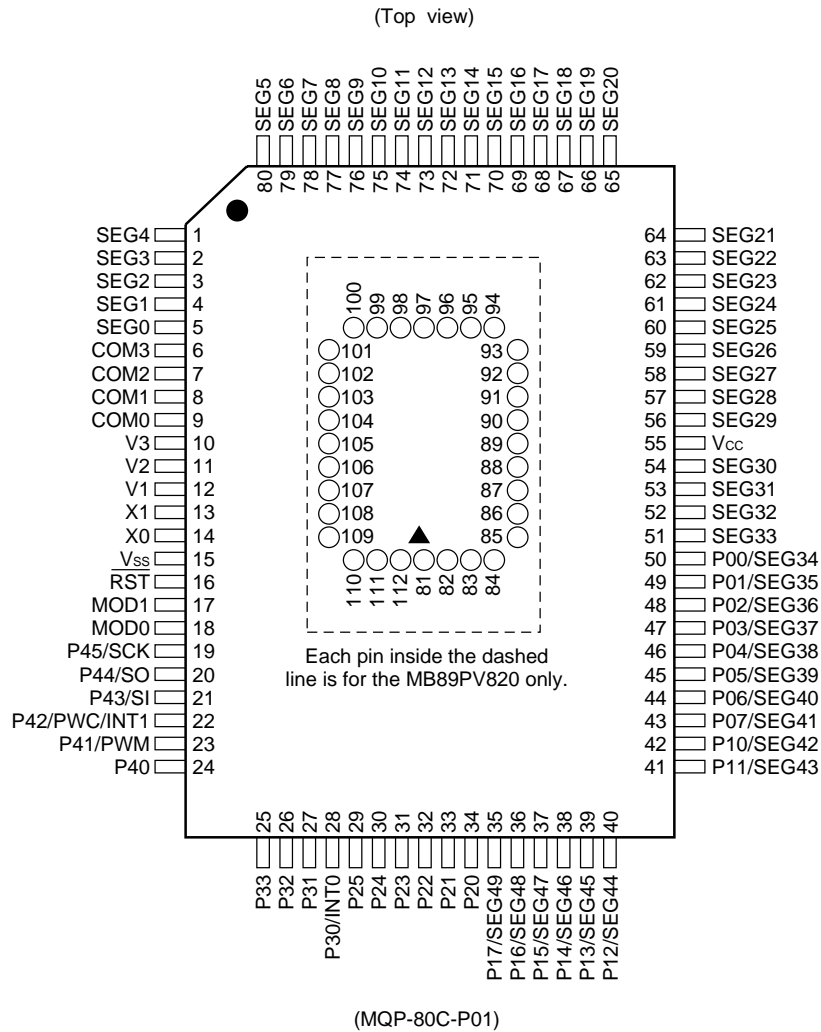Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options."

Take particular care on the following point : Options are fixed on the MB89PV820.

4

■ PIN ASSIGNMENT

(Top view)

Top pins (left to right, pins 80 to 61):
V1, V2, V3, COM0, COM1, COM2, COM3, SEG0, SEG1, SEG2, SEG3, SEG4, SEG5, SEG6, SEG7, SEG8, SEG9, SEG10, SEG11, SEG12

Left side pins (top to bottom):
Vss	1
X1	2
X0	3
RST	4
MOD1	5
MOD0	6
P45/SCK	7
P44/SO	8
P43/SI	9
P42/PWC/INT1	10
P41/PWM	11
P40	12
P33	13
P32	14
P31	15
P30/INT0	16
P25	17
P24	18
P23	19
P22	20

Right side pins (top to bottom):
60	SEG13
59	SEG14
58	SEG15
57	SEG16
56	SEG17
55	SEG18
54	SEG19
53	SEG20
52	SEG21
51	SEG22
50	SEG23
49	SEG24
48	SEG25
47	SEG26
46	SEG27
45	SEG28
44	SEG29
43	SEG30
42	SEG31
41	SEG32

Bottom pins (left to right, pins 21 to 40):
P21, P20, Vcc, P17/SEG49, P16/SEG48, P15/SEG47, P14/SEG46, P13/SEG45, P12/SEG44, P11/SEG43, A10/SEG42, P07/SEG41, P06/SEG40, P05/SEG39, P04/SEG38, P03/SEG37, P02/SEG36, P01/SEG35, P00/SEG34, SEG33

(FPT-80P-M11)

(Top view)

Each pin inside the dashed line is for the MB89PV820 only.

(MQP-80C-P01)

- **Pin assignment on package top (MB89PV820 only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
81	N.C.	89	A2	97	N.C.	105	$\overline{OE}$
82	V_{PP}	90	A1	98	O4	106	N.C.
83	A12	91	A0	99	O5	107	A11
84	A7	92	N.C.	100	O6	108	A9
85	A6	93	O1	101	O7	109	A8
86	A5	94	O2	102	O8	110	A13
87	A4	95	O3	103	$\overline{CE}$	111	A14
88	A3	96	V_{SS}	104	A10	112	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
QFP*1	MQFP*2			
3	14	X0	A	Clock crystal oscillator pins
2	13	X1		
6	18	MOD0	B	Operating mode selection pins Connect directly to Vss.
5	17	MOD1		
4	16	RST	C	Reset I/O pin This pin is an N-ch open-drain type with a pull-up resistor, and a hysteresis input type. "L" is output from this pin by an internal reset source (optional function). The internal circuit is initialized by the input of "L".
39 to 32	50 to 43	P00/SEG34 to P07/SEG41	D	General-purpose N-ch open-drain I/O ports Also serve as an LCD controller/driver segment output. The port and segment output are switched by mask option in 8-bit unit.
31 to 24	42 to 35	P10/SEG42 to P17/SEG49	D	General-purpose N-ch open-drain I/O ports Also serve as an LCD controller/driver segment output. The port and segment output are switched by mask option in 4 to 1-bit unit.
22 to 17	34 to 29	P20 to P25	F	General-purpose N-ch open-drain I/O ports A pull-up resistor option is provided.
16	28	P30/INT0	H	General-purpose input port The input is hysteresis input. Also serves as an external interrupt input (INT0). A pull-up resistor option is provided.
15 to 13	27 to 25	P31 to P33	H	General-purpose input ports These pins are a hysteresis input type. A pull-up resistor option is provided.
12	24	P40	E	General-purpose I/O port A pull-up resistor option is provided.
11	23	P41/PWM	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as an 8-bit PWM timer toggle output (PWM).
10	22	P42/PWC/INT1	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as an 8-bit pulse width count timer input (PWC) and an external interrupt input (INT1). The PWC and INT1 input is hysteresis input.
9	21	P43/SI	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as an 8-bit serial I/O and a UART data input (SI). The SI input is hysteresis input.

*1: FPT-80P-M11
*2: MQP-80C-P01

(Continued)

(Continued)

Pin no.		Pin name	Circuit type	Function
QFP*1	MQFP*2			
8	20	P44/SO	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as a serial I/O and a UART data output (SO).
7	19	P45/SCK	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as a serial I/O and a UART clock I/O (SCK). The SCK input is hysteresis input.
73 to 40	5 to 1, 80 to 56, 54 to 51	SEG0 to SEG33	G	LCD controller/driver segment output pins
77 to 74	9 to 6	COM0 to COM3	G	LCD controller/driver common output pins
80 to 78	12 to 10	V1 to V3	—	LCD driving power supply pins
23	55	V_{CC}	—	Power supply pin
1	15	V_{SS}	—	Power supply (GND) pin

*1: FPT-80P-M11
*2: MQP-80C-P01

• **External EPROM pins (MB89PV820 only)**

Pin no.	Pin name	I/O	Function
82	V_{PP}	O	"H" level output pin
83 84 85 86 87 88 89 90 91	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
93 94 95	O1 O2 O3	I	Data input pins
96	V_{SS}	O	Power supply (GND) pin
98 99 100 101 102	O4 O5 O6 O7 O8	I	Data input pins
103	$\overline{CE}$	O	ROM chip enable pin Outputs "H" during standby.
104	A10	O	Address output pin
105	$\overline{OE}$	O	ROM output enable pin Outputs "L" at all times.
107 108 109	A11 A9 A8	O	Address output pins
110	A13	O	
111	A14	O	
112	V_{CC}	O	EPROM power supply pin
81 92 97 106	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	X1 X0 Standby control signal	• Crystal oscillator circuit • At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
B		
C	R P-ch N-ch	• At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • Hysteresis input
D	P-ch N-ch P-ch N-ch N-ch Port	• N-ch open-drain output • CMOS input • Segment output optional
E	R P-ch P-ch N-ch Peripheral Port	• CMOS output • CMOS input • Hysteresis input (peripheral input) • Pull-up resistor optional

(Continued)

Type	Circuit	Remarks
F		• N-ch open-drain output • CMOS input • Pull-up resistor optional
G		• LCD controller/driver
H		• Hysteresis input • Pull-up resistor optional

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on "1. Absolute Maximum Ratings" in section "■ Electrical Characteristics" is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

7. Note to Noise In the External Reset Pin ($\overline{RST}$)

If the reset pulse applied to the external reset pin ($\overline{RST}$) does not meet the specifications, it may cause malfunctions. Use caution so that the reset pulse less than the specifications will not be fed to the external reset pin ($\overline{RST}$).
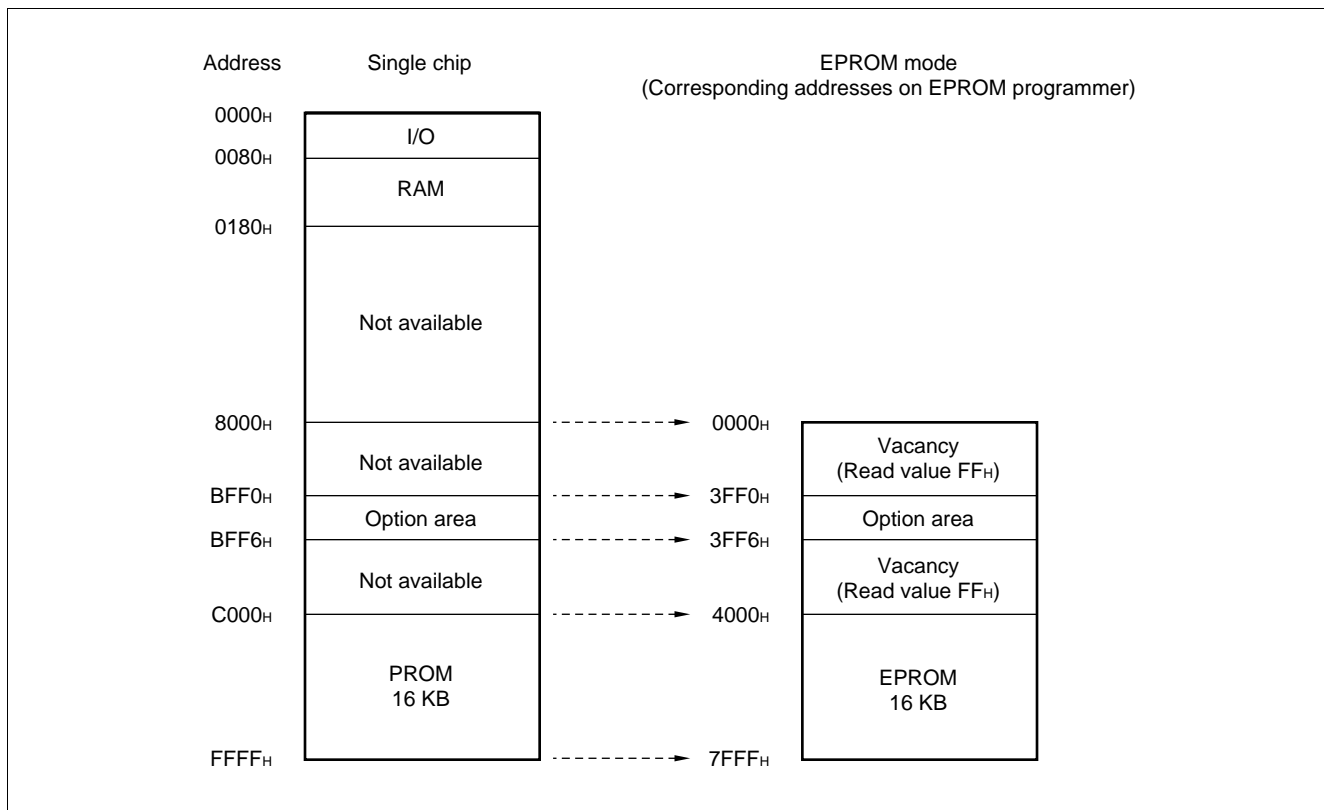
■ PROGRAMMING TO THE EPROM ON THE MB89P825

The MB89P825 is an OTPROM (one-time PROM) version for the MB89820 series.

1. Features

• 16-Kbyte PROM on chip
• Options can be set using the EPROM programmer.
• Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below.

Address	Single chip	EPROM mode (Corresponding addresses on EPROM programmer)	
0000$_H$	I/O		
0080$_H$	RAM		
0180$_H$			
	Not available		
8000$_H$	Not available	0000$_H$	Vacancy (Read value FF$_H$)
BFF0$_H$	Option area	3FF0$_H$	Option area
BFF6$_H$	Not available	3FF6$_H$	Vacancy (Read value FF$_H$)
C000$_H$	PROM 16 KB	4000$_H$	EPROM 16 KB
FFFF$_H$		7FFF$_H$	

3. Programming to the EPROM

In EPROM mode, the MB89P825 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

• **Programming procedure**

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 4000$_H$ to 7FFF$_H$ (note that addresses C000$_H$ to FFFF$_H$ while operating as a single chip assign to 4000$_H$ to 7FFF$_H$ in EPROM mode).
Load option data into addresses 3FF0$_H$ to 3FF5$_H$ of the EPROM programmer. (For information about each corresponding option, see "7. OTPROM Option Bit Map.")

(3) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product for a product with a blanked OTPROM microcomputer program.

```
                    ┌─────────────────────┐
                    │   Program, verify   │
                    └─────────────────────┘
                               │
                               ▼
                    ┌─────────────────────┐
                    │       Aging         │
                    │   +150 ˚C, 48 h     │
                    └─────────────────────┘
                               │
                               ▼
                    ┌─────────────────────┐
                    │  Data verification  │
                    └─────────────────────┘
                               │
                               ▼
                    (      Assembly      )
```
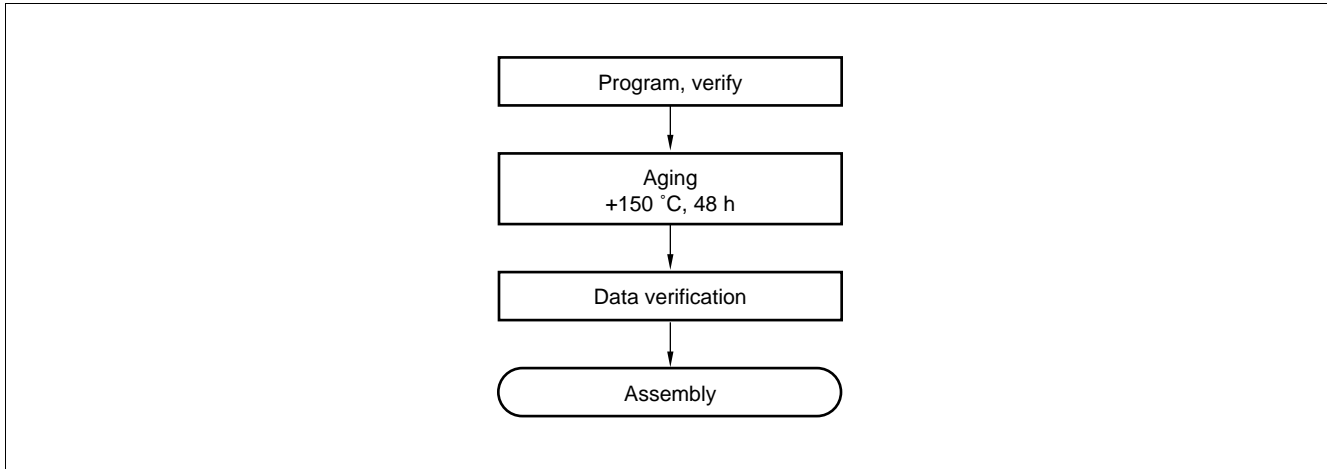
5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
FPT-80P-M11	ROM-80QF2-28DP-8L3

Inquiry: Sunhayato Corp. : TEL   : +81-3-3984-7791
                           FAX   : +81-3-3971-0535
                           E-mail : adapter@sunhayato.co.jp

7. OTPROM Option Bit Map

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FF0$_H$	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Reset pin output 1: Yes 0: No	Oscillation stabilization time 1: 2^{18}/F_C 0: 2^{14}/F_C	Power-on reset 1: Yes 0: No
3FF1$_H$	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable
3FF2$_H$	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable
3FF3$_H$	Vacancy Readable	Vacancy Readable	P25 Pull-up 1: No 0: Yes	P24 Pull-up 1: No 0: Yes	P23 Pull-up 1: No 0: Yes	P22 Pull-up 1: No 0: Yes	P21 Pull-up 1: No 0: Yes	P20 Pull-up 1: No 0: Yes
3FF4$_H$	Vacancy Readable	Vacancy Readable	P45 Pull-up 1: No 0: Yes	P44 Pull-up 1: No 0: Yes	P43 Pull-up 1: No 0: Yes	P42 Pull-up 1: No 0: Yes	P41 Pull-up 1: No 0: Yes	P40 Pull-up 1: No 0: Yes
3FF5$_H$	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes

Notes: • Set each bit to 1 to erase.
      • Do not write 0 to the vacant bit.
        The read value of the vacant bit is 1, unless 0 is written to it.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TV

2. Programming Socket Adapter

To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sunhayato Corp.) listed below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sunhayato Corp. : TEL : +81-3-3984-7791
FAX : +81-3-3971-0535
E-mail : adapter@sunhayato.co.jp

3. Memory Space

Memory space in each mode, such as 32 Kbyte PROM, option area is diagrammed below.
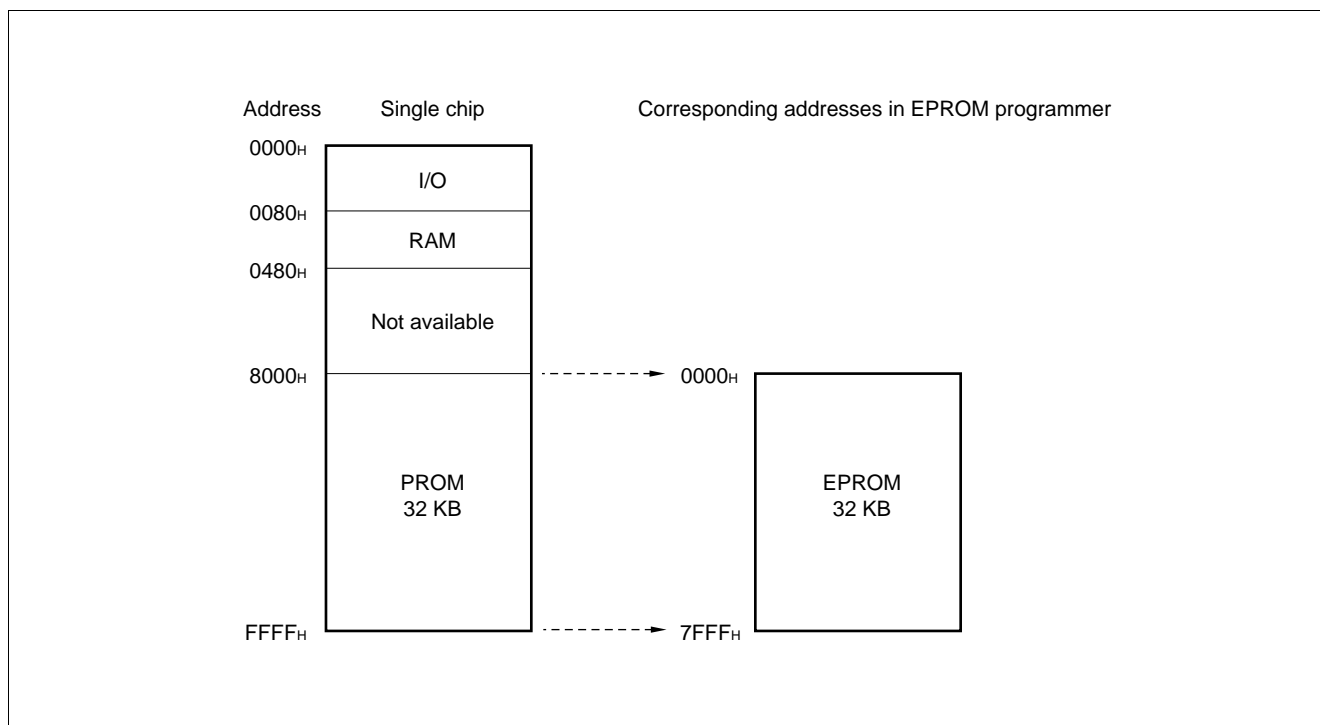
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

X0
X1
Oscillator

Clock controller

20-bit time-base timer

8-bit PWM timer → P41/PWM

External interrupt

RST → Reset circuit (WDT)

Internal bus

Port 4

8-bit pulse width timer/counter

Noise cancel-lation → P42/PWC/INT1

Port 2
N-ch open-drain I/O port
P20 to P25 6

8-bit serial I/O → P45/SCK
P44/SO
P43/SI

P30/INT0 → External interrupt

UART

P31 to P33 3 Port 3 I/O port

CMOS I/O port → P40

RAM

N-ch open-drain I/O port

F2MC-8L CPU

Port 0 and port 1

16 → P00/SEG34 to P07/SEG41 8

ROM

LCD controller/driver

8 → P10/SEG42 to P17/SEG49

Other pins
MOD0, MOD1,
Vcc, Vss

34 → SEG0 to SEG33

4 → COM0 to COM3

3 → V1 to V3

MB89820 Series

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89820 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89820 series is structured as illustrated below.

Memory Space
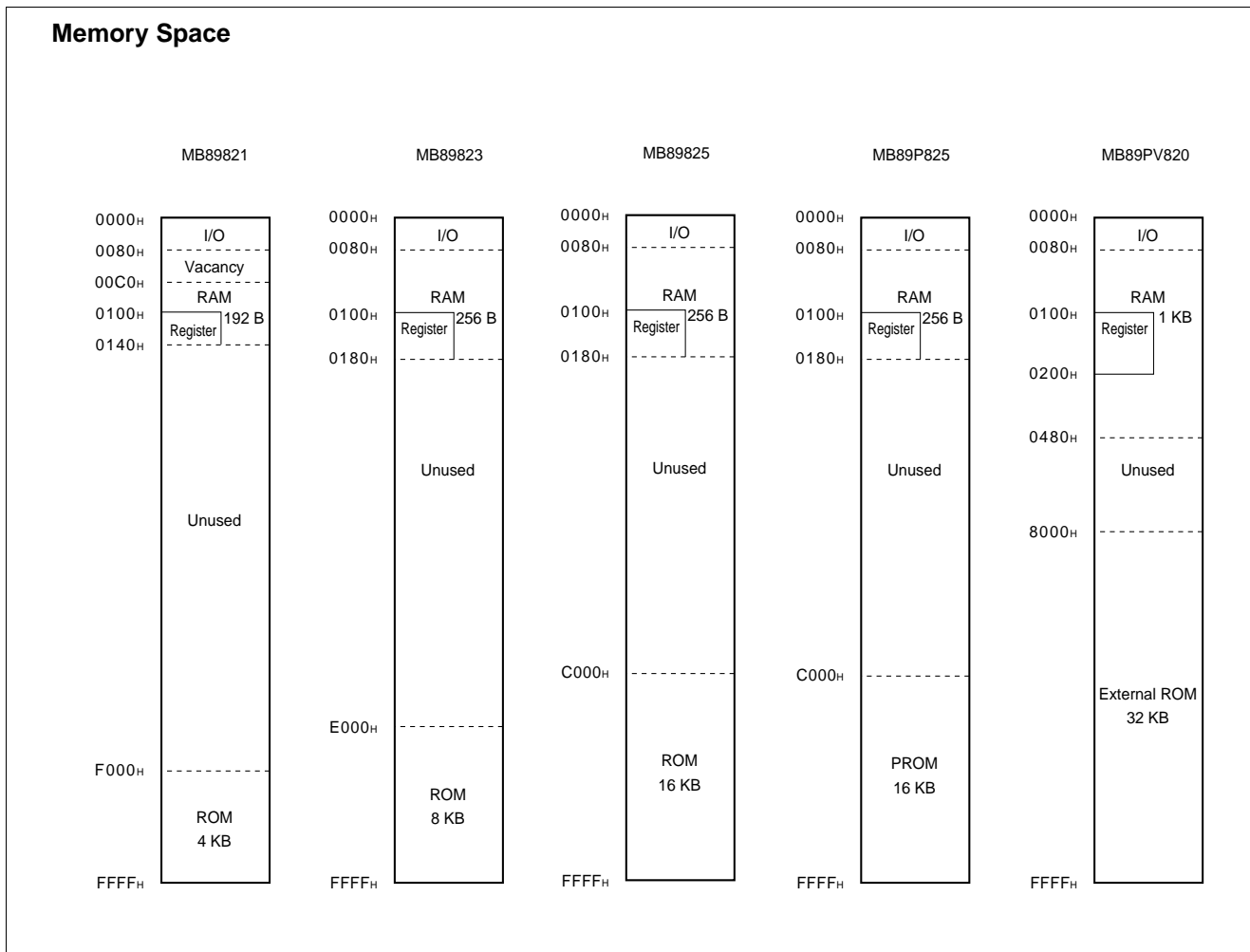
2. Registers

The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):   A 16-bit register for indicating instruction storage positions

Accumulator (A):   A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.

Temporary accumulator (T):   A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.

Index register (IX):   A 16-bit register for index modification

Extra pointer (EP):   A 16-bit pointer for indicating a memory address

Stack pointer (SP):   A 16-bit register for indicating a stack area

Program status (PS):   A 16-bit register for storing a register pointer, a condition code

```
           16 bits                                      Initial value
  ┌──────────────────────┐
  │          PC          │   : Program counter          FFFDH
  ├──────────────────────┤
  │          A           │   : Accumulator              Undefined
  ├──────────────────────┤
  │          T           │   : Temporary accumulator    Undefined
  ├──────────────────────┤
  │          IX          │   : Index register           Undefined
  ├──────────────────────┤
  │          EP          │   : Extra pointer            Undefined
  ├──────────────────────┤
  │          SP          │   : Stack pointer            Undefined
  ├──────────────────────┤
  │          PS          │   : Program status      I-flag = 0, IL1, IL0 = 11
  └──────────────────────┘                              Other bits are undefined.
```
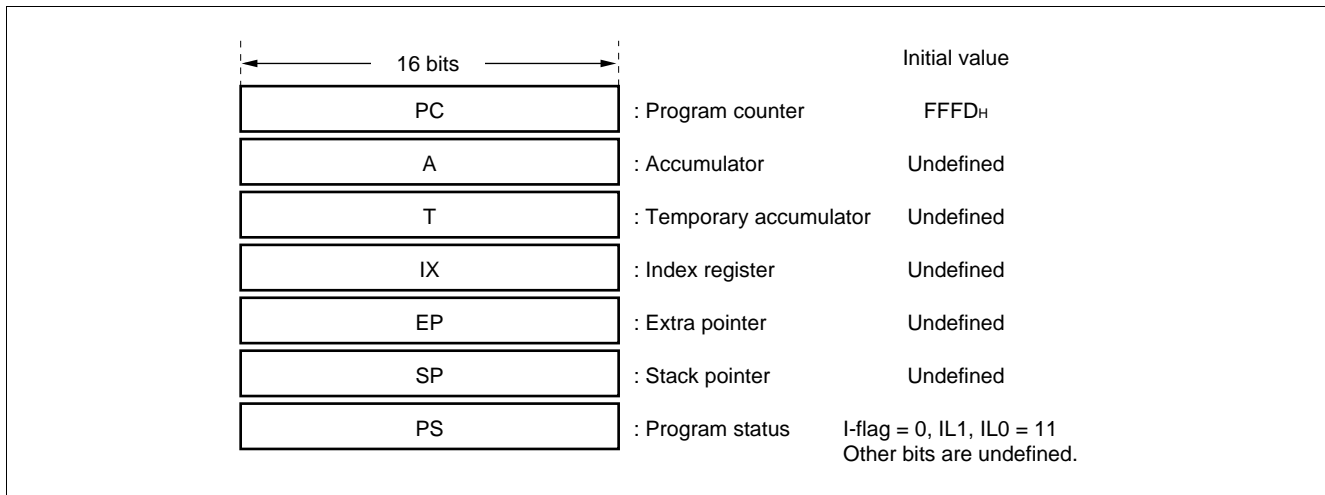
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register

```
      15    14    13    12    11    10    9     8     7     6     5     4     3     2     1     0
     ┌─────────────────────────────┬───────┬───────┬───────┬─────┬─────┬───────────┬─────┬─────┬─────┬─────┐
  PS │             RP              │Vacancy│Vacancy│Vacancy│  H  │  I  │  IL1, 0   │  N  │  Z  │  V  │  C  │
     └─────────────────────────────┴───────┴───────┴───────┴─────┴─────┴───────────┴─────┴─────┴─────┴─────┘
       └──────────────────── RP ───────────────────┘       └──────────────────── CCR ────────────────────┘
```
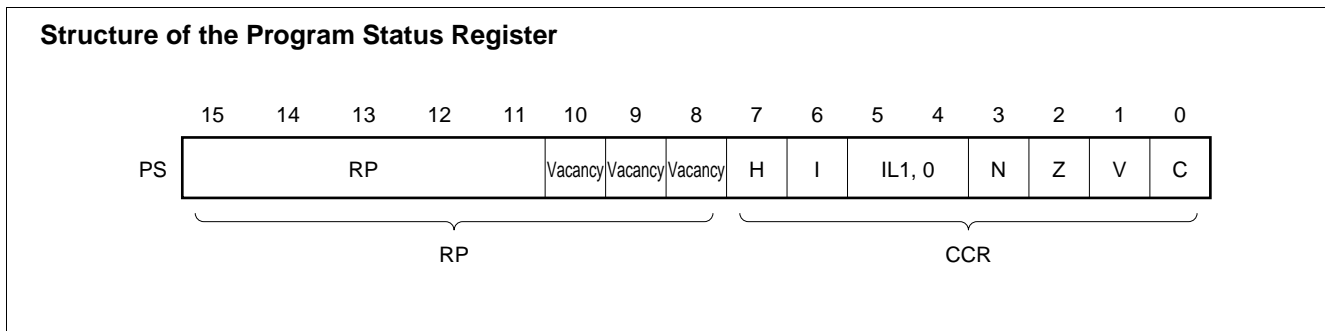
The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area

```
                                                  RP           Lower OP codes
          "0"  "0"  "0"  "0"  "0"  "0"  "0"  "1"  R4  R3  R2  R1  R0  b2  b1  b0

           ↓    ↓    ↓    ↓    ↓    ↓    ↓    ↓    ↓   ↓   ↓   ↓   ↓   ↓   ↓   ↓

Generated addresses  A15 A14 A13 A12 A11 A10  A9   A8   A7  A6  A5  A4  A3  A2  A1  A0
```
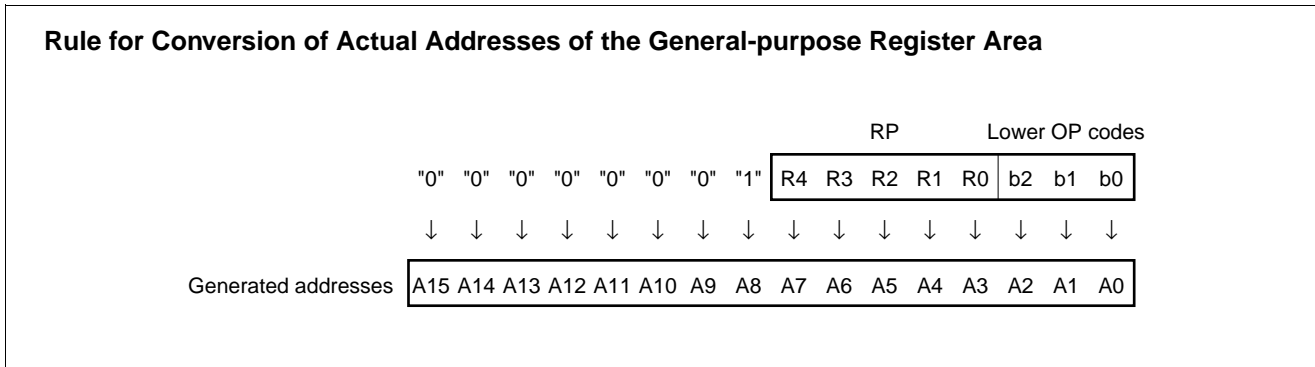
The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag : Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag : Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0 : Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag : Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag : Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag : Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

C-flag : Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 16 banks can be used on the MB89823R/825 (RAM 256 × 8 bits). The bank currently in use is indicated by the register bank pointer (RP).

NoteThe number of register banks that can be used varies with the RAM size.

MB89821	0100_H to $013F_H$	8 banks
MB89823R	0100_H to $017F_H$	16 banks
MB89825	0100_H to $017F_H$	16 banks
MB89P825	0100_H to $017F_H$	16 banks
MB89PV820	0100_H to $01FF_H$	32 banks

Register Bank Configuration

This address = $0100_H + 8 \times (RP)$

R 0
R 1
R 2
R 3
R 4
R 5
R 6
R 7

16 banks

Memory area
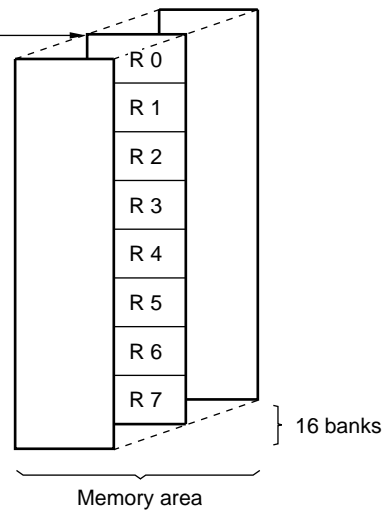
■ I/O MAP

Address	Read/write	Register name	Register description
00$_H$	(R/W)	PDR0	Port 0 data register
01$_H$			Vacancy
02$_H$	(R/W)	PDR1	Port 1 data register
03$_H$			Vacancy
04$_H$	(R/W)	PDR2	Port 2 data register
05$_H$			Vacancy
06$_H$			Vacancy
07$_H$			Vacancy
08$_H$	(R/W)	STBC	Standby control register
09$_H$	(R/W)	WDTC	Watchdog timer control register
0A$_H$	(R/W)	TBCR	Time-base timer control register
0B$_H$			Vacancy
0C$_H$	(R)	PDR3	Port 3 data register
0D$_H$			Vacancy
0E$_H$	(R/W)	PDR4	Port 4 data register
0F$_H$	(W)	DDR4	Port 4 data direction register
10$_H$			Vacancy
11$_H$			Vacancy
12$_H$	(R/W)	CNTR	PWM timer control register
13$_H$	(W)	COMR	PWM timer compare register
14$_H$	(R/W)	PCR1	PWC pulse width control register 1
15$_H$	(R/W)	PCR2	PWC pulse width control register 2
16$_H$	(R/W)	RLBR	PWC reload buffer register
17$_H$	(R/W)	NCCR	PWC noise cancellation control register
18$_H$			Vacancy
19$_H$			Vacancy
1A$_H$			Vacancy
1B$_H$			Vacancy
1C$_H$	(R/W)	SMR	Serial mode register
1D$_H$	(R/W)	SDR	Serial data register
1E$_H$			Vacancy
1F$_H$			Vacancy

(Continued)

(Continued)

Address	Read/write	Register name	Register description
20$_H$	(R/W)	SMC1	UART serial mode control register 1
21$_H$	(R/W)	SRC	UART serial rate control register
22$_H$	(R/W)	SSD	UART serial status/data register
23$_H$	(R/W)	SIDR/SODR	UART serial data register
24$_H$	(R/W)	SMC2	UART serial mode control register 2
25$_H$			Vacancy
26$_H$			Vacancy
27$_H$			Vacancy
28$_H$			Vacancy
29$_H$			Vacancy
2A$_H$			Vacancy
2B$_H$			Vacancy
2C$_H$			Vacancy
2D$_H$			Vacancy
2E$_H$			Vacancy
2F$_H$			Vacancy
30$_H$	(R/W)	EIC1	External interrupt 1 control register
31$_H$ to 5F$_H$			Vacancy
60$_H$ to 78$_H$	(R/W)	VRAM	Display data RAM
79$_H$	(R/W)	LCR1	LCD controller/driver control register
7A$_H$	(R/W)	SEGR	Segment output selection register
7B$_H$			Vacancy
7C$_H$	(W)	ILR1	Interrupt level setting register 1
7D$_H$	(W)	ILR2	Interrupt level setting register 2
7E$_H$	(W)	ILR3	Interrupt level setting register 3
7F$_H$			Vacancy

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = 0.0 V)

Parameter	Symbol	Value Min	Value Max	Unit	Remarks
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	
LCD power supply voltage	V3	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	V3 pin
Input voltage	V_{I1}	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	V_{I1} must not exceed V_{SS} + 7.0 V. Except P00 to P07 and P10 to P17 for the MB89P825/PV820, and P20 to P25 without a pull-up resistor
	V_{I2}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P00 to P07 and P10 to P17 (when selected as ports) for the MB89821/823R/825, and P20 to P25 without a pull-up resistor
	V_{I3}	$V_{SS} - 0.3$	V3 + 0.3	V	P00 to P07 and P10 to P17 for the MB89P825/PV820
Output voltage	V_{O1}	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	V_{O1} must not exceed V_{SS} + 7.0 V. Except P00 to P07 and P10 to P17 for the MB89P825/PV820, and P20 to P25 without a pull-up resistor
	V_{O2}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P00 to P07 and P10 to P17 (when selected as ports) for the MB89821/823R/825, and P20 to P25 without a pull-up resistor
	V_{O3}	$V_{SS} - 0.3$	V3 + 0.3	V	P00 to P07 and P10 to P17 for the MB89P825/PV820
"L" level output current	I_{OL}	—	10	mA	Except power supply pins
"L" level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate) Except power supply pins
Total "L" level output current	ΣI_{OL}	—	40	mA	
"H" level output current	I_{OH}	—	–5	mA	Except power supply pins
"H" level average output current	I_{OHAV}	—	–2	mA	Average value (operating current × operating rate) Except power supply pins
Total "H" level output current	ΣI_{OH}	—	–10	mA	
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	2.2*	6.0*	V	Normal operation assurance range*
		1.5	6.0	V	Retains the RAM state in stop mode
LCD power supply voltage	V3	V_{SS}	6.0	V	V3 pin LCD power supply range. The optimum value is dependent on the element in use.
Operating temperature	T_A	−40	+85	°C	

*: The minimum operating power supply voltage varies with the operating frequency.
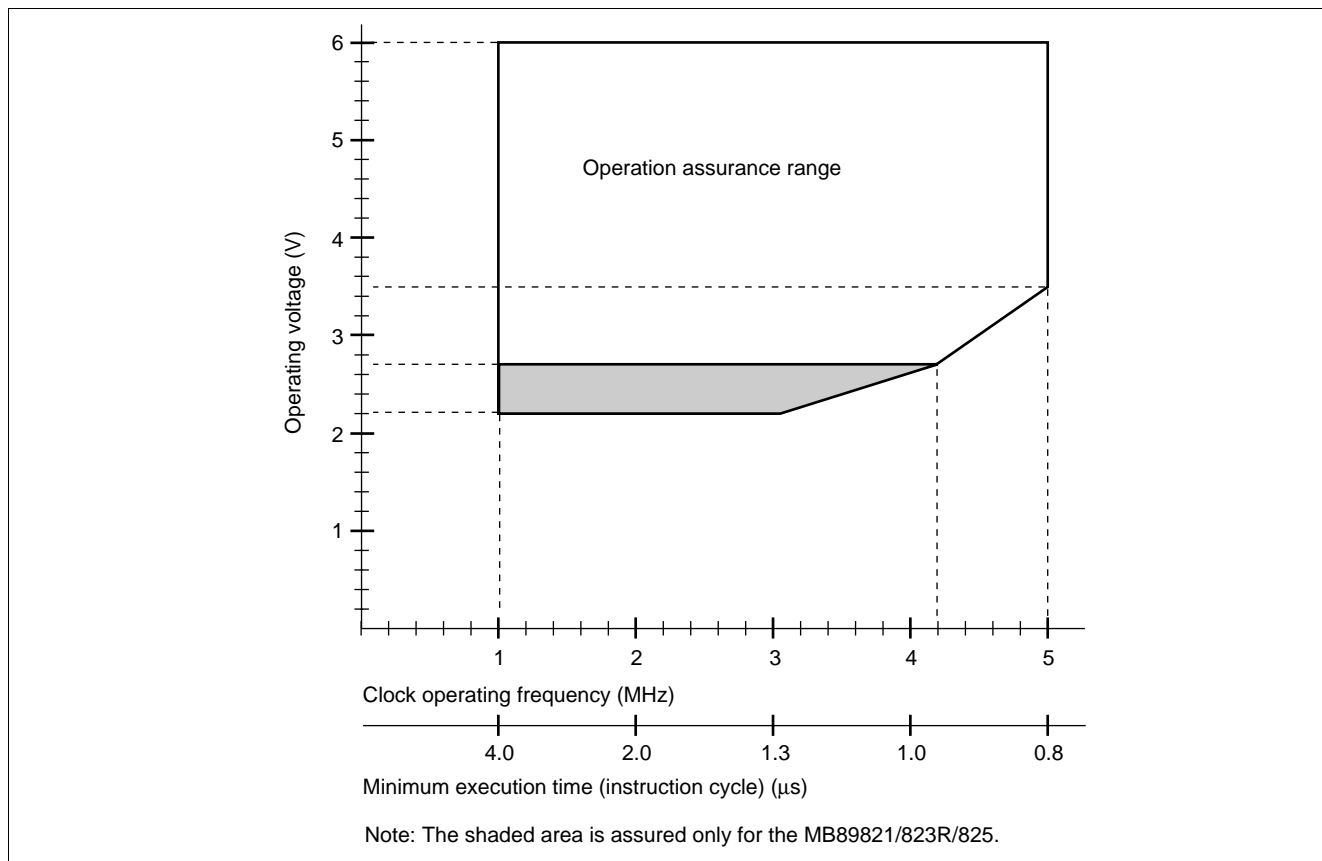
Figure 1   Operating Voltage vs. Clock Operating Frequency

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/F_C.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

$(V_{CC} = V3 = +5.0\ V, V_{SS} = 0.0\ V, T_A = -40°C\ to\ +85°C)$

Parameter	Symbol	Pin	Condition	Value Min	Typ	Max	Unit	Remarks
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P25, P30 to P33, P40 to P45	—	$0.7\ V_{CC}$*1	—	$V_{CC} + 0.3$*1	V	
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, INT0, SCK, SI, PWC/INT1	—	$0.8\ V_{CC}$	—	$V_{CC} + 0.3$	V	
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P22 to P25, P30 to P33, P40 to P45	—	$V_{CC} - 0.3$	—	$0.3\ V_{CC}$*1	V	
	V_{ILS}	$\overline{RST}$, MOD0, MOD1, INT0, SCK, SI, PWC/INT1	—	$V_{SS} - 0.3$	—	$0.2\ V_{CC}$	V	
Open-drain output pin application voltage	V_D	P20 to P25, P00 to P07, P10 to P17	—	$V_{SS} - 0.3$	—	$V_{CC} + 6.0$	V	P00 to P07 and P10 to P17 (when selected as ports) for the MB89821/823R/825, and P20 to P25 without pull-up resistor
"H" level output voltage	V_{OH}	P40 to P45	$I_{OH} = -2\ mA$	2.4	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20 to P25, P40 to P45	$I_{OL} = 1.8\ mA$	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$	$I_{OL} = 4\ mA$	—	—	0.4	V	
Input leakage current (Hi-Z output leakage current)	I_{LI1}	MOD0, MOD1, P30 to P33, P40 to P45	$0.0\ V < V_I < V_{CC}$	—	—	±5	µA	Without pull-up resistor for the MB89821/823R/825
		MOD0, MOD1, P00 to P07, P10 to P17, P30 to P33, P40 to P45		—	—	±5	µA	Without pull-up resistor for the MB89P825/PV820
	I_{LI2}	P00 to P07, P10 to P17, P20 to P25	$0.0\ V < V_I < 6.0\ V$	—	—	±1	µA	Without pull-up resistor for the MB89821/823R/825
		P20 to P25		—	—	±1	µA	Without pull-up resistor for the MB89P825/PV820

(Continued)

(Continued)

$(V_{CC} = V3 = +5.0 \text{ V}, V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Pull-up resistance	R_{PULL}	P20 to P25, P30 to P33, P40 to P45, $\overline{RST}$	V1 = 0.0 V	25	50	100	kΩ	With pull-up resistor
Common output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = +5.0 V	—	—	2.5	kΩ	
Segment output impedance	R_{VSEG}	SEG0 to SEG49	V1 to V3 = +5.0 V	—	—	15	kΩ	
LCD divided resistance	R_{LCD}	—	Between V3 and V_{SS}	30	60	120	kΩ	
LCD leakage current	I_{LCDL}	V1 to V3, COM0 to COM3, SEG0 to SEG49	—	—	—	±1	µA	
Power supply current*2	I_{CC}	V_{CC}	$F_C = 5$ MHz t_{inst}*3 = 0.8 µs	—	3.5	5.0	mA	MB89821, MB89823R, MB89825, MB89PV820
				—	4.0	6.5	mA	MB89P825
	I_{CCS}		$F_C = 5$ MHz t_{inst}*3 = 0.8 µs Sleep mode	—	1.1	1.7	mA	MB89821, MB89823R, MB89825, MB89PV820, MB89P825
	I_{CCH}		$T_A = +25°C$ Stop mode	—	0.1	1	µA	MB89821, MB89823R, MB89825
				—	0.1	10	µA	MB89PV820, MB89P825
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

*1: The input voltage to P00 to P07 and P10 to P17 for the MB89P825/PV820 must not exceed the LCD power supply voltage (V3 pin voltage).

*2: The measurement condition of power supply current is as follows: the external clock, open output pins and the external LCD dividing resistor.
In the case of the MB89PV820, the current consumed by the connected EPROM and ICE is not included.

*3: For information on t_{inst}, see "(4) Instruction Cycle" in "4. AC Characteristics."

4. AC Characteristics

(1) Reset Timing

$(V_{CC} = +5.0 \text{ V} \pm 10\%, V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	**Max**		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{XCYL}	—	ns	

Notes : • t_{XCYL} is the main clock oscillator period.
  • If the reset pulse applied to the external reset pin ($\overline{RST}$) does not meet the specifications, it may cause malfunctions. Use caution so that the reset pulse less than the specifications will not be fed to the external reset pin ($\overline{RST}$) .
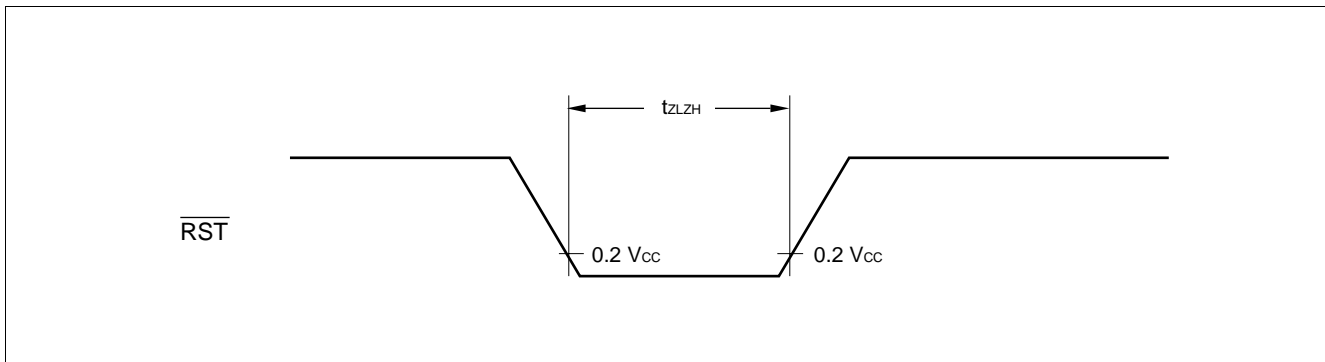
(2) Power-on Reset

$(V_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +85°C)$

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	**Max**		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
  If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.
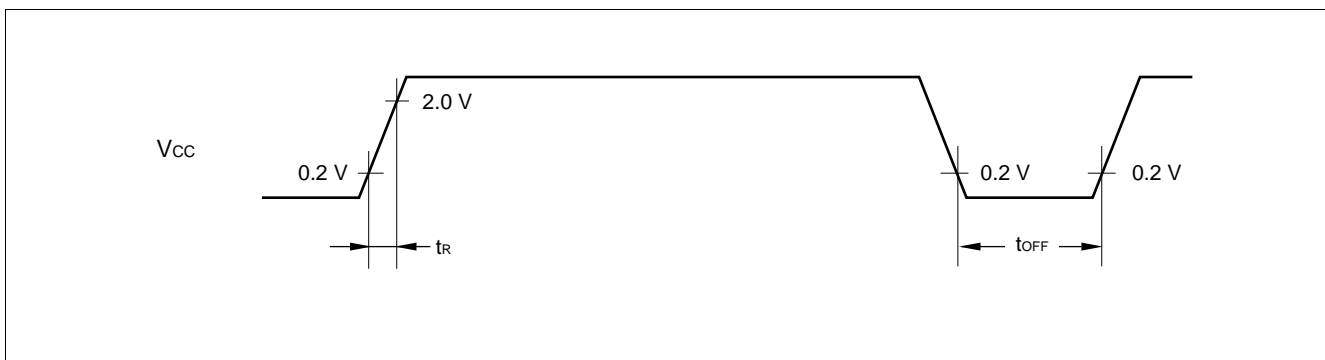
(3) Clock Timing

$(V_{SS} = 0.0\ V, T_A = -40°C\ to\ +85°C)$

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_C	X0, X1	—	1	—	5	MHz	
Clock cycle time	t_{XCYL}			200	—	1000	ns	Crystal or ceramic resonator
Input clock duty ratio*	duty	X0		30	—	70	%	External clock
Input clock rising/ falling time	t_{CR} t_{CF}			—	—	10	ns	External clock

*: duty = P_{WH}/t_{HCYL}, P_{WL}/t_{HCYL}

X0 and X1 Timing and Conditions

Clock Conditions

When a crystal or ceramic resonator is used

When an external clock in use
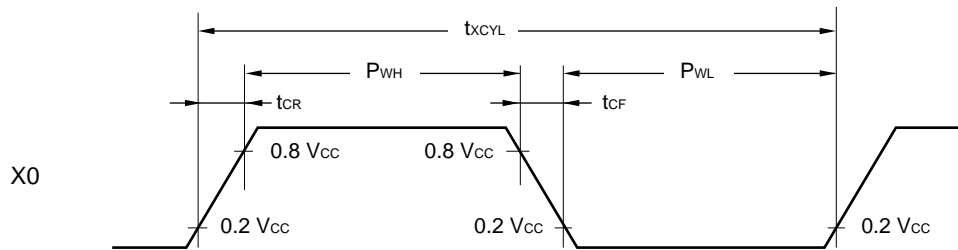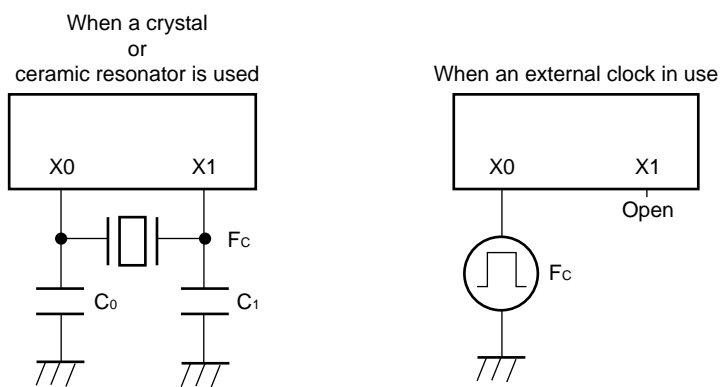
(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_C$	µs	$t_{inst} = 0.8$ µs when operating at $F_C = 5$ MHz

(5) Serial I/O Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

$(V_{CC} = +5.0\ V\pm10\%,\ V_{SS} = 0.0\ V,\ T_A = -40°C\ to\ +85°C)$

Parameter	Symbol	Pin	Condition	Value Min	Value Max	Unit	Remarks
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		−200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	
Serial clock "H" pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock "L" pulse width	t_{SLSH}			1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	

*: For information on t_{inst}, see "(4) Instruction Cycle."

(6) UART Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

$(V_{CC} = +5.0\ V\pm10\%,\ V_{SS} = 0.0\ V,\ T_A = -40°C\ to\ +85°C)$

Parameter	Symbol	Pin	Condition	Value Min	Value Max	Unit	Remarks
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		−200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	
Serial clock "H" pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock "L" pulse width	t_{SLSH}			1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	

*: For information on t_{inst}, see "(4) Instruction Cycle."

Internal Shift Clock Mode
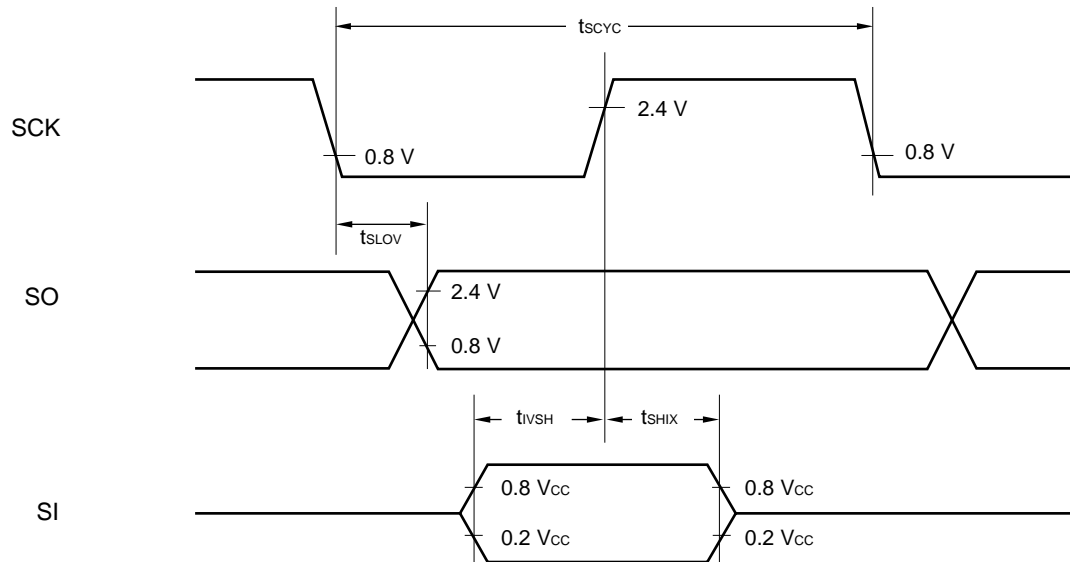
External Shift Clock Mode
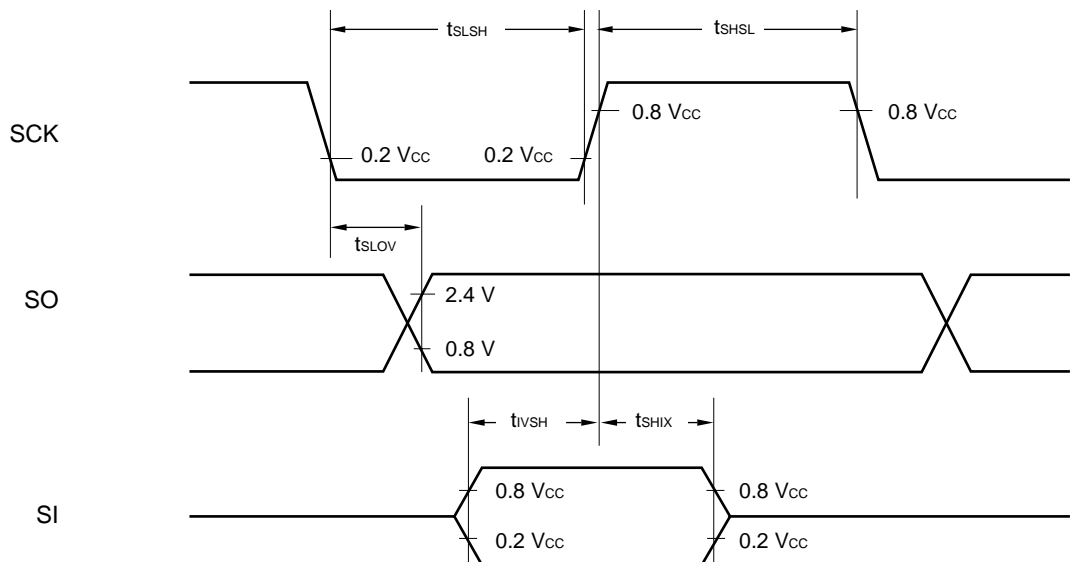
(7) Peripheral Input Timing

$(V_{CC} = +5.0\ V\pm10\%,\ V_{SS} = 0.0\ V,\ T_A = -40°C\ to\ +85°C)$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Peripheral input "H" pulse width	t_{ILIH}	PWC/INT1 INT0	—	$2\ t_{inst}$*	—	μs	
Peripheral input "L" pulse width	t_{IHIL}			$2\ t_{inst}$*	—	μs	

*: For information on t_{inst}, see "(4) Instruction Cycle."
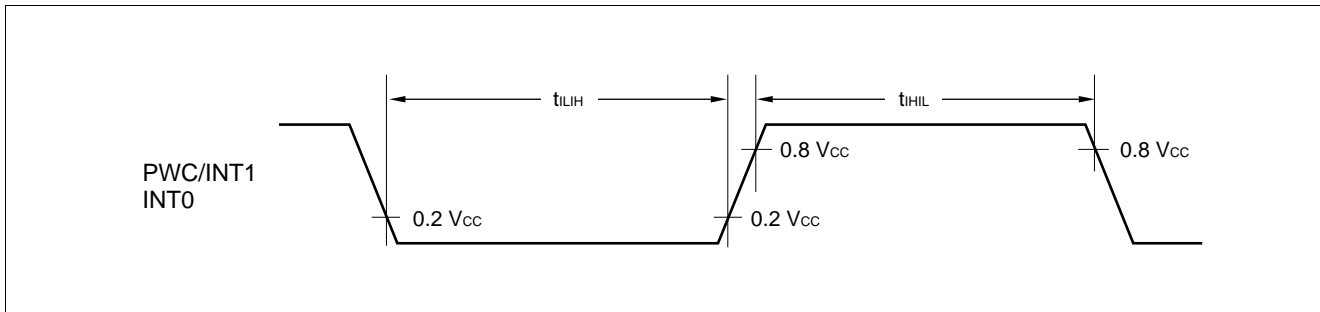
■ EXAMPLE CHARACTERISTICS

(1) "L" Level Output Voltage

V_{OL} vs. I_{OL}

V_{OL1} (V)
V_{CC} = 2.5 V
V_{CC} = 2.0 V V_{CC} = 3.0 V
T_A = +25°C
V_{CC} = 4.0 V
V_{CC} = 5.0 V
V_{CC} = 6.0 V

I_{OL} (mA)

(2) "H" Level Output Voltage

$V_{CC} - V_{OH}$ vs. I_{OH}

$V_{CC} - V_{OH}$ (V)
V_{CC} = 2.5 V
V_{CC} = 2.0 V V_{CC} = 3.0 V
T_A = +25°C
V_{CC} = 4.0 V
V_{CC} = 5.0 V
V_{CC} = 6.0 V

I_{OH} (mA)
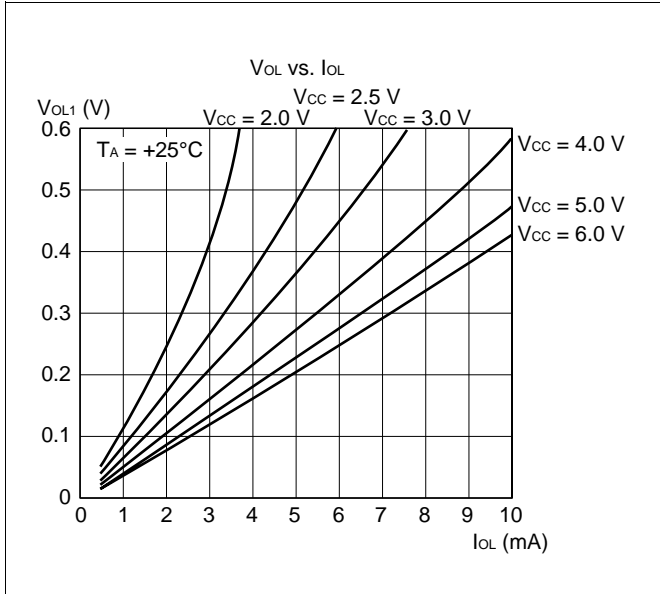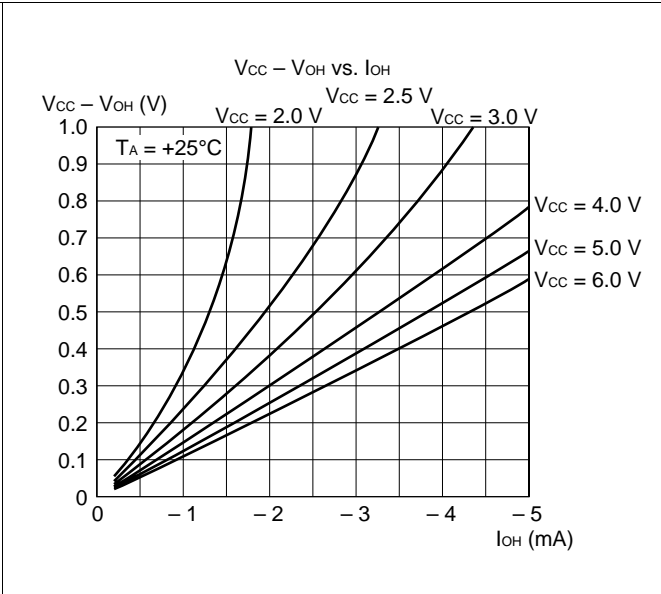
(3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)

V_{IN} vs. V_{CC}

V_{IN} (V)
T_A = +25°C

V_{CC} (V)
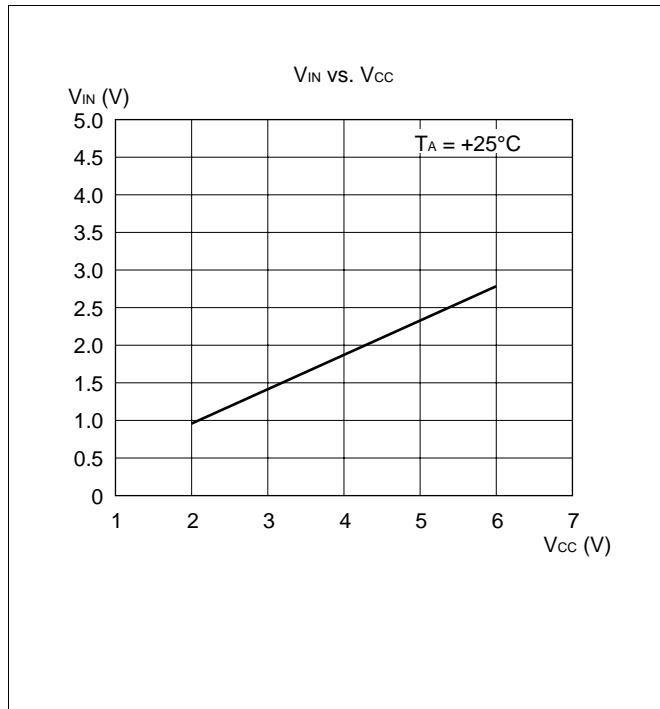
(4) "H" level Input Voltage/"L" Level Input Voltage (CMOS Hysteresis Input)

V_{IN} vs. V_{CC}

V_{IN} (V)
T_A = +25°C
V_{IHS}
V_{ILS}

V_{CC} (V)

V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to "H" level

V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to "L" level

33
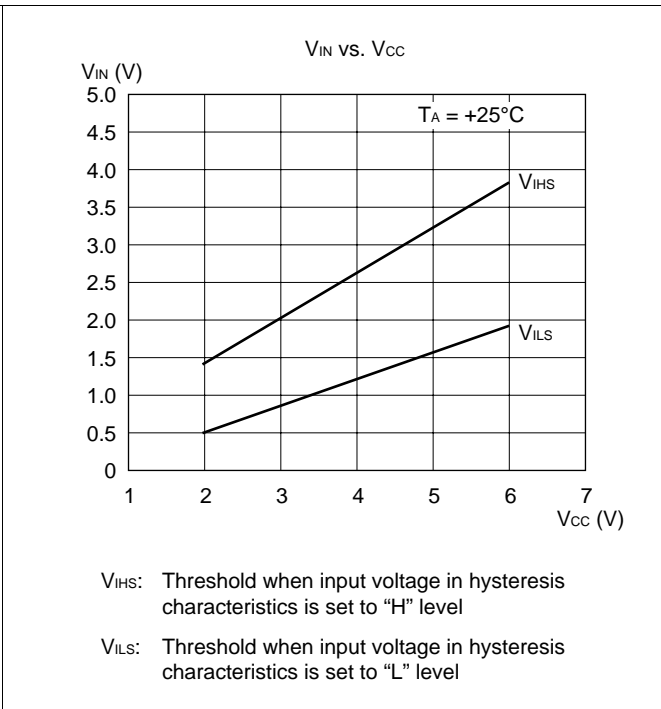
(5) Power Supply Current (External Clock)

I_{CC} vs. V_{CC}

I_{CC}(mA)

T_A = +25 °C
F_C = 5 MHz
F_C = 4.2 MHz
F_C = 3 MHz
F_C = 1 MHz

V_{CC} (V)

I_{CCS} vs. V_{CC}

I_{CCS} (mA)

T_A = +25 °C
F_C = 5 MHz
F_C = 4.2 MHz
F_C = 3 MHz
F_C = 1 MHz

V_{CC} (V)

(6) Pull-up Resistance

R_{PULL} vs. V_{CC}

R_{PULL} (kΩ)

T_A = +25 °C

V_{CC} (V)
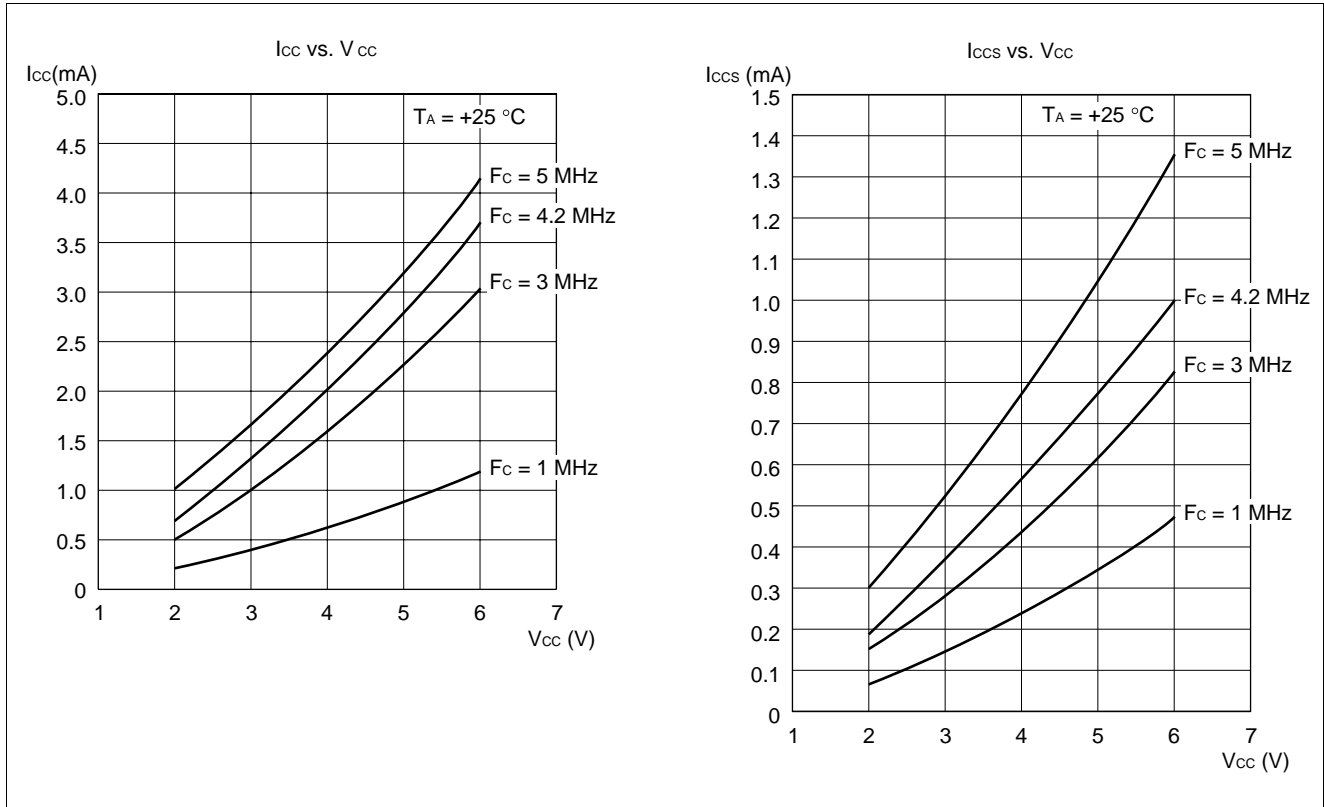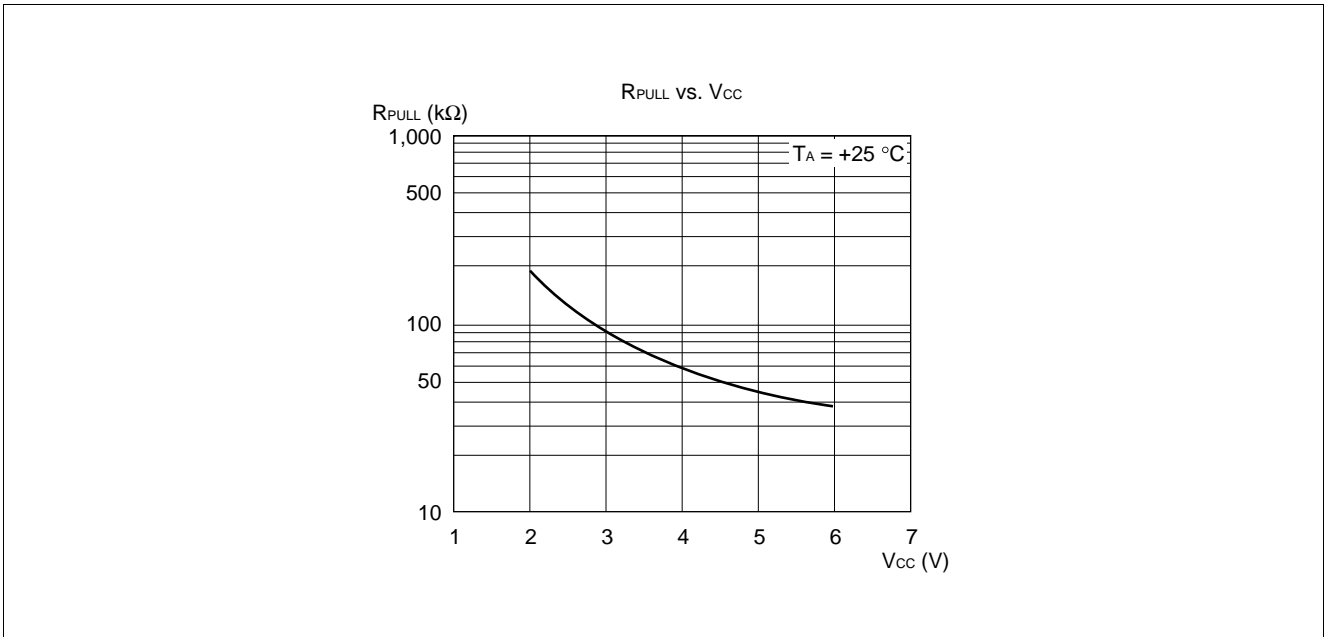
■ MASK OPTIONS

No.	Part number	MB89821/823R/825	MB89P825	MB89PV820
	Specifying procedure	Specify when ordering masking	Set with EPROM programmer	Setting not possible (Fixed)
1	Pull-up resistors P20 to P25, P30 to P33, P40 to P45	Selectable by pin	Can be set per pin	Without pull-up resistor

2	Power-on reset
	    With power-on reset
	    Without power-on reset
		Selectable	Can be set	With power-on reset

3	Oscillation stabilization time selection
	(F_C = 5 MHz)[*1]
	    Approx. $2^{18}/F_C$ (Approx. 52.4 ms)
	    Approx. $2^{14}/F_C$ (Approx. 3.28 ms)
		Selectable	Can be set	Oscillation stabilization time Approx. $2^{18}/F_C$ (Approx. 52.4 ms)

4	Reset pin output
	    With reset output
	    Without reset output
		Selectable	Can be set	With reset output

5	Segment output switching
	    50 segments: No port selection
	    49 segments: Selection of P17
	    48 segments: Selection of P17 to P16
	    46 segments: Selection of P17 to P14
	    42 segments: Selection of P17 to P10
	    34 segments: Selection of P17 to P10
	                  and P07 to P00
		Selectable[*2]	Can be set[*3]	Can be set[*3]

*1: The oscillation settling time is generated by dividing the oscillation clock frequency. Since the oscillation period is not stable immediately after oscillation has been started, therefore, the oscillation settling time in the above list should be regarded as a reference.

*2: Port selection must be same setting of the segment output selection register of LCD controller.

*3: Note that, when ports are set, the input voltage value for the port pins are different from those for mask ROM products.
Ports are set by the register setting of the segment output selection register of LCD controller.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89821PFM MB89823RPFM MB89825PFM MB89P825PFM	80-pin Plastic QFP (FPT-80P-M11)	
MB89PV820CF	80-pin Ceramic MQFP (MQP-80C-P01)	

■ PACKAGE DIMENSIONS

80-pin Plastic QFP
(FPT-80P-M11)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

16.00±0.20(.630±.008)SQ

*14.00±0.10(.551±.004)SQ

60   41

61   40

INDEX

80   21

1   20

0.65(.026)

0.32±0.05
(.013±.002)

⊕ 0.13(.005) Ⓜ

0.145±0.055
(.006±.002)

⌂ 0.10(.004)

"A"

Details of "A" part

$1.50\,^{+0.20}_{-0.10}\,(.059\,^{+.008}_{-.004})$
(Mounting height)

0.25(.010)

0~8°

0.50±0.20
(.020±.008)

0.60±0.15
(.024±.006)

0.10±0.10
(.004±.004)
(Stand off)
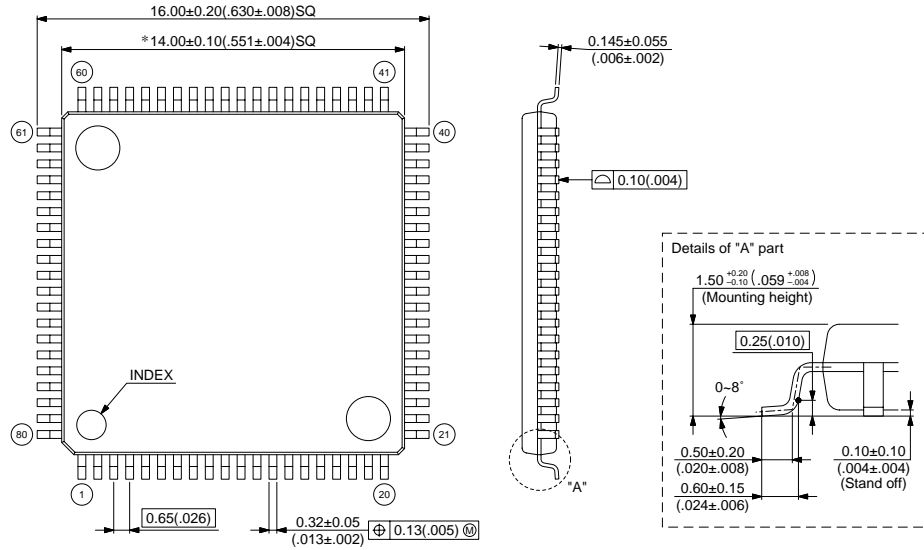
© 2003 FUJITSU LIMITED F80016S-c-3-6

Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

(Continued)

(Continued)

80-pin Ceramic MQFP
(MQP-80C-P01)
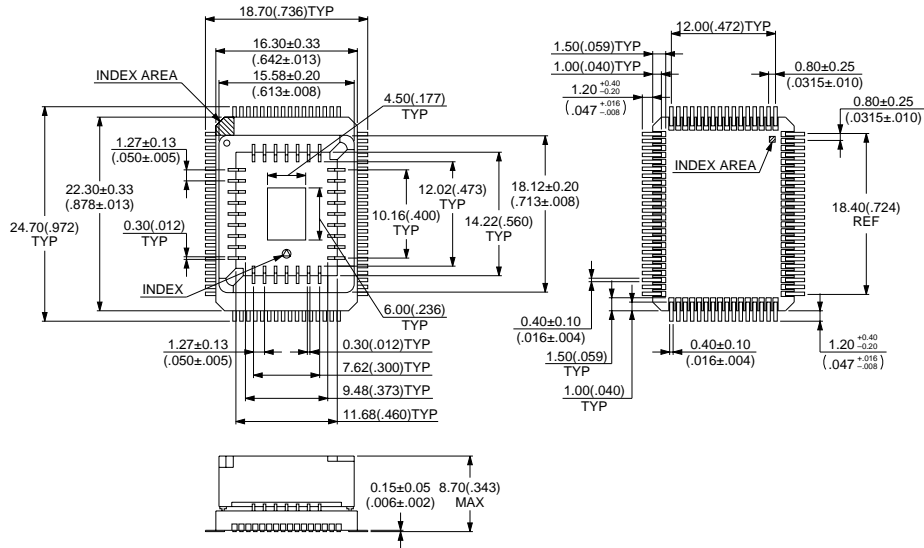
© 1994 FUJITSU LIMITED M80001SC-4-2

Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

FUJITSU LIMITED