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MOTOROLA

MC33143

Advance Information

Dual High-Side Switch

The MC33143 is a dual high–side switch designed for solenoid control in harsh automotive applications, but is well suited for other environments. The device can also be used to control small motors and relays as well as solenoids. The MC33143 incorporates SMARTMOS™ technology, with CMOS logic, bipolar/MOS analog circuitry, and DMOS power outputs. An internal charge pump is incorporated for efficient gate enhancement of the internal high–side power output devices. The outputs are designed to provide current to low impedance solenoids. The MC33143 provides individual output fault status reporting along with internal Overcurrent and Over Temperature protection. The device also has Overvoltage protection, with automatic recovery, which "globally" disables both outputs for the duration of an Overvoltage condition. Each output has individual Overcurrent and Over Temperature shutdown with automatic retry recovery. Outputs are enabled with a CMOS logic high signal applied to an input to providing true logic control. The outputs, when turned on, provide full supply (battery) voltage across the solenoid coil.

The MC33143 is packaged in an economical 24 pin surface mount power package and specified over an operating voltage of 5.5 V ≤ V_{Pwr} < 26 V for –40°C ≤ T_A ≤ 125°C.

- Designed to Operate Over Wide Supply Voltages of 5.5 V to 26 V
- Dual High–Side Outputs Clamped to –10 V for Driving Inductive Loads
- Internal Charge Pump for Enhanced Gate Drive
- Interfaces Directly to a Microcontroller with Parallel Input Control
- Outputs Current Limited to 3.0 A to 6.0 A for Driving Incandescent Loads
- Chip Enable "Sleep Mode" for Power Conservation
- Individual Output Status Reporting
- Fault Interrupt Output for System Interrupt Use
- Output ON or OFF Open Load Detection
- Overvoltage Detection and Shutdown
- Output Over Temperature Detection and Shutdown with Automatic Retry
- Sustained Current Limit or Immediate Overcurrent Shutdown Output Modes
- Output Short to Ground Detection and Shutdown with Automatic Retry
- Output Short to V_{Pwr} Detection

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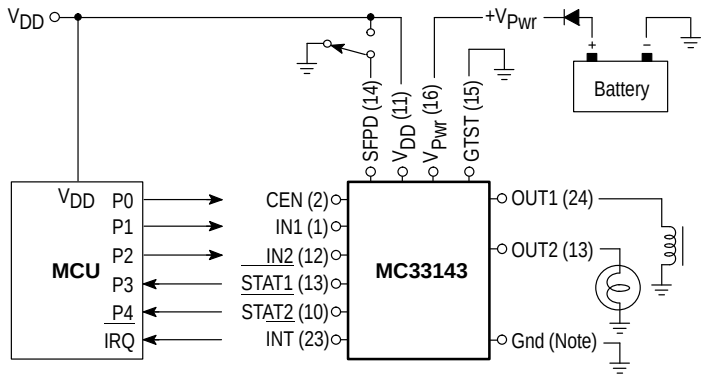
Simplified Application

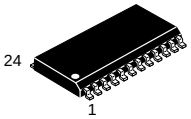


NOTE: Pins 5, 6, 7, 8, 17, 18, 19 and 20 provide electrical ground and heatsinking.

This device contains 889 active transistors.

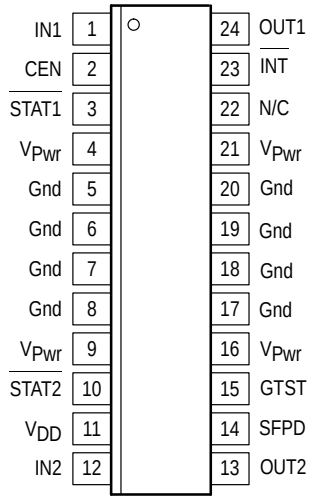
DUAL HIGH–SIDE SWITCH

SEMICONDUCTOR TECHNICAL DATA



DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SOP (16+4+4)L)

PIN CONNECTIONS



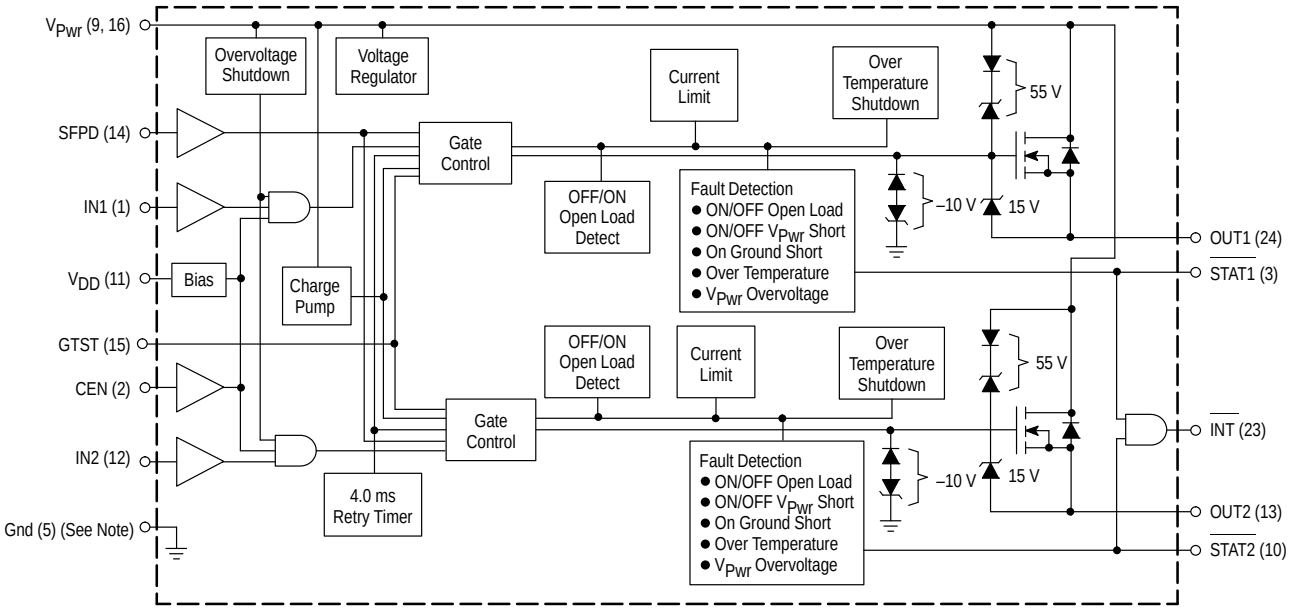
(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33143DW	T_A = – 40° to +125°C	SOP–24L

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Figure 1. Simplified Internal Block Diagram



NOTE: Pins 5, 6, 7, 8, 17, 18, 19 and 20 should all be grounded so as to provide electrical as well as thermal heatsinking of the device.

MAXIMUM RATINGS (All voltages are with respect to ground, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage Steady State Continuous Operation Negative Transient (Note 1) Positive Load Dump Transient (Note 2)	V_{Pwr}	 26 –1.5 60	V
Logic Supply Voltage Range	V_{DD}	–0.3 to 7.0	V
Logic Supply Current	I_{DD}	5.0	mA
Input Voltage (Note 3)	V_{in}	–0.3 to 7.0	V
Output Clamp Voltage I_O = –20 mA I_O = –200 mA	V_{Clamp}	 –3.0 to –20 –5.5 to –20	V
Output Current Limit (Note 4)	$I_{O(Lim)}$	–3.0 to –6.0	A
Output Clamp Energy (I_O = –1.0 A) T_J = 25°C T_J = 125°C	E_{Clamp}	 300 100	mJ
ESD (Minimum) Human Body Model (Note 5) Machine Model (Note 6)	 HBM MM	 2000 200	V
Power Dissipation (T_A = 25°C) (Note 7)	P_D	4.2	W
Operating Temperature (Note 8)	T_A	–40 to +125	°C
Operating Junction Temperature	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Soldering Temperature (for 10 Seconds)	T_{solder}	270	°C
Thermal Resistance Junction–to–Lead Junction–to–Ambient	 $R_{\theta JL}$ $R_{\theta JA}$	 15 30	°C/W

NOTES:
1. Negative transient survival capability for 100 ms time duration.
2. Positive transient survival capability with typical automotive load dump condition; 400 ms time constant decay.
3. All input pins (IN1–2, CEN and SFPD).
4. Each output has independent current limiting.
5. Performed in accordance to HBM; C_{Zap} = 100 pF, R_{Zap} = 1500 Ω.
6. Performed in accordance to MM; C_{Zap} = 100 pF, R_{Zap} = 0 Ω.
7. Derate Power Dissipation 33 mW/°C for temperatures above 25°C.
8. Ambient temperature is given as a practical reference; Maximum junction temperature is the limiting factor.
9. ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions 9.0 V ≤ V_{Pwr} ≤ 17 V, 4.5 V ≤ V_{DD} 5.5 V, –40°C ≤ T_L ≤ 125°C, unless otherwise noted, typical values represent approximate mean at T_L = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Range (Operational)	V_{Pwr}	9.0	–	17	V
Supply Current (Note 1) Both Outputs ON (CEN = IN1 = IN2 = 0.7 x V_{DD}, I_{O1} = I_{O2} = –1.0 A) Standby (CEN = 0.7 x V_{DD}, IN1 = IN2 = 0.3 x V_{DD}, R_L = 12 Ω) "Sleep State" (CEN = IN1 = IN2 = 0.3 x V_{DD}, R_L = 12 Ω)	 I_{Pwr} $I_{Pwr(sby)}$ $I_{Pwr(sleep)}$	 0.1 – –	 4.2 3.9 0.2	 7.0 7.0 300	 mA mA μA
Logic Supply Voltage Range	V_{DD}	4.5	–	5.5	V
Logic Supply Current Both Outputs ON (IN1 = IN2 = 0.7 x V_{DD}, I_{O1} = I_{O2} = –1.0 A)	I_{DD}	–	0.43	5.0	mA
Overvoltage Shutdown (Note 2)	$V_{Pwr(ovsd)}$	30	33.2	38	V
Overvoltage Shutdown Hysteresis	$V_{Pwr(hys)}$	0.3	0.5	1.5	V

NOTES: 1. Supply current when both outputs are ON and during standby are measured in the Ground pin while during "sleep state" is measured in the V_{Pwr} pin.
2. Overvoltage Shutdown causes enabled outputs to be forced OFF; Overvoltage fault is immediately reported.

DC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions 9.0 V ≤ V_{Pwr} ≤ 17 V, 4.5 V ≤ V_{DD} 5.5 V, –40°C ≤ T_L ≤ 125°C, unless otherwise noted, typical values represent approximate mean at T_L = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT					
Drain–to–Source ON Resistance (Note 1) (T_J = 25°C, CEN = IN1 = IN2 = 0.7 x V_{DD}) I_O = –0.5 A. V_{Pwr} = 5.5 V I_O = –1.0 A. V_{Pwr} = 14 V I_O = –2.0 A. V_{Pwr} = 24 V	$R_{DS(on)}$	 – – –	 0.2 0.14 0.14	 0.5 0.2 0.2	Ω
Drain–to–Source ON Resistance (Note 1) (T_J = 125°C, CEN = IN1 = IN2 = 0.7 x V_{DD}) I_O = –0.5 A. V_{Pwr} = 5.5 V I_O = –1.0 A. V_{Pwr} = 14 V I_O = –2.0 A. V_{Pwr} = 24 V	$R_{DS(on)}$	 – – –	 – – –	 1.0 0.38 0.38	Ω
Output Self–Limiting Current (Note 2) (CEN = IN1 = IN2 = SFPD = 0.7 x V_{DD}, R_L = 0 Ω)	$I_{O(Lim)}$	–3.0	–4.1	–6.0	A
Output OFF Leakage Current (CEN = 0.7 x V_{DD}, IN1 = IN2 = 0.3 x V_{DD})	$I_{O(Lkg)}$	–5.0	–45	–150	μA
Output OFF Open Load Sense Current (CEN = 0.7 x V_{DD}, IN1 = IN2 = 0.3 x V_{DD})	$I_{O(Sense)}$	–5.0	–45	–150	μA
Output ON Open Load Detection Current (Note 3) (CEN = IN1 = IN2 = 0.7 x V_{DD}) T_L = –40°C T_L = 125°C	$I_{O(On)}$	 –2.0 –2.0	 –145 –181	 –200 –200	mA
Output Clamp Voltage (Note 4) (CEN = 0.7 x V_{DD}, IN1 = IN2 = 0.3 x V_{DD}) I_O = –20 mA I_O = –200 mA	V_{Clamp}	 –9.0 –9.0	 –13.2 –13.5	 –20 –20	V
Over Temperature Shutdown Range (Note 5) (CEN = IN1 = IN2 = SFPD = 0.7 x V_{DD})	T_{Lim}	155	–	185	°C
Over Temperature Shutdown Hysteresis (Note 6)	$T_{Lim(hys)}$	–	–	15	°C

NOTES: 1. $R_{DS(on)}$ applies to OUT1, OUT2 and is independent of output current.
2. Applies to each output; each output has independent self–limiting source current feature; Over Current and Short–to–Ground defined as condition when output source current exceeds $I_{O(Lim)}$; Device ignores Over Current and Short–to–Ground faults from 0 to t_{SS}.
3. Applies to each output; tested for by ramping I_O from 0 until STAT ≤ 0.7 x V_{DD}; defined as the condition when I_O is outside of $I_{O(on)}$ current window.
4. Applies to each output; each output has independent dynamic output voltage clamping feature.
5. Applies to each output; each output has independent thermal shutdown; parameter is measured by ramping temperature until enabled output is disabled; parameter is established by design but is not production tested; thermal fault is immediately reported.
6. Parameter is established by design but is not production tested.

DC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions 9.0 V ≤ V_{Pwr} ≤ 17 V, 4.5 V ≤ V_{DD} 5.5 V, –40°C ≤ T_L ≤ 125°C, unless otherwise noted, typical values represent approximate mean at T_L = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL INTERFACE					
Input Control					V_{DD}
Logic High (I_O = –0.1 A) (Note 1)	V_{IH}	0.7	0.56	–	
Logic Low (I_O = 0) (Note 2)	V_{IL}	–	0.52	0.3	
Input Logic Voltage Hysteresis ($V_{IH} – V_{IL}$)	V_{hys}	50	250	500	mV
Input Pull–Down Current (0.3 x V_{DD} ≤ V_{in} < 0.7 x V_{DD}) (Note 3)	$I_{in(pd)}$	20	44	100	µA
Chip–Enable Threshold					V_{DD}
Logic Low (Note 4)	$V_{CEN(IL)}$	–	0.5	0.3	
Logic High (Note 5)	$V_{CEN(IH)}$	0.7	0.5	–	
Chip–Enable Hysteresis ($V_{CEN(IH)} – V_{CEN(IL)}$)	$V_{CEN(hys)}$	50	150	500	mV
Chip–Enable Pull–Up Current (CEN = 0.7 x V_{DD})	$I_{CEN(pu)}$	–2.0	–16.8	–40	µA
Status Low Voltage (I_{in} = 600 µA) (Note 6)	$V_{\overline{STAT}(low)}$	–	0.07	0.2	V_{DD}
Status Pull–Up Current (Note 7)	$I_{\overline{STAT}(pu)}$	–20	–44	–100	µA
Interrupt (Note 8)					V_{DD}
Logic High	$\overline{INT}_h$	0.7	–	–	
Logic Low	INT_l	–	–	0.3	

NOTES: 1. Upper logic threshold voltage applies to IN1, IN2, and SFPD and expressed in V_{DD} units

2. Lower logic threshold voltage applies to IN1, IN2, and SFPD and expressed in V_{DD} units.

3. Applies to IN1, IN2, and SFPD.

4. Initially have CEN = 0.7 x V_{DD}, Ramp CEN down from V_{DD} until I_O = 0 and note disabling point.

5. Initially have V_{in} = 0.7 x V_{DD}, Ramp CEN up from ground until I_O = 0.1 A and note enabling point.

6. Applies equally to STAT1–2 and INT outputs; Measured threshold voltage by applying an "open" fault to OUT1 or OUT2 while forcing 600 µA of current into STAT1–2 or INT.

7. Measured with no faults on OUT1–2, $V_{\overline{STAT}} = V_{\overline{INT}}$ = 0.8 x V_{DD}.

8. The Interrupt output has an internal active current pull–up.

DC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions 9.0 V ≤ V_{Pwr} ≤ 17 V, 4.5 V ≤ V_{DD} 5.5 V, –40°C ≤ T_L ≤ 125°C, unless otherwise noted, typical values represent approximate mean at T_L = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT DYNAMICS					
Output Short Sense Time (Note 1)	t_{ss}	30	54	100	µs
Output Short Refresh Time (Note 2)	t_{ref}	3.0	4.1	6.0	ms
Output Open Sense ON Time (Note 3)	$t_{os(on)}$	3.0	6.4	12	ms
Output Propagation Delay					µs
Turn–On (Output Low to High) (Note 4)	t_{dlh}	–	7.2	50	
Turn–Off (Output High to Low) (Note 5)	t_{dhl}	–	40	75	
Output Slew Rate					V/µs
Output Rising (Note 6)	SR_r	0.2	11	10	
Output Falling (Note 7)	SR_f	0.2	2.6	10	

NOTES: 1. CEN = 0.7 x V_{DD}, SFPD = 0.3 x V_{DD}, R_L = 0, Step V_{in} from 0.3 x V_{DD} to 0.7 x V_{DD}; Sense time measured from step until $\overline{STAT}$ = 0.2 x V_{DD}.

2. CEN = IN1 = IN2 = 0.7 x V_{DD}, R_L = 0; Refresh time measured from output disable until output is re–enabled.

3. R_L = "open", Step V_{in} from ground to 0.7 x V_{DD}, Open sense time measured from step until $V_{\overline{STAT}} \le$ 0.2 x V_{DD}.

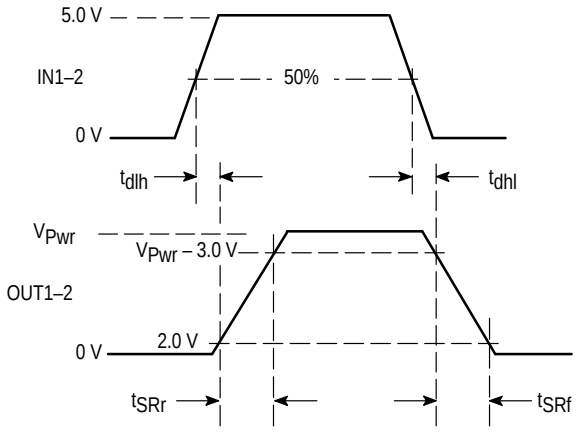
4. R_L = 12 Ω, C_L = 0.01 µF, step V_{in} from V_{IL} to V_{IH}; Turn–On propagation measured from V_{in} = 0.5 x V_{DD} until V_{out} = 2.0 V (see Figure 2).

5. R_L = 12 Ω, C_L = 0.01 µF, step V_{in} from V_{IH} to V_{IL}; Turn–Off propagation measured from V_{out} = V_{Pwr} –3.0 V until V_{out} = 2.0 V (see Figure 2).

6. R_L = 12 Ω, C_L = 0.01 µF, step V_{in} from V_{IL} to V_{IH}; Output Slew Rate measured from 2.0 V to V_{Pwr} – 3.0 V (see Figure 2).

7. R_L = 12 Ω, C_L = 0.01 µF, step V_{in} from V_{IH} to V_{IL}; Output Slew Rate measured from V_{Pwr} – 3.0 V to 2.0 V (see Figure 2).

Figure 2. Output Response Waveform



PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1, 12	IN1, IN2	INput 1 and INput 2 (IN1 and IN2) respectively determine the state of the corresponding output drivers (OUT1 and OUT2) under normal operating conditions. When an input is high, it's corresponding output is active ON, and when low is disabled OFF. IN1 and IN2 have internal active pull–downs which allow a floating input pin to be conservatively interpreted as a logic low, turning Off the output. An unused input should be connected to ground.
2	CEN	Chip Enable (CEN) input pin, when low, disables both outputs (OUT1 and OUT2) and places the device in a "sleep mode" reducing the bias current required from V_{DD} and V_{Pwr}. A falling edge of CEN causes OUT1 and OUT2 to rapidly turn OFF. A falling edge of CEN should precede any V_{DD} shutdown to allow time OUT1 and OUT2 to be disabled. When CEN is low, INTerrupt (INT) and STATus 1 and 2 (STAT1–2) will be tri–stated (high impedance). The CEN pin can also be used for power–on reset and under voltage lockout to disable the outputs for power supply voltages less than 4.5 V. CEN is a dependent input from the system microcontroller unit (MCU) or some other integrated circuit. It has an internal pull–up resistor to V_{DD} affording a floating pin to be interpreted as a logic high. $R_{pull–up}$ is greater than 50 kΩ. If used externally, this pin should be connected to V_{DD}.
3, 10	$\overline{STAT1}$. $\overline{STAT2}$	The STATus pins (STAT1–2) respectively indicate the presence of faults on OUT1–2. STAT1–2 will be logic high during normal operation. A logic low will occur whenever an Open Load, Short–to–Ground, Short–to–Supply (Battery), Thermal Limit, or Overvoltage Shutdown fault condition is experienced on a corresponding output. STAT1–2 are both active low digital drivers. A 10 kΩ resistor between STAT1–2 and the system CPU may improve a Failure Mode Evaluation Analysis (FMEA) score if STAT1–2 are externally shorted to V_{Pwr}. If unused, this pin should be left connected.
4, 9, 16, 21	V_{Pwr}	These pins are connected to the supply and provide load current to the DMOS outputs, are used pumping the DMOS gates, and for Overvoltage shutdown detection of the DMOS. The DMOS outputs will turn ON with 5.5 to 24 V applied to V_{Pwr}. V_{Pwr} is limited to –1.5 V for a maximum duration of 250 ms. A 10 nF de–coupling cap is recommended to be used from V_{Pwr} to Ground.
5, 6, 7, 8, 17, 18, 19, 20	Gnd	These eight pins constitute the circuits ground (Gnd) and also provide heatsinking for the DMOS output transistors. Ground continuity is required for the outputs2 to turn ON.
11	V_{DD}	This pin is to be connected to the 5.0 V logic supply of the system. A 10 nF de–coupling capacitor is recommended from V_{DD} to Gnd.
13, 24	OUT1, OUT2	These pins are connected internally to the DMOS output transistors which source current into the corresponding load. Each output incorporates dynamic clamping to accommodate inductive loads. In addition, each output has independent short to ground detection and protection, current limit detection and protection, thermal limit detection and protection, ON open load and or short to supply (battery) detection. Neither output will turn ON if CEN is logic low. An unused output should be connected to a 10 kΩ load to prevent false fault reporting. A 1.0 nF filter capacitor may be used from OUT to Gnd to provide dV/dt noise filtering.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Description
14	SFPD	This is a Short Fault Protect Disable (SFPD) input; which when logic high disables the internal current limit timer preventing OUT1–2 from latching OFF when confronted with an overcurrent condition. The condition of SFPD does not affect fault reporting. Current and thermal limit remain active when the SFPD pin is logic high. Having the SFPD pin logic high facilitates the device to drive incandescent lamp loads with peak in–rush currents in excess of three amperes. When SFPD is logic low, an overcurrent demand will latch OFF only the output affected. The device will then automatically begin active re–enabling of the corresponding output affected for the duration of the overcurrent condition. SFPD has an internal active pull–down which affords a floating input pin condition to be conservatively interpreted as a logic low. A 10 kΩ resistor between SFPD and the system CPU may improve the FMEA score if SFPD is externally shorted to OUT2. SFPD should be connected to Gnd or V_{DD} for the desired operating mode and not be left “floating”.
15	GTST	The Gate TeST (GTST) pin is used to stress the devices DMOS gates during testing operations. This pin should normally be connected to ground in the application.
23	$\overline{INT}$	The INTerrupt pin $\overline{INT}$ is active logic low and indicates the presence of a fault on either the output. $\overline{INT}$ can be paralleled with additional fault pins and used as a system CPU interrupt to indicate the presence of a fault. The system CPU can then read STAT1–2 to determine the specific type of fault occurring. $\overline{INT}$ will be logic high during normal operation. A logic low will result if a fault occurs on either OUT1 or OUT2. $\overline{INT}$ has an internal active pull–up and requires no external pull–up resistor to be used. The $\overline{INT}$ output has sufficient current drive capability to afford paralleling of up to five $\overline{INT}$ pins. A 10 kΩ resistor between $\overline{INT}$ and the system CPU may improve the FMEA score if $\overline{INT}$ is externally shorted to OUT1. This pin should be left unconnected if the feature is not used.

Figure 3. Function Table

Device Condition	In	Out	$\overline{STAT}$	Output Condition	$\overline{STAT}$ Condition
Normal	Low High	Low High	High High	Normal OFF Normal ON	Normal Normal
Output to Gnd Short	Low	Low	High	Normal OFF	Normal
	High	High/Low	Low	Output in active retry mode. Normal ON when short is removed.	Short fault reported. Fault clears when short is removed.
Open Load	Low	High	Low	Normal OFF	“OFF” open fault reported. Fault clears when load is connected.
	High	High	Low	Normal ON	“ON” open fault reported. Fault clears when load is connected.
Output to V_{Pwr} Short	Low	High	Low	Normal OFF	“OFF” open fault reported. Fault clears when short is removed.
	HIgh	High	Low	Normal ON	“ON” open fault reported. Fault clears when short is removed.
Over Temperature	Low	Low	Low	Normal OFF	Thermal fault reported. Fault clears with no thermal limit.
	High	Low	Low	Output disabled. Output Retries with no thermal limit.	Thermal fault reported. IN low and no thermal limit required to clear the fault.
V_{Pwr} Overvoltage	Low	Low	Low	Normal OFF	Overvoltage fault reported. Fault clears with no overvoltage.
	High	Low	Low	Output disabled. Will reset with no overvoltage.	Overvoltage fault reported. Fault clears with no overvoltage.
“Sleep”/Under Voltage Mode, CEN Low	Low	Low	High–Z	Output disabled.	STAT tri–stated, no faults reported.
	High	Low	High–Z	Output disabled.	STAT tri–stated, no faults reported.

FUNCTIONAL DESCRIPTION

General

The MC33143 is designed as an interface device; between system's electronic control unit and the actuators. It is designed to withstand several abnormal operating conditions, with the capability of reporting it's operating status back to the control unit. The MC33143 will resume normal operation after having experienced 60 V transients on the V_{Pwr} line, output shorts to V_{Pwr}, open loads, output shorts to ground, over current, over temperature, or overvoltage conditions. Status information is available when ever a load experiences any of the faults. In addition, the MC33143 device incorporates internal output transient clamps allowing it to control inductive loads and survive negative voltage spikes without the need of external components.

Power Supply Voltage Requirements

The MC33143 is designed to operate with 5.5 V to 26 V applied to the power supply pin (V_{Pwr}) and 4.5 V to 5.5 V applied to the logic supply pin (V_{DD}). If V_{Pwr} is above the specified Overvoltage Shutdown voltage limit ($V_{Pwr(ovsd)}$) the outputs will be disabled and the status line voltage will transition to a low logic state indicating a fault.

When the CEN voltage is at a low logic state, OUT1 and OUT2 will turn OFF. This provides an under voltage shutdown for V_{Pwr} in the 0 to 4.5 V range. The active low under voltage must be externally provided to the CEN pin.

The MC33143 is designed to survive the loss of V_{Pwr}.

Normal Operations

The MC33143 is considered to be operating normal when the following conditions are met:

1) 5.5 V ≤ V_{Pwr} ≤ 26 V.
2) –40°C ≤ TJ ≤ 150°C.
3) When load currents (I_O) exceed the Output Open "ON" detection current ($I_{O(on)}$) and occur within the Open Sense "ON" time ($t_{os(on)}$) window.
4) When load currents (I_O) are less than the Output Limit Current ($I_{O(Lim)}$) for durations in excess of the Short Sense time (t_{SS}).
5) So long as the output of the device is able to clamp negative voltages produced when switching inductive loads to the specified clamp voltage (V_{Clamp}).

Fault Conditions

Anytime the MC33143 is not operating normal it is said to be operating in a "faulted condition". Fault conditions will result in level changes of the status outputs (STAT1–2) and disable the affected faulted output.

Output Over Current/Short to Ground Faults

For an enabled input, the status line voltage will transition to a low logic level if the output current equals or exceeds the Output Limit current ($I_{O(Lim)}$) for a period of time in excess of the Short Sense time (t_{SS}). Only the affected output will turn off; independent of the corresponding input's condition. The device incorporates an internal short duration Refresh timer (t_{ref}) to mask edge transients due to switching noise. The output will remain off for the short t_{ref} duration and then attempt to re–energize the shorted load. The internal protection circuitry continues to be active during this process. If the short is not removed; the circuitry will sequence and the output will remain off for a another t_{ref} time. This process will continue so long as the output remains shorted and the input remains in a logic high state. If the short is removed from the output, while the input is ON, the MC33143 will return to normal operation and the status line will go to a logic high state after the t_{ref} time–out. The status line will also go to a logic high state on the falling edge of the corresponding input.

Open Load/Short to V_{Pwr} Fault

This condition is commonly referred to as an "ON" open fault. For this fault to be present, the output current of the driver must be at or near zero. Since the MC33143 is a "high–side switch"; It is for this reason a Short to V_{Pwr} fault resembles an Open Load fault, in so far as the MC33143 is concerned. When this fault is present the status line voltage will transition to a low logic level so long as the output current does not exceed the specified Open ON detection current ($I_{O(on)}$) for a duration in excess of the specified Open Sense ON time ($t_{os(on)}$). If the open load or output short to V_{Pwr} condition is removed, and the corresponding input is at a logic high state, the status line voltage will go to a logic high state after the drain current has exceeded $I_{O(on)}$. The ON open fault detection circuit incorporates a voltage comparator which monitors the voltage difference from V_{Pwr} to OUT. When ever the V_{Pwr} to OUT voltage difference falls below 10 mV an ON Open fault is reported. A Short to V_{Pwr} external to any module the MC33143 is in will not be detected as an ON Open fault if the voltage difference from V_{Pwr} to OUT is greater than 10 mV. V_{Pwr} line voltage drops directly impact this detection ability.

Overvoltage Fault

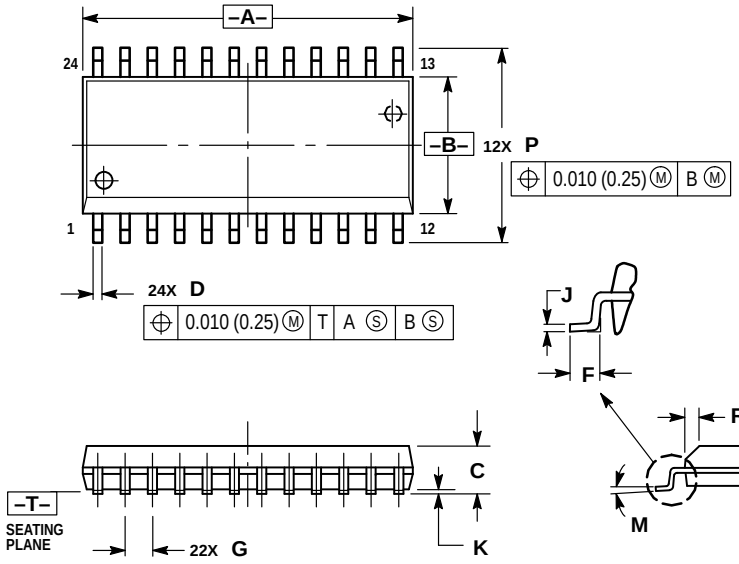
When this fault is present the status line voltage will transition to a logic low state when V_{Pwr} exceeds the specified Overvoltage Shutdown threshold $V_{Pwr(ovsd)}$. This fault produces a "global" response on the part of the MC33143 by turning OFF both outputs independent of input conditions. The outputs will resume normal operation when V_{Pwr} drops the specified Overvoltage Hysteresis $V_{Pwr(hys)}$ value.

Over Temperature Fault

When this fault is present the status line voltage transitions to a low logic level when the junction temperature of either output exceeds the specified Thermal Limit threshold (T_{Lim}). Only the specific faulted output will shutdown independent of the input condition. The other output will continue to operate in a normal fashion unless it also becomes faulted. The thermally faulted output will resume normal operation when the junction temperature drops the specified Over Temperature Shutdown Hysteresis ($T_{Lim(hys)}$) amount.

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC PACKAGE
CASE 751E–04
(SOP (16+4+4)L)
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0 °	8 °	0 °	8 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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