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TECHNICAL DATA

MC68HC711J6

Technical Summary
8-Bit Microcontroller

Introduction

The MC68HC711J6 is a member of the HC11 series of microcontrollers (MCU) and has been designed for applications that require additional input/output (I/O) ports and more erasable programmable, or one-time programmable ROM (EPROM or OTPROM). Eliminating several on-chip peripherals contained in the original HC11 design has contributed to the economy of this MCU, which has features comparable to those of the MC68HC711D3 but different data bus configuration, quantity of memory, and number of I/O ports. For detailed information about this microcontroller, refer to the *M68HC11 Reference Manual*, document number M68HC11 RM/AD.

Features

- MC68HC11 CPU
- 16K Bytes of EPROM, or OTPROM
- 512 Bytes of On-Chip RAM (All Saved During Standby)
- 54 Multifunction I/O Pins
  - — 46 Bidirectional on 6 Ports
  - — 8 Fixed Input on 1 Port
- Enhanced 16-Bit Timer System
  - — 3 Input Capture (IC) Functions
  - — 4 Output Compare (OC) Functions
  - — 4th IC or 5th OC (Software Selectable)
- Real-Time Interrupt Circuit
- 8-Bit Pulse Accumulator
- Synchronous Serial Peripheral Interface (SPI)
- Asynchronous Nonreturn to Zero (NRZ) Serial Communications Interface (SCI)
- Power-Saving STOP and WAIT Modes
- Computer Operating Properly (COP) Watchdog System and Clock Speed Monitor
- 68-Pin PLCC and 64-Pin Quad Flat Packages (QFP)

Ordering Information

Package	Temperature	MC Order Number	Description
68-Pin PLCC	– 40° to + 85° C	MC68HC711J6FN	Plastic Quad OTPROM
64-Pin QFP	– 40° to + 85° C	MC68HC711J6FU	Plastic Quad OTPROM
68-Pin Cerquad	– 40° to + 85° C	MC68HC711J6FS	Ceramic Quad EPROM

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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For More Information On This Product,
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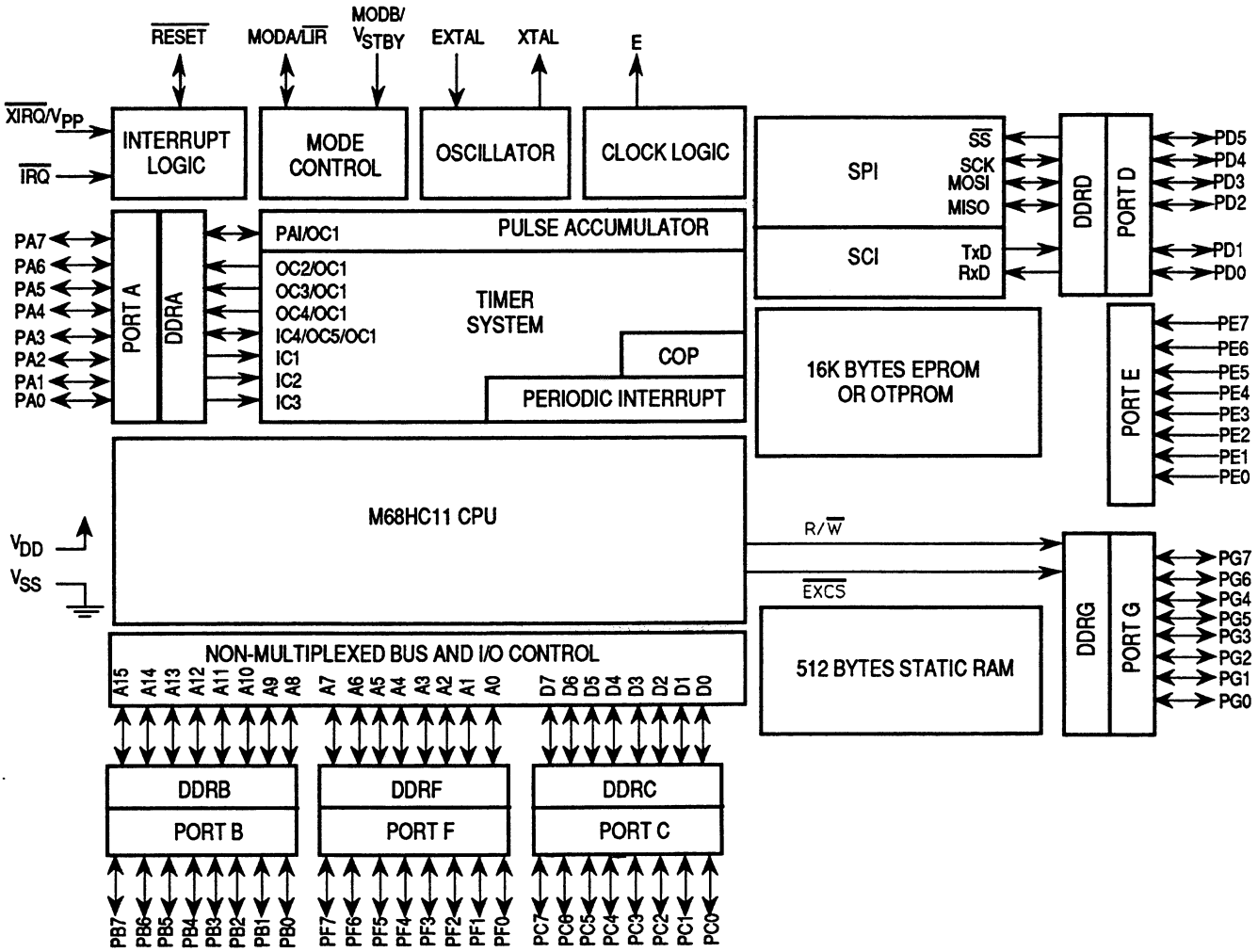

Block Diagram

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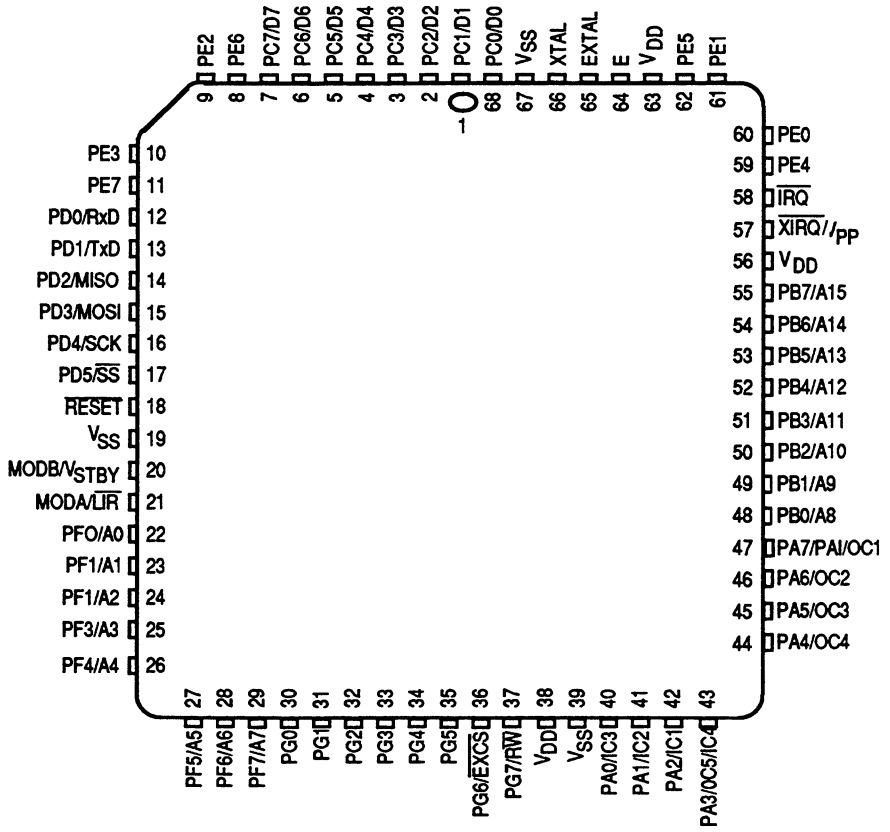
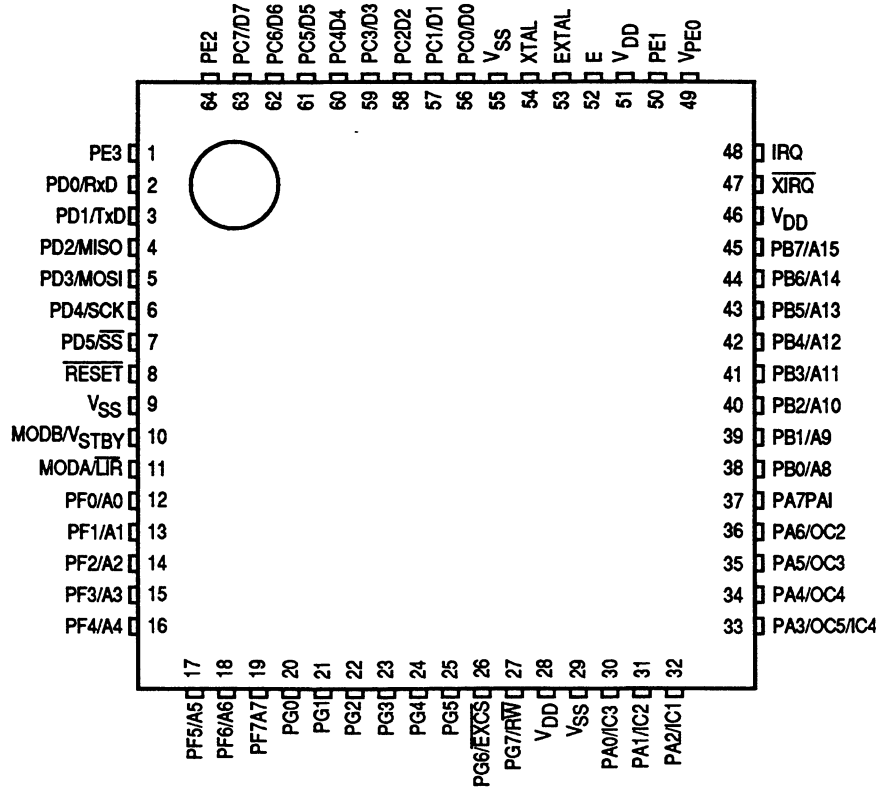
Pin Assignments



68-Pin PLCC Cerquad



64-Pin QFP

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Operating Modes and Memory Maps

In single-chip operating mode, the MC68HC11L6 is a monolithic microcontroller without external address or data buses. In expanded nonmultiplexed operating mode, the MCU can access a 64K byte address space. High-order address bits are output on the port B pins, low-order address bits on the port F pins, and the data bus on port C. The R/$\overline{W}$ pin controls the direction of data transfer on the port C bus and the $\overline{EXCS}$ pin is an external chip select, which can be used directly or as a qualifier for decoding any external devices.

Special bootstrap mode allows special-purpose programs to be entered into internal RAM. The boot loader program uses the SCI to read a program of up to 512 bytes into on-chip RAM at $0000 through $01FF. After a four-character delay, or after receiving the character for address $01FF, control passes to the loaded program at $0000.

Special test mode is used primarily for factory testing.

Memory Maps

Memory locations are the same for all modes except for the default location of the 16K bytes of EPROM or OTPROM, and the boot ROM, which appears only in special-bootstrap mode. The 64-byte register block originates at $1000 after reset, but can be placed at any other 4K boundary ($x000) after reset by writing an appropriate value to the INIT register.

The on-board 512-byte RAM is initially located at $0000 after reset, but can be placed at any other 4K boundary ($x000) by writing an appropriate value to the INIT register.

Hardware priority is built into the memory remapping. Registers have priority over RAM, and RAM has priority over ROM. The higher priority resource covers the lower, making the underlying locations inaccessible.

The 16K-byte EPROM or OTPROM is located at $C000 in all modes except expanded nonmultiplexed, where it is located at $4000. The EPROM or OTPROM can be located at $C000 in expanded nonmultiplexed mode by entering single-chip mode out of reset, then setting the MDA bit in the HPRIO register to 1, entering expanded mode from internal PROM. Enable the EPROM or OTPROM by setting the EPON bit of the CONFIG register.

In special test and special bootstrap modes, reset and interrupt vectors are located at $BFC0 through $BFFF. In special bootstrap mode, a bootloader ROM is enabled at locations $BF00 through $BFFF.

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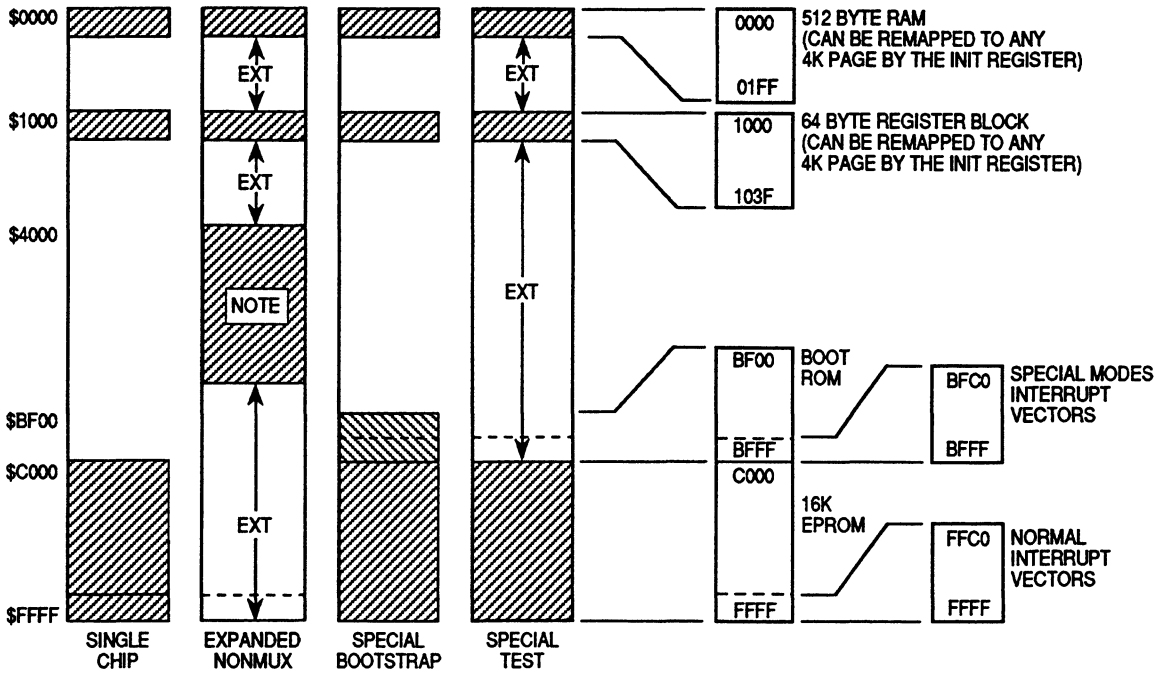

NOTE: In expanded nonmultiplexed mode, the 16K EPROM is initially located at $4000–$7FFF.

Memory Map

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Register and Control Bit Assignments (1 of 2)

This register block can be remapped to any 4K boundary.

	Bit 7	6	5	4	3	2	1	Bit 0	
$1000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$1001	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA
$1002	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	PORTF
$1003	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0	DDRF
$1004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$1005	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
$1006	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$1007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
$1008	0	0	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$1009	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
$100A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
$100E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (High)
$100F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (Low)
$1010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (High)
$1011	Bit 7	6	5	4	3	2	1	Bit 0	TIC1 (Low)
$1012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (High)
$1013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (Low)
$1014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (High)
$1015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (Low)
$1016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1(High)
$1017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (Low)
$1018	Bit 15	14	13	12	11	10	9	Bit 8	TOC2 (High)
$1019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (Low)
$101A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (High)
$101B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (Low)
$101C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (High)
$101D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (Low)
$101E	Bit 15	14	13	12	11	10	9	Bit 8	TI4O5 (High)
$101F	Bit 7	6	5	4	3	2	1	Bit 0	TI4O5 (Low)

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Register and Control Bit Assignments (2 of 2)

	Bit 7	6	5	4	3	2	1	Bit 0	
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
$1022	OC1I	OC2I	OC3I	OC4I	I4O5I	IC1I	IC2I	IC3I	TMSK1
$1023	OC1F	OC2F	OC3F	OC4F	I4O5F	IC1F	IC2F	IC3F	TFLG1
$1024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
$1025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2
$1026	0	PAEN	PAMOD	PEDGE	0	I4/O5	RTR1	RTR0	PACTL
$1027	Bit 7	6	5	4	3	2	1	Bit 0	PACNT
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
$1029	SPIF	WCOL	0	MODF	0	0	0	0	SPSR
$102A	Bit 7	6	5	4	3	2	1	Bit 0	SPDR
$102B	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD
$102C	R8	T8	0	M	WAKE	0	0	0	SCCR1
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE	0	SCSR
$102F	Bit 7	6	5	4	3	2	1	Bit 0	SCDR
$1030 to $1035									Reserved
$1036	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	PORTG
$1037	DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0	DDRG
$1038	GWOM	CWOM	0	0	0	XCSEN	0	0	OPT2
$1039	0	0	IRQE	DLY	CME	0	CR1	CR0	OPTION
$103A	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
$103B	0	0	ELAT	0	0	0	0	PGM	PPROG
$103C	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
$103E	TILOP	EPTST	OCCR	CBYP	DISR	FCM	FCOP	0	TEST1
$103F	0	0	0	0	0	NOCOP	EPON	0	CONFIG

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OPT2 — System Configuration Options Register 2 **$1038**

	Bit 7	6	5	4	3	2	1	Bit 0
	GWOM	CWOM	0	0	0	XCSEN	0	0
RESET:	0	0	0	0	0	*	0	0

*Reset sets this bit in expanded and test modes and clears it in single-chip and bootstrap modes.

Bit 7–6 — Refer to **Parallel I/O**.

Bits 5–3, 1–0 — Not implemented

XCSEN — External Chip-Select Enable

0 = $\overline{\text{EXCS}}$ signal is disabled. PG6 is general-purpose I/O.

1 = $\overline{\text{EXCS}}$ signal is enabled. In expanded and test modes only, the $\overline{\text{EXCS}}$ signal can drive the chip selects of off-chip devices. The signal is valid for any address not decoded internally. Using this signal to decode external devices prevents bus conflicts with internal devices.

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous **$103C**

	Bit 7	6	5	4	3	2	1	Bit 0	
	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0	
RESETS:									
	0	0	0	0	0	1	0	1	Single-Chip Mode
	0	0	1	0	0	1	0	1	Exp'd-NonMux'd
	1	1	0	0	0	1	0	1	Bootstrap
	0	1	1	1	0	1	0	1	Special Test

RBOOT, SMOD, MDA, AND IRVNE reset depend on mode selected at power-up.

RBOOT — Read Bootstrap ROM

Valid only when SMOD is set to one (special bootstrap or special test mode). Can only be written in special modes.

0 = Boot loader ROM disabled and not in map

1 = Boot loader ROM enabled and in map at $BF00–$BFFF

SMOD and MDA — Special Mode Select and Mode Select A

These two bits can be read at any time. SMOD can only be written in special modes. MDA can be written at any time in special modes, but only once in normal modes.

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Inputs		Mode	Latched at Reset	
MODB	MODA		SMOD	MDA
1	0	Single Chip	0	0
1	1	Expanded Nonmultiplexed	0	1
0	0	Special Bootstrap	1	0
0	1	Special Test	1	1

IRVNE — Internal Read Visibility/Not E (IRVNE can be written once in any mode)

In expanded modes, IRVNE determines whether IRV is on or off.

In special test mode, IRVNE is reset to 1 and in all other modes IRVNE is reset to 0.

0 = No internal read visibility on external bus

1 = Data from internal reads is driven out of the external data bus

In single-chip modes, this bit determines whether the E clock drives out of the chip.

0 = E driven out from the chip

1 = E pin driven low

Mode	IRVNE Out of Reset	E Clock Out of Reset	IRV Out of Reset	IRVNE Affects Only
Single Chip	0	On	Off	E
Expanded	0	On	Off	IRV
Bootstrap	0	On	Off	E
Special Test	1	On	On	IRV

For information on bits 3–0, refer to **Resets and Interrupts**.

INIT — RAM and I/O Mapping **$103D**

	Bit 7	6	5	4	3	2	1	Bit 0
	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
RESET:	0	0	0	0	0	0	0	1

RAM3–RAM0 — Internal RAM Map Position

These four bits determine the upper four bits of the RAM address.

REG3–REG0 — 64-Byte Register Block Map Position

These four bits determine the upper four bits of the register block address.

NOTE

Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes. Refer to **Operating Modes and Memory Maps** for additional information.

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TEST1 — Factory Test (Test Mode Only) **$103E**

	Bit 7	6	5	4	3	2	1	Bit 0
	TILOP	EPTST	OCCR	CBYP	DISR	FCM	FCOP	0
RESET:	0	0	0	0	—	0	0	0

TILOP — Test Illegal Opcode

EPTEST — EPROM Test

OCCR — Output Condition Code Register to Timer Port

CBYP — Timer Divider Chain Bypass

DISR — Disable Resets from COP and Clock Monitor

In test and bootstrap modes, this bit is reset to 1 to inhibit clock monitor and COP resets. In normal modes, DISR is reset to 0.

FCM — Force Clock Monitor Failure

FCOP — Force COP Watchdog Failure

CONFIG — Configuration Control **$103F**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	0	NOCOP	EPON	0
RESET								
Normal Modes:	0	0	0	0	0	0	1	0
Special Modes:	0	0	0	0	0	1	1	0

Bits 7–3 and 0 — Not implemented. These bits always read zero.

Bit 2 — Refer to **Resets and Interrupts**.

EPON — PROM Enable

This bit is set out of reset, enabling the EPROM or OTPROM in all modes. In single chip, bootstrap, and test modes, PROM is located at $C000–$FFFF. In expanded mode, PROM is located at $4000–$7FFF. Refer to **Operating Modes and Memory Maps** for information about relocating PROM in expanded mode. This bit is not writable in single-chip mode, but is writable once in expanded mode, or at any time in special modes.

0 = PROM is disabled from the memory map

1 = PROM is present in the memory map

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Resets and Interrupts

The MC68HC711J6 has 3 reset vectors and 18 interrupt vectors. The reset vectors are as follows:

- $\overline{\text{RESET}}$, or Power-On Reset
- Clock Monitor Fail
- COP Failure

The 18 interrupt vectors service 22 interrupt sources (3 non-maskable, 19 maskable). The three non-maskable interrupt vectors are as follows:

- Illegal Opcode Trap
- Software Interrupt
- $\overline{\text{XIRQ}}$ Pin (Pseudo Non-Maskable Interrupt)

On-chip peripheral systems generate maskable interrupts, which are recognized only if the global interrupt mask bit (I) in the condition code register (CCR) is clear. Nineteen interrupt sources in the MC68HC711J6 are subject to masking by a global interrupt mask bit.

Interrupt and Reset Vector Assignments

Vector Address	Interrupt Source	CC Register Mask	Local Mask
FFD4, D5 — FFC0, C1	Reserved	—	—
FFD6, D7	SCI Serial System	I Bit	—
	SCI Transmit Complete		TCIE
	SCI Transmit Data Register Empty		TIE
	SCI Idle Line Detect		ILIE
	SCI Receiver Overrun		RIE
	SCI Receive Data Register Full		RIE
FFD8, D9	SPI Serial Transfer Complete	I Bit	SPIE
FFDA, DB	Pulse Accumulator Input Edge	I Bit	PAII
FFDC, DD	Pulse Accumulator Overflow	I Bit	PAOVI
FFDE, DF	Timer Overflow	I Bit	TOI
FFE0, E1	Timer Input Capture 4/Output Compare 5	I Bit	I4O5I
FFE3, E2	Timer Output Compare 4	I Bit	OC4I
FFE4, E5	Timer Output Compare 3	I Bit	OC3I
FFE6, E7	Timer Output Compare 2	I Bit	OC2I
FFE8, E9	Timer Output Compare 1	I Bit	OC1I
FFEA, EB	Timer Input Capture 3	I Bit	IC3I
FFEC, ED	Timer Input Capture 2	I Bit	IC2I
FFEE, EF	Timer Input Capture 1	I Bit	IC1I
FFF0, F1	Real-Time Interrupt	I Bit	RTII
FFF2, F3	$\overline{\text{IRQ}}$ (External Pin)	I Bit	None
FFF4, F5	$\overline{\text{XIRQ}}$ Pin	I Bit	None
FFF6, F7	Software Interrupt	None	None
FFF8, F9	Illegal Opcode Trap	None	None
FFFA, FB	COP Failure	None	NOCOP
FFFC, FD	COP Clock Monitor Fail	None	CME
FFFE, FF	$\overline{\text{RESET}}$	None	None

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Maskable interrupts are prioritized according to a default arrangement; however, any source can be elevated to the highest maskable priority position by a software-accessible control register, HPRIO. This register can be written at any time, provided the I bit in the CCR is set. In addition to the global I bit, all of these sources, except the external interrupt (IRQ pin), are controlled by local enable bits in control registers. Most interrupt sources in the M68HC11 have separate interrupt vectors and there is usually no need for software to poll control registers to determine the cause of an interrupt. Refer to the table of interrupt and reset vector assignments.

For some interrupt sources, such as the SCI interrupts, the flags are automatically cleared as interrupt requests are processed. For example, the RDRF flag in the SCI system is cleared by the automatic clearing mechanism, which consists of a read of the SCI status register while RDRF is set, followed by a read of the SCI data register. The normal response to an RDRF interrupt request is to read the SCI status register to check for receive errors, then to read the received data from the SCI data register. These two steps satisfy the automatic clearing mechanism without requiring any special instructions.

OPTION — System Configuration Options **$1039**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	IRQE*	DLY*	CME	0	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes.

Bits 7–6, and 2 are not implemented. These bits always read zero.

IRQE — IRQ Select Edge Sensitive Only
0 = Low-level recognition
1 = Falling edge recognition

DLY — Enable Oscillator Start-Up Delay on Exit from STOP
0 = No stabilization delay on exit from STOP
1 = Stabilization delay of 4064 E-clock cycles is enabled on exit from STOP.

CME — Clock Monitor Enable
0 = Clock monitor disabled; slow clocks can be used.
1 = Slow or stopped clocks cause clock failure reset.

CR1, CR0 — COP Timer Rate Select

COP Timer Rate Select

CR [1:0]	Divide E/2^{15} By	XTAL = 4.0 MHz Timeout –0/+32.8 ms	XTAL = 8.0 MHz Timeout –0/+16.4 ms	XTAL = 12.0 MHz Timeout –0/+10.9 ms
0 0	1	32.768 ms	16.384 ms	10.923 ms
0 1	4	131.07 ms	65.536 ms	43.691 ms
1 0	16	524.29 ms	262.14 ms	174.76 ms
1 1	64	2.097 sec	1.049 sec	699.05 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz

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COPRST — Arm/Reset COP Timer Circuitry **$103A**

	Bit 7	6	5	4	3	2	1	Bit 0
	7	6	5	4	3	2	1	0
RESET:	0	0	0	0	0	0	0	0

Write $55 to COPRST to arm COP watchdog clearing mechanism.
Write $AA to COPRST to reset COP watchdog.

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous **$103C**

	Bit 7	6	5	4	3	2	1	Bit 0
	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0
RESET:	–	–	–	–	0	1	0	1

For information on bits 4–7, refer to **Operating Modes and Memory Maps**.

PSEL3–PSEL0 — Priority Select Bits 3 –0
Writable only while the I bit in the CCR is set (interrupts disabled). These bits select one interrupt source to be elevated above all other I-bit-related sources.

PSEL [3:0]	Interrupt Source Promoted
0000	Timer Overflow
0001	Pulse Accumulator Overflow
0010	Pulse Accumulator Input Edge
0011	SPI Serial Transfer Complete
0100	SCI Serial System
0101	Reserved (Default to $\overline{\text{IRQ}}$)
0110	$\overline{\text{IRQ}}$ (External Pin)
0111	Real-Time Interrupt
1000	Timer Input Capture 1
1001	Timer Input Capture 2
1010	Timer Input Capture 3
1011	Timer Output Compare 1
1100	Timer Output Compare 2
1101	Timer Output Compare 3
1110	Timer Output Compare 4
1111	Timer Output Compare 5/Input Capture 4

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CONFIG — Configuration Control **$103F**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	0	NOCOP	EPON	0
RESET:								
Normal Modes:	0	0	0	0	0	0	1	0
Special Modes:	0	0	0	0	0	1	1	0

Bits 7–3 and 0 — Not implemented. These bits always read zero.

NOCOP — COP System Disable

Writable once after reset in normal modes; writable any time in special modes

0 = COP enabled (forces reset on timeout)

1 = COP disabled (does not force reset on timeout)

Bit 1 — Refer to **Modes of Operation and Memory Maps.**

Erasable or One-Time Programmable ROM

The MC68HC711J6 has 16K bytes of PROM, either EPROM or OTPROM. Once programmed, EPROM must be erased by exposure to ultraviolet light before it can be reprogrammed. OTPROM cannot be erased.

The PROM address is normally $C000–$FFFF. In expanded nonmultiplexed mode, however, the PROM is located at $4000–$7FFF.

To protect the OTPROM or EPROM, observe the following precautions:

1. Ensure that the voltage on the $\overline{\text{XIRQ}}$/V_{PP} pin does not exceed the voltage on the V_{DD} pin. The PROM cannot be programmed or corrupted without high voltage on the $\overline{\text{XIRQ}}$ pin.

2. If the part is operated with V_{PP} voltage present on the \s\up6(\f(,XIRQ))/V_{PP} pin, the $\overline{\text{IRQ}}$/$\overline{\text{CE}}$ pin must be pulled to a high level in reset.

3. Ensure V_{PP} is not present when $\overline{\text{IRQ}}$ is low if the part is in bootstrap mode. A pull-up resistor on the $\overline{\text{IRQ}}$ line keeps it high during reset.

Programming EPROM requires an external 12.25-volt nominal power supply (V_{PP}). There are two ways to program the PROM: EPROM emulation, PROG mode, and MCU mode. In PROG mode, the EPROM is programmed as a standalone by adapting the MCU footprint to the 27256-type EPROM and using an appropriate EPROM programmer. Refer to the following block diagram, which shows the PROM in PROG mode.

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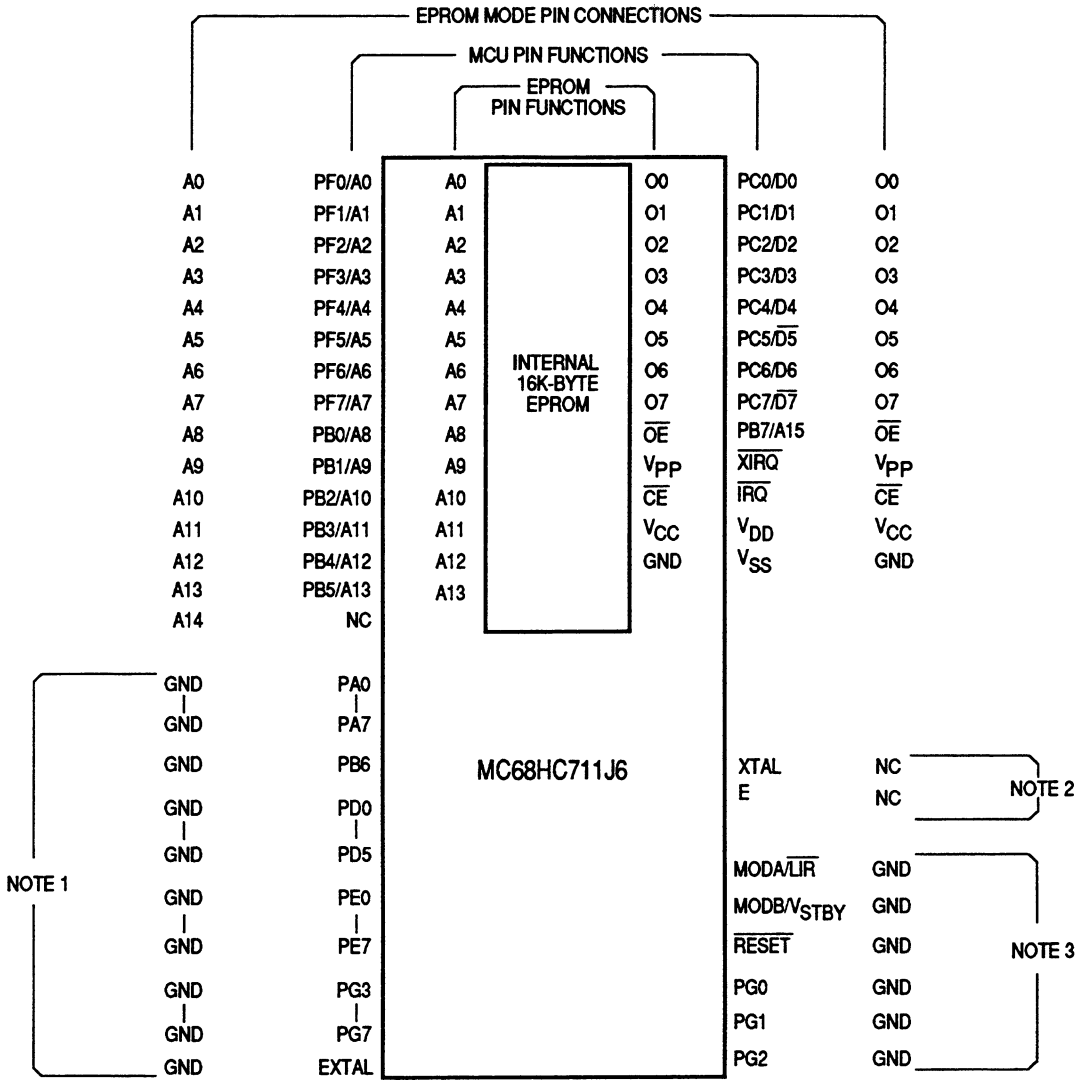

NOTES:

1. Unused Inputs — grounding is recommended.
2. Unused outputs — these pins should be left unterminated.
3. These pins must be grounded for PROG mode.

Block Diagram in PROG Mode

In normal MCU mode, EPROM can be programmed in any operating mode. Special test and bootstrap modes are preferred, however. Normal programming is accomplished through the PPROG register.

Erase the EPROM by exposing the chip to high-intensity ultraviolet light (wavelength 2537 Å for 30–60 minutes. The erased state of an EPROM location is $FF. OTPROM cannot be erased after programming.

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PPROG — EPROM Programming Control **$103B**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	ELAT	0	0	0	0	PGM
RESET:	0	0	0	0	0	0	0	0

Bits 7–6, and 4–1 — Not implemented; always read zero

ELAT — EPROM or OTPROM Latch Control
0 = EPROM address and data bus configured for normal reads
1 = EPROM address and data bus configured for programming

PGM — EPROM or OTPROM Program Command
This bit can be written only when ELAT = 1.
0 = Programming voltage switched off to PROM array
1 = Programming voltage switched on to PROM array

CONFIG — Configuration Control **$103F**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	0	NOCOP	EPON	0
RESET:								
Normal Modes	0	0	0	0	0	0	1	0
Special Modes:	0	0	0	0	0	1	1	0

Bits 7–3 and 0 — Not implemented. These bits always read zero.

Bit 2 — Refer to **Resets and Interrupts**.

EPON — PROM Enable
This bit is set out of reset, enabling the EPROM or OTPROM in all modes. In single chip, bootstrap, and test modes, the PROM is located at $C000–$FFFF. In expanded mode, the PROM is located at $4000–$7FFF. Refer to **Operating Modes and Memory Maps** for information on relocating the PROM in expanded mode.

EPON is not writable in single-chip mode, but is writable once in expanded mode. In special modes, this bit is always writable.
0 = PROM is disabled from the memory map
1 = PROM is present in the memory map

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Parallel Input/Output

The MC68HC711J6 has six 8-bit I/O ports (A, B, C, E, F, and G), and one 6-bit I/O port (D). I/O functions on some ports (B, C, F, and G) are affected by the mode of operation selected. In the single-chip and bootstrap modes, the ports are configured as parallel I/O data ports. In expanded non-multiplexed and test modes, ports B, C, and F and lines PG6 ($\overline{EXCS}$) and PG7 (R/$\overline{W}$) are configured as a memory expansion bus with ports B and F as the address bus; port C as the data bus; R/$\overline{W}$ as the data bus direction control; and $\overline{EXCS}$ as a chip-select output.

The remaining ports are unaffected by mode changes. Ports A and D and the remaining port G pins can be used as general-purpose I/O ports, though Ports A and D have alternate functions. Port A pins share timer functions, and port D pins share the SPI and SCI functions. Port E is used for general-purpose static inputs.

Port A is an 8-bit general-purpose I/O port with both a data register, PORTA, and a data direction register, DDRA. Port A pins are available for shared use among main timer, pulse accumulator, and general I/O functions. Port A pins can be configured for three timer input captures (ICs) and four timer output compares (OCs), and either a fourth IC or a fifth OC. PAI function is always available on PA7 (software readable at any time, even when another function is enabled).

Port B is an 8-bit general-purpose I/O port with a data register, PORTB, and a data direction register, DDRB, in single-chip modes. In expanded modes, Port B is used for the high-order address lines, A15–A8, of the address bus, and accesses to PORTB are treated as external.

Port C is an 8-bit general-purpose I/O port with a data register, PORTC, and a data direction register, DDRC, in the single-chip modes. Port C can be configured for wired-OR operation in single-chip modes by setting the CWOM bit of the OPT2 register. In the expanded non-multiplexed mode, Port C is a bidirectional data bus, D7–D0, controlled by the R/$\overline{W}$ signal.

Port D is a 6-bit, general-purpose I/O port with a data register, PORTD, and a data direction register, DDRD. In all modes, the six port D pins, D5–D0, can be used for general-purpose I/O, or for the SCI and SPI subsystems.

Port E is an 8-bit, input-only port with a data register, PORTE, that is enabled only during read cycles.

Port F is an 8-bit, general-purpose I/O port with a data register, PORTF, and a data direction register, DDRF, in single-chip mode. In expanded modes, Port F is used for the low-order address, A7–A0.

Port G is an 8-bit, general-purpose I/O port with both a data register, PORTG, and a data direction register, DDRG. In single-chip mode, PORTG pins are general-purpose I/O pins, PG7–PG0. In the expanded non-multiplexed mode, PORTG pins 7 and 6 are configured as non-multiplexed address/data bus control lines R/$\overline{W}$ and $\overline{EXCS}$; pins PG5–PG0 remain general-purpose I/O.

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PORTA — Port A Data **$1000**

	Bit 7	6	5	4	3	2	1	Bit 0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	Reset configures pins as HiZ inputs							
Alt. Pin Funct.:	PAI	OC2	OC3	OC4	OC5/IC4	IC1	IC2	IC3
And/or:	OC1	OC1	OC1	OC1	OC1	—	—	—

The OC5/IC4 selection is controlled by the I4O5I bit in the TMSK1 register.

DDRA — Data Direction Register for Port A **$1001**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
RESET:	0	0	0	0	0	0	0	0

For DDRx bits, 0 = input and 1 = output.

PORTF— Port F Data **$1002**

	Bit 7	6	5	4	3	2	1	Bit 0
	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
S. Chip or Boot:	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
RESET:	Reset configures pins as HiZ inputs							
Expan. or Test	A7	A6	A5	A4	A3	A2	A1	A0

DDRF — Data Direction Register for Port F **$1003**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0
RESET:	0	0	0	0	0	0	0	0

For DDRx bits, 0 = input and 1 = output.

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PORTB — Port B Data **$1004**

	Bit 7	6	5	4	3	2	1	Bit 0
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
S. Chip or Boot:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
RESET:	Reset configures pins as HiZ inputs							
Expan. or Test:	A15	A14	A13	A12	A11	A10	A9	A8

DDRB — Data Direction Register for Port B **$1005**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
RESET:	0	0	0	0	0	0	0	0

For DDRx bits, 0 = input and 1 = output.

PORTC — Port C Data **$1006**

	Bit 7	6	5	4	3	2	1	Bit 0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
S. Chip or Boot:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:	Reset configures pins as HiZ inputs							
Expan. or Test:	D7	D6	D5	D4	D3	D2	D1	D0

DDRC — Data Direction Register for Port C **$1007**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
RESET:	0	0	0	0	0	0	0	0

For DDRx bits, 0 = input and 1 = output.

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PORTD — Port D Data **$1008**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	Reset configures pins as HiZ inputs							
Alt. Pin Funct.:	0	0	$\overline{SS}$	SCK	MOSI	MISO	TxD	RxD

Bits 7–6 — Not implemented; always read zero

DDD5–DDD0 — Data Direction for Port D

When DDRD bit 5 is zero and MSTR = 1 in SPCR, PD5/SS is a general-purpose output and mode fault logic is disabled.

0 = Input
1 = Output

DDRD — Data Direction Register for Port D **$1009**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0

Bits 7–6 — Not implemented; always read 0

For DDRx bits, 0 = input and 1 = output.

PORTE — Port E Data **$100A**

	Bit 7	6	5	4	3	2	1	Bit 0
	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
RESET:	*	*	*	*	*	*	*	*

*Reset does not affect this address.

PORTG — Port G Data **$1036**

	Bit 7	6	5	4	3	2	1	Bit 0
	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
S. Chip or Boot:	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
RESET:	Output latches cleared at reset, but pins configured as HiZ inputs							
Alt. Pin Funct.:	R/$\overline{W}$	$\overline{EXCS}$	PG5	PG4	PG3	PG2	PG1	PG0

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DDRG — Data Direction Register for Port G **$1037**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0
RESET:	0	0	0	0	0	0	0	0

For DDRx bits, 0 = input and 1 = output

OPT2 — System Configuration Options Register 2 **$1038**

	Bit 7	6	5	4	3	2	1	Bit 0
	GWOM	CWOM	0	0	0	XCSEN	0	0
RESET:	0	0	0	0	0	*	0	0

*Reset sets XCSEN in expanded and test modes, clears it in single-chip and bootstrap modes.

GWOM — Port G Wired-OR Mode Option
This bit affects all port G pins together.
0 = Port G outputs are normal CMOS outputs.
1 = Port G outputs act as open-drain outputs.

CWOM — Port C Wired-OR Mode Option
This bit affects all port C pins together.
0 = Port C outputs are normal CMOS outputs.
1 = Port C outputs act as open-drain outputs.

Bits 5–3, 1–0 — Not implemented

Bit 2 — Refer to **Operating Modes and Memory Maps**.

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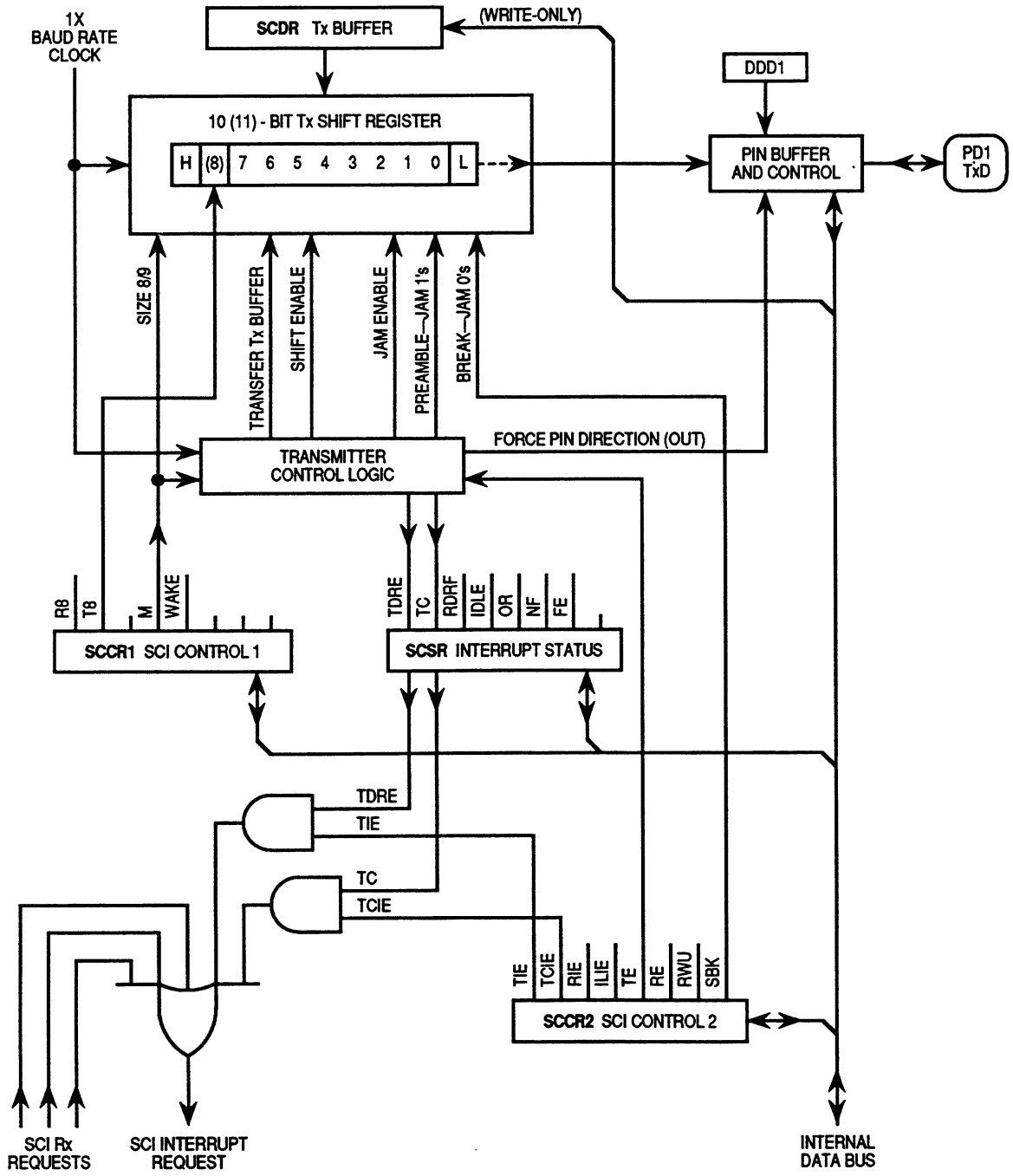
Serial Communications Interface (SCI)

The SCI, a universal asynchronous receiver transmitter (UART) serial communications interface, is one of two independent serial I/O subsystems in the MC68HC711J6. The SCI has a standard NRZ format (one start, eight or nine data and one stop bit) and several baud rates. The transmitter and receiver are independent but use the same data format and bit rate.



SCI Transmitter Block Diagram

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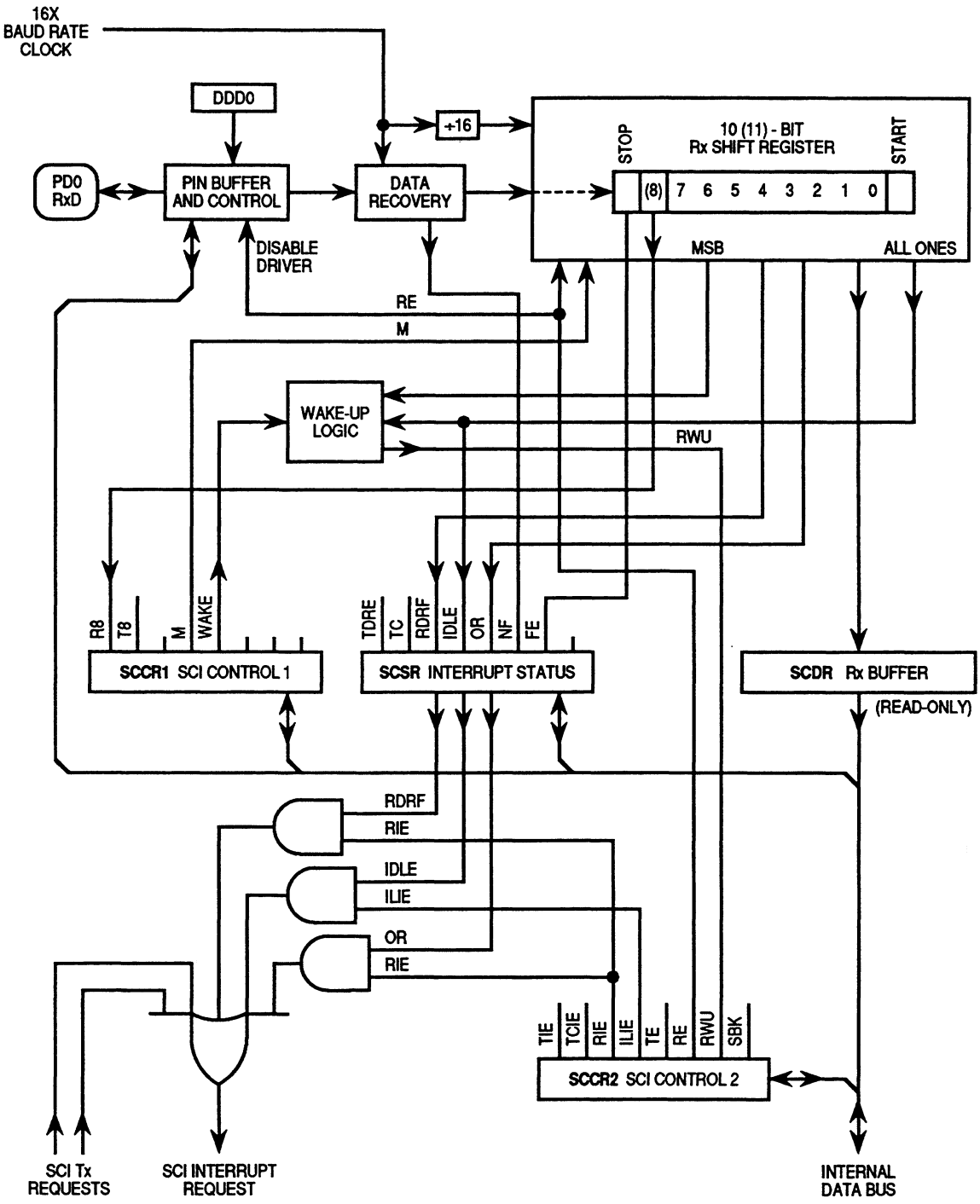

SCI Receiver Block Diagram

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SPCR — Serial Peripheral Control **$1028**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

Bits 7–6 and 4–0 — Refer to **Serial Peripheral Interface**.

DWOM — Port D Wired-OR Mode Option
DWOM affects all six port D pins.
0 = Normal CMOS outputs
1 = Open-drain outputs

BAUD — Baud Rate **$102B**

	Bit 7	6	5	4	3	2	1	Bit 0
	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
RESET:	0	0	0	0	0	U	U	U

TCLR — Clear Baud Rate Counters (Test)

Bit 6 — Not implemented; always reads zero

SCP1, SCP0 — SCI Baud Rate Prescaler Selects
Refer to the baud rate prescaler and selection tables.

RCKB – SCI Baud Rate Clock Check (Test)

SCR2, SCR1, and SCR0 — SCI Baud Rate Selects
Selects receiver and transmitter baud rate. Refer to the the baud rate clock divider chain schematic.

Baud Rate Prescaler Sets Highest Rate

SCP [1:0]	Divide Internal Clock By	Crystal Frequency in MHz			
		4.0 MHz (Baud)	8.0 MHz (Baud)	10.0 MHz (Baud)	12.0 MHz (Baud)
0 0	1	62.50K	125.0K	156.25K	187.5K
0 1	3	20.83K	41.67K	52.08K	62.5K
1 0	4	15.625K	31.25K	38.4K	46.88K
1 1	13	4800	9600	12.02K	14.42K

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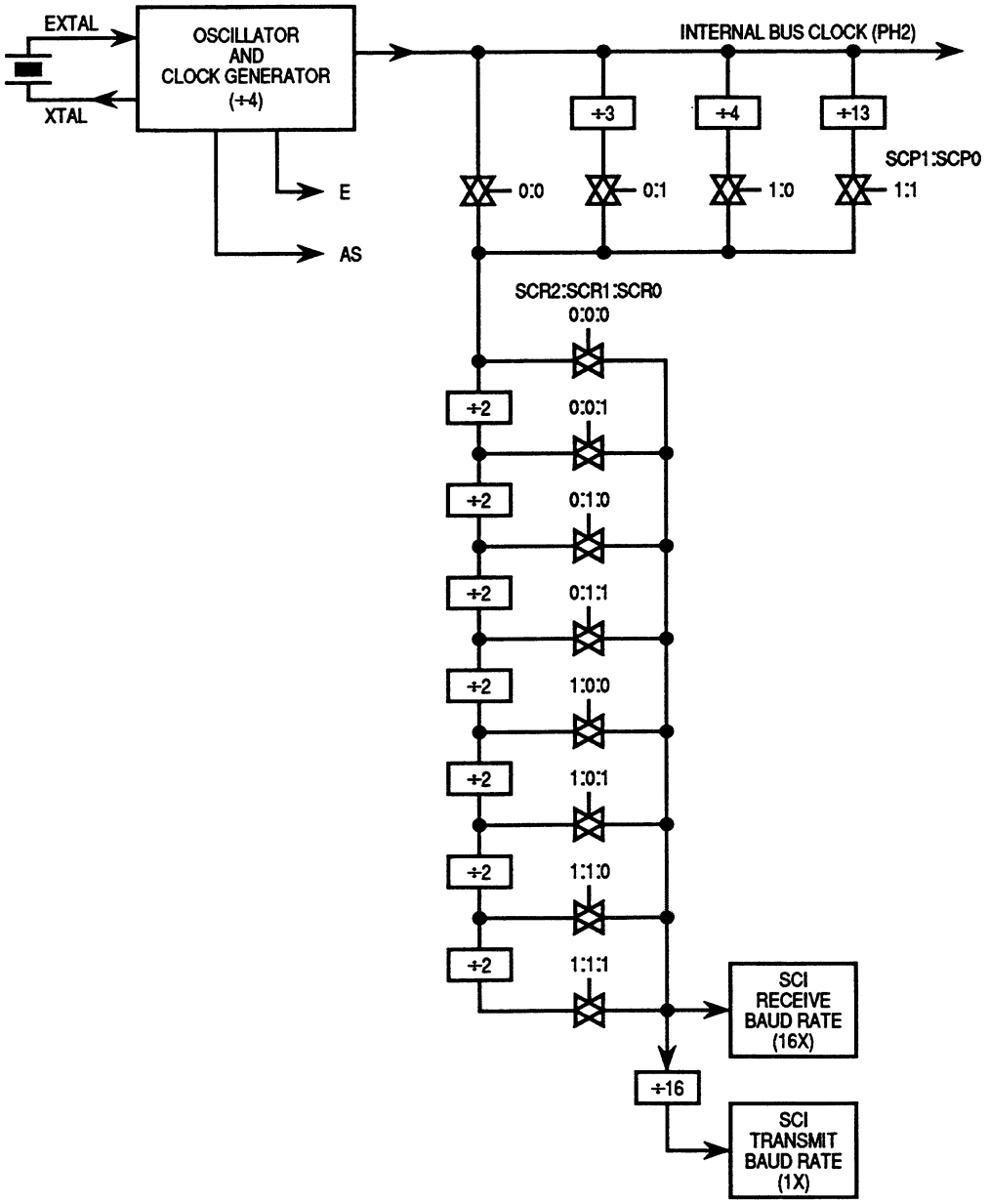
Baud Rate Selection

SCR Bit [2:0]	Divide Prescaler By	Highest Baud Rate (Prescaler Output from Previous Table)		
		4800	9600	38.4K
000	1	4800	9600	38.4K
001	2	2400	4800	19.2K
010	4	1200	2400	9600
011	8	600	1200	4800
100	16	300	600	2400
101	32	150	300	1200
110	64	—	150	600
111	128	—	—	300



Baud Rate Generator Block Diagram

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SCCR1 — SCI Control 1 **$102C**

	Bit 7	6	5	4	3	2	1	Bit 0
	R8	T8	0	M	WAKE	0	0	0
RESET:	U	U	0	0	0	0	0	0

R8 — Receive Data Bit 8
If M bit is set, R8 stores ninth bit in receive data character.

T8 — Transmit Data bit 8
If M bit is set, T8 stores ninth bit in transmit data character.

Bits 5 and 2–0 — Not implemented; always read zero

M — Mode (Select Character Format)
0 = Start, 8 data bits, 1 stop bit
1 = Start, 9 data bits, 1 stop bit

WAKE — Wake-Up by Address Mark/Idle
0 = Wake-up by IDLE line recognition
1 = Wake-up by address mark

SCCR2 — SCI Control 2 **$102D**

	Bit 7	6	5	4	3	2	1	Bit 0
	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET:	0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
0 = TDRE interrupts disabled
1 = SCI interrupt requested when TDRE status flag is set

TCIE — Transmit Complete Interrupt Enable
0 = TC interrupts disabled
1 = SCI interrupt requested when TC status flag is set

RIE — Receiver Interrupt Enable
0 = RDRF and OR interrupts disabled
1 = SCI interrupt requested when RDRF flag or the OR status flag is set

ILIE — Idle Line Interrupt Enable
0 = IDLE interrupts disabled
1 = SCI interrupt requested when IDLE status flag is set

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TE — Transmitter Enable
When TE goes from zero to one, one unit of idle character time, logic one, is queued as a preamble.
0 = Transmitter disabled
1 = Transmitter enabled

RE — Receiver Enable
0 = Receiver disabled
1 = Receiver enabled

RWU — Receiver Wake-Up Control
0 = Normal SCI receiver
1 = Wake-up enabled and receiver interrupt inhibited

SBK — Send Break
0 = Break generator off
1 = Break codes generated as long as SBK = 1

SCSR — SCI Status **$102E**

	Bit 7	6	5	4	3	2	1	Bit 0
	TDRE	TC	RDRF	IDLE	OR	NF	FE	0
RESET:	1	1	0	0	0	0	0	0

TDRE — Transmit Data Register Empty Flag
Set if transmit data has been written to SCDR
Cleared by SCSR read with TDRE set, followed by SCDR write

TC — Transmit Complete Flag
Set if transmitter is idle (no data, preamble, or break transmission in progress)
Cleared by SCSR read with TC set, followed by SCDR write

RDRF — Receive Data Register Full Flag
Set if a received character is ready to be read from SCDR
Cleared by SCSR read with RDRF set, followed by SCDR read

IDLE — Idle Line Detected Flag
Set if the RxD line is idle
Cleared by SCSR read with IDLE set, followed by SCDR read. Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again

OR — Overrun Error Flag
Set if a new character is received before a previously received character is read from SCDR
Cleared by SCSR read with OR set, followed by SCDR read

NF — Noise Error Flag
Set if majority sample logic detects anything other than a unanimous decision
Cleared by SCSR read with NF set, followed by SCDR read

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FE — Framing Error

Set if a 0 is detected where a stop bit was expected

Cleared by SCSR read with FE set, followed by SCDR read

Bit 0 — Not implemented; always reads 0

SCDR — Serial Communications Data Register **$102F**

	Bit 7	6	5	4	3	2	1	Bit 0
	Bit 7	6	5	4	3	2	2	Bit 0
RESET:	U	U	U	U	U	U	U	U

Reads access buffered receive data. Writes access transmit data buffer register. Receive and transmit are double buffered.

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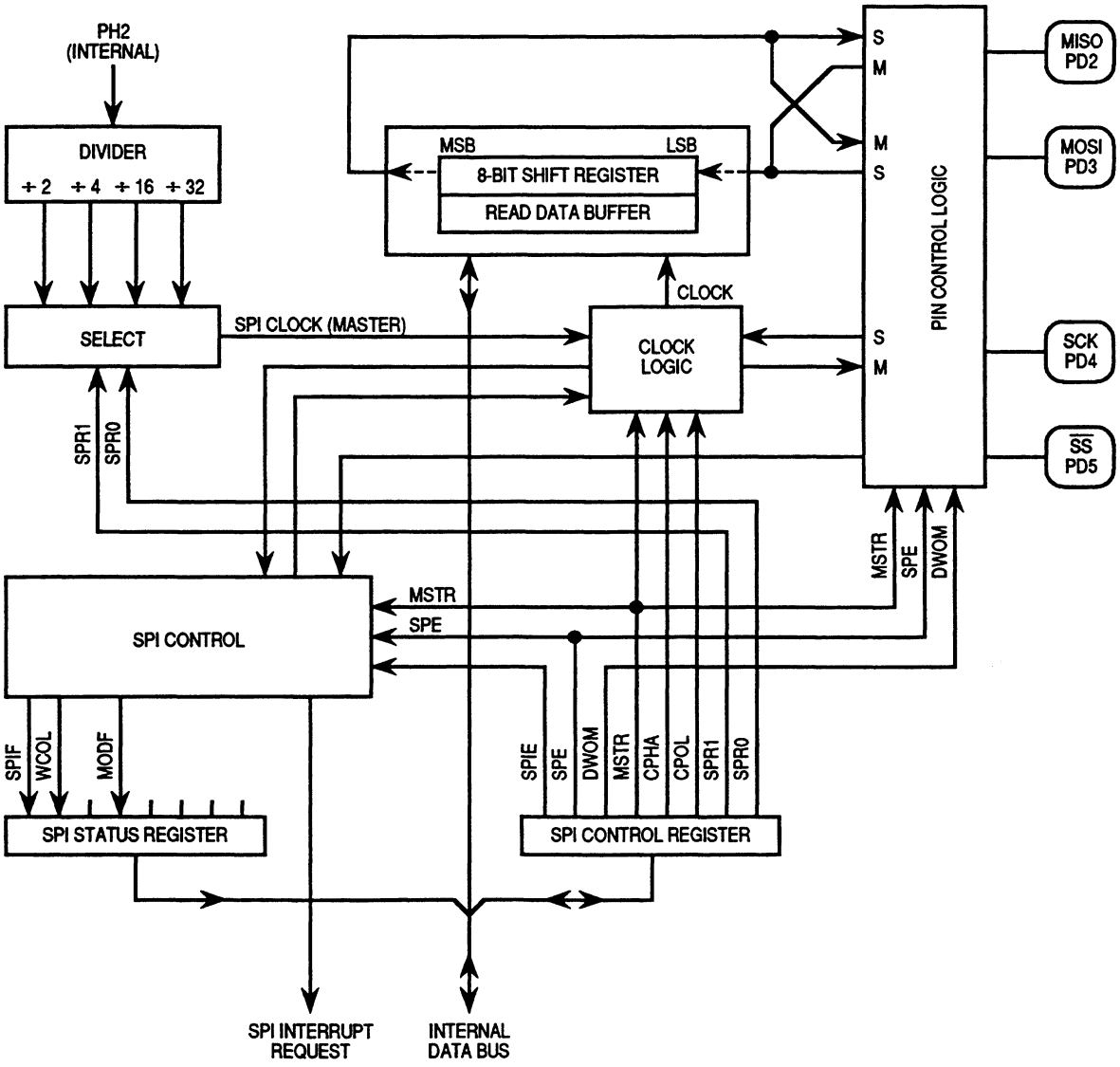
Serial Peripheral Interface (SPI)

The SPI is one of two independent serial communications subsystems that allows the MCU to communicate synchronously with peripheral devices and other microprocessors. The SPI protocol facilitates rapid exchange of serial data between devices in a control system. Each SPI compatible component in a system can be set up for master or slave operation. Data rates can be as high as one half of the E clock rate when configured as a master and as fast as the E clock when configured as a slave.



SPI Block Diagram

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DDRD — Data Direction Register for Port D **$1009**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	—	—	$\overline{SS}$	SCK	MOSI	MISO	TxD	RxD

DDD5–DDD0 — Data Direction for Port D

When DDRD bit 5 is zero and MSTR = 1 in SPCR, PD5/SS is a general-purpose output and mode fault logic is disabled.

0 = Input
1 = Output

SPCR — Serial Peripheral Control **$1028**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

SPIE — Serial Peripheral Interrupt Enable

0 = SPI interrupt disabled
1 = SPI interrupt enabled

SPE — Serial Peripheral System Enable

0 = SPI on
1 = SPI off

DWOM — Port D Wired-OR Mode Option

DWOM affects all six port D pins.

0 = Normal CMOS outputs
1 = Open-drain outputs

MSTR — Master Mode Select

0 = Slave mode
1 = Master mode

CPOL, CPHA — Clock Phase, Clock Polarity (Refer to following figure, **SPI Transfer Format**.)

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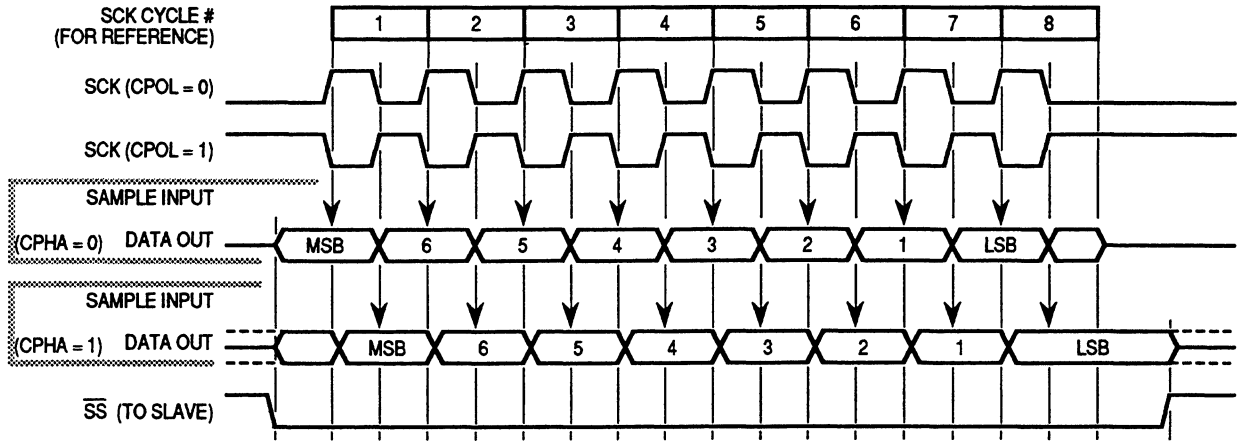

SPI Transfer Format

SPR1 and SPR0 — SPI Clock Rate Selects

SPI Clock Rate Selects

SPR [1:0]	E Clock Divide By	Frequency at E = 2 MHz (Baud)
0 0	2	1.0 MHz
0 1	4	500 kHz
1 0	16	125 kHz
1 1	32	62.5 kHz

SPSR — Serial Peripheral Status **$1029**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIF	WCOL	0	MODF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

SPIF — SPI Transfer Complete Flag
Set when an SPI transfer is complete
Cleared by reading SPSR with SPIF set, followed by SPDR access

WCOL — Write Collision
Set when SPDR is written while transfer is in progress
Cleared by SPSR with WCOL set, followed by SPDR access

Bits 5 and 3–0 — Not implemented; always read zero

MODF — Mode Fault (A Mode Fault Terminates SPI Operation)
Set when $\overline{SS}$ is pulled low while MSTR = 1
Cleared by SPSR read with MODF set, followed by SPCR write

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SPDR — SPI Data **$102A**

Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

SPI is double buffered in, single buffered out.

Main Timer

The main timer is based on a free-running 16-bit counter with a four-stage programmable prescaler. The timer shares port A pins, which can be configured for three timer input captures (ICs) and four timer output compares (OCs), and either a fourth IC or a fifth OC. Refer to the following table for crystal-related frequencies and periods.

Timer Summary

Control Bits	XTAL Frequencies			
	4.0 MHz	8.0 MHz	12.0 MHz	Other Rates
	1.0 MHz	2.0 MHz	3.0 MHz	(E)
	1000 ns	500 ns	333 ns	(1/E)
PR [1:0]	Main Timer Count Rates			
0 0 1 count overflow	1.0 µs 65.536 ms	500 ns 32.768 ms	333 ns 21.845 ms	(E/1) ($E/2^{16}$)
0 1 1 count overflow	4.0 µs 262.14 ms	2.0 µs 131.07 ms	1.333 µs 87.381 ms	(E/4) ($E/2^{18}$)
1 0 1 count overflow	8.0 µs 524.29 ms	4.0 µs 262.14 ms	2.667 µs 174.76 ms	(E/8) ($E/2^{19}$)
1 1 1 count overflow	16.0 µs 1.049 s	8.0 µs 524.29 ms	5.333 µs 349.52 ms	(E/16) ($E/2^{20}$)
RTR [1:0]	Periodic (RTI) Interrupt Rates			
0 0	8.192 ms	4.096 ms	2.731 ms	($E/2^{13}$)
0 1	16.384 ms	8.192 ms	5.461 ms	($E/2^{14}$)
1 0	32.768 ms	16.384 ms	10.923 ms	($E/2^{15}$)
1 1	65.536 ms	32.768 ms	21.845 ms	($E/2^{16}$)
CR [1:0]	COP Watchdog Timeout Rates			
0 0	32.768 ms	16.384 ms	10.923 ms	($E/2^{15}$)
0 1	131.07 ms	65.536 ms	43.691 ms	($E/2^{17}$)
1 0	524.29 ms	262.14 ms	174.76 ms	($E/2^{19}$)
1 1	2.097 s	1.049 s	699.05 ms	($E/2^{21}$)
Timeout Tolerance (–0 ms/+...)	32.768 ms	16.4 ms	10.9 ms	($E/2^{15}$)

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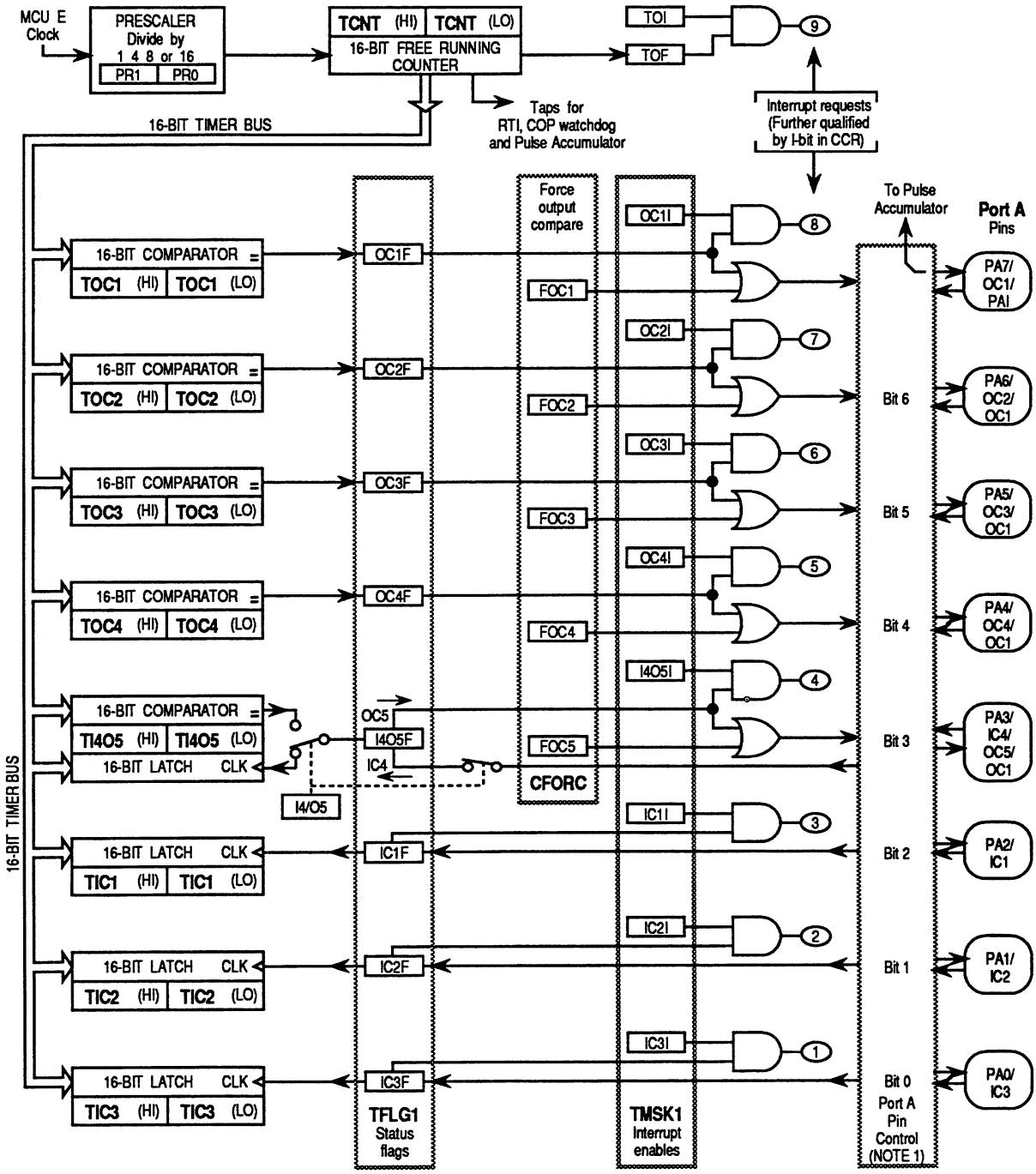

NOTE 1. Port A pin actions controlled by DDRA, OC1M, OC1D, PACTL, TCTL1, and TCTL2 registers.

Main Timer

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CFORC — Timer Compare Force **$100B**

	Bit 7	6	5	4	3	2	1	Bit 0
	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0
RESET:	0	0	0	0	0	0	0	0

FOC5–FOC1 — Force Output Compare x Action
0 = Not affected
1 = Output compare x action occurs, but OCxF flag bit is not set

Bits 2 – 0 — Not implemented; always read zero

OC1M — Output Compare 1 Mask **$100C**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0
RESET:	0	0	0	0	0	0	0	0

Set bit(s) to enable OC1 to control corresponding pin(s) of port A

OC1M7–OC1M3 — Output Compare Masks
0 = OC1 is disabled
1 = OC1 is enabled to control the corresponding pin of Port A.

Bits 2–0 — Not implemented; always read zero

OC1D — Output Compare 1 Data **$100D**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0
RESET:	0	0	0	0	0	0	0	0

If OC1Mx is set, data in OC1Dx is output to port A bit x on successful OC1 compares

Bits 2–0 — Not implemented; always read zero

TCNT — Timer Count **$100E, $100F**

$100E	Bit 15	14	13	12	11	10	9	Bit 8	High	**TCNT**
$100F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TCNT resets to $0000.
In normal modes, TCNT is read-only.

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TIC1–TIC3 — Timer Input Capture **$1010–$1015**

$1010	Bit 15	14	13	12	11	10	9	Bit 8	High	**TIC1**
$1011	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1012	Bit 15	14	13	12	11	10	9	Bit 8	High	**TIC2**
$1013	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1014	Bit 15	14	13	12	11	10	9	Bit 8	High	**TIC3**
$1015	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TICx not affected by reset

TOC1–TOC4 — Timer Output Compare **$1016–$101D**

$1016	Bit 15	14	13	12	11	10	9	Bit 8	High	**TOC1**
$1017	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1018	Bit 15	14	13	12	11	10	9	Bit 8	High	**TOC2**
$1019	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$101A	Bit 15	14	13	12	11	10	9	Bit 8	High	**TOC3**
$101B	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$101C	Bit 15	14	13	12	11	10	9	Bit 8	High	**TOC4**
$101D	Bit 7	6	5	4	3	2	1	Bit 0	Low	

All TOCx register pairs reset to ones ($FFFF)

TI4O5 — Timer Input Capture 4/Output Compare 5 **$101E, $101F**

$101E	Bit 15	14	13	12	11	10	9	Bit 8	High	**TI4O5**
$101F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

All TI4O5 register pairs reset to ones ($FFFF).

TCTL1 — Timer Control 1 **$1020**

	Bit 7	6	5	4	3	2	1	Bit 0
	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
RESET:	0	0	0	0	0	0	0	0

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OM2–OM5 — Output Mode

OL2–OL5 — Output Level

OMx	OLx	Action Taken on Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to 0
1	1	Set OCx output line to 1

TCTL2 — Timer Control 2 **$1021**

	Bit 7	6	5	4	3	2	1	Bit 0
	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
RESET:	0	0	0	0	0	0	0	0

Timer Control Configuration

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge

TMSK1 — Timer Interrupt Mask 1 **$1022**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1I	OC2I	OC3I	OC4I	I4O5I	IC1I	IC2I	IC3I
RESET:	0	0	0	0	0	0	0	0

OC1I–OC4I — Output Compare x Interrupt Enable

I4O5I — Input Capture 4 or Output Compare 5 Interrupt Enable

IC1I–IC3I — Input Capture x Interrupt Enable

NOTE

Bits in TMSK1 correspond bit for bit with flag bits in TFLG1. Ones in TMSK1 enable the corresponding interrupt sources.

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TFLG1 — Timer Interrupt Flag 1 **$1023**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1F	OC2F	OC3F	OC4F	I4O5F	IC1F	IC2F	IC3F
RESET:	0	0	0	0	0	0	0	0

Cleared by writing a one to the corresponding bit position(s).

OC1F–OC4F — Output Compare x Flag
Set each time the counter matches output compare x value.

I4O5F — Input Capture 4/Output Compare 5 Flag
Set by IC4 or OC5, depending on which function was enabled by I4O5 of PACTL.

IC1F–IC3F — Input Capture x Flag
Set each time a selected active edge is detected on the ICx input line.

TMSK2 — Timer Interrupt Mask 2 **$1024**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt Enable

RTII — Real-Time Interrupt Enable

PAOVI — Pulse Accumulator Overflow Interrupt Enable

PAII — Pulse Accumulator Interrupt Enable

NOTE

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

Bits 3–2 — Not implemented; always read zero

PR1 and PR0 — Timer Prescaler Select
In normal modes, PR1 and PR0 can only be written once, and the write must be within 64 cycles after reset. Refer to timer summary table for specific timing values.

PR [1:0]	Prescaler
0 0	1
0 1	4
1 0	8
1 1	16

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TFLG2 — Timer Interrupt Flag 2 **$1025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Cleared by writing a one to the corresponding bit position(s)

TOF — Timer Overflow Flag
Set when TCNT changes from $FFFF to $0000

RTIF — Real-Time (Periodic) Interrupt Flag
Set periodically (See RTR1:0 bits in PACTL register)

PAOVF — Pulse Accumulator Overflow Flag
Set when PACNT changes from $FF to $00

PAIF — Pulse Accumulator Input Edge Flag
Set each time a selected active edge is detected on the PAI input line

Bits 3–0 — Not implemented; always read zero

PACTL — Pulse Accumulator Control **$1026**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	PAEN	PAMOD	PEDGE	0	I4O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

Bits 7 and 3 — Not implemented; always read zero

Bits 6–4 and 2 — Refer to **Pulse Accumulator.**

RTR1–RTR0 — RTI Interrupt Rate Selects
These two bits select one of four rates for the real-time periodic interrupt circuit. Refer to the following table for additional detail.

Real-Time Interrupt Rates

RTR [1:0]	Divide E By	XTAL = 4.0 MHz	XTAL = 8.0 MHz	XTAL = 12.0 MHz
0 0	2^{13}	8.19 ms	4.096 ms	2.731 ms
0 1	2^{14}	16.38 ms	8.192 ms	5.461 ms
1 0	2^{15}	32.77 ms	16.384 ms	10.923 ms
1 1	2^{16}	65.54 ms	32.768 ms	21.845 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz

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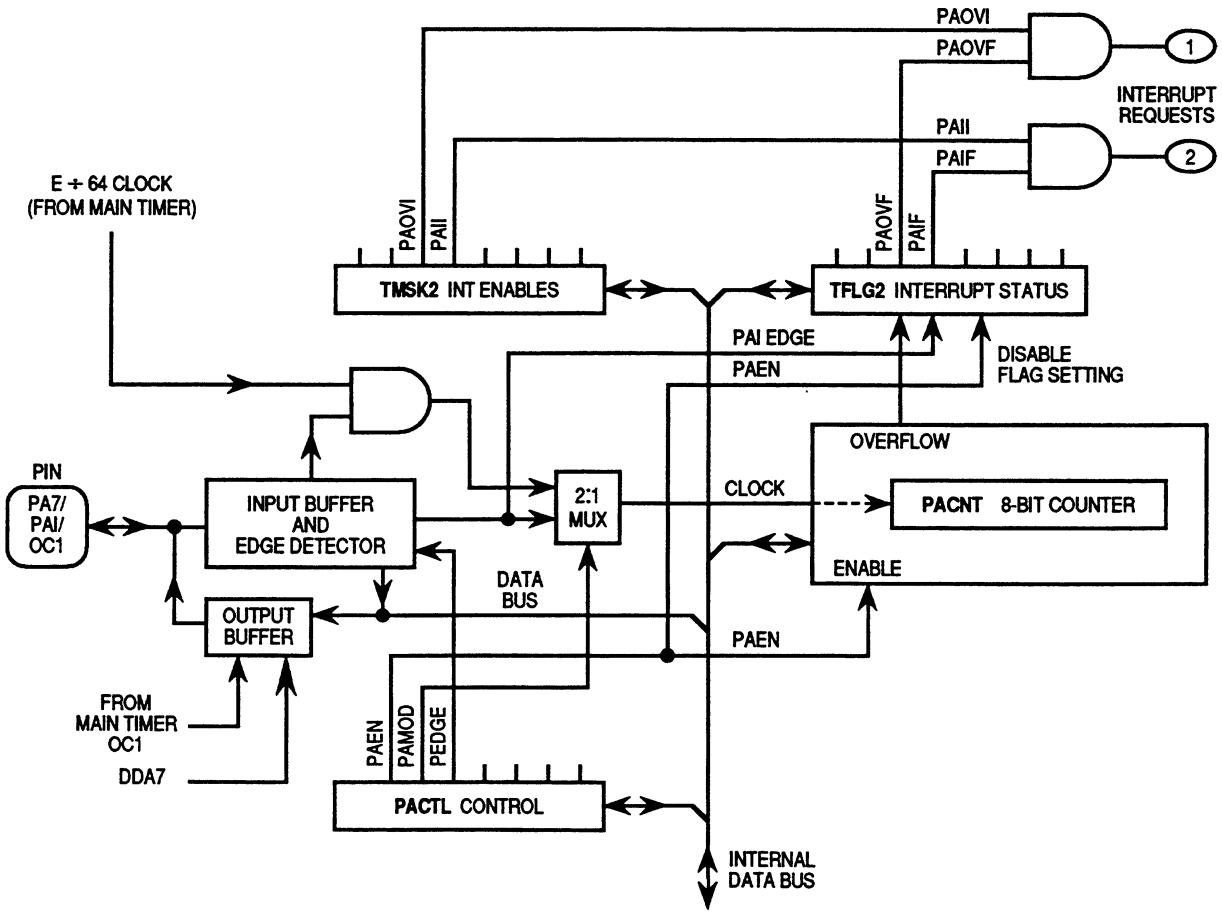
Pulse Accumulator

The MC68HC711J6 has an 8-bit counter that can be configured to operate as a simple event counter or as a gated time accumulator, depending on the PAMOD bit in the PACTL register. The pulse accumulator counter can be read or written at any time. The port A, bit 7, I/O pin can be configured as a clock in event counting mode, or as a gate signal to enable a free-running clock (E divided by 64) in gated time accumulation mode.

Pulse Accumulator Timing

	Selected Crystal	Common XTAL Frequencies		
		4.0 MHz	8.0 MHz	12.0 MHz
CPU Clock	**(E)**	**1.0 MHz**	**2.0 MHz**	**3.0 MHz**
Cycle Time	**(1/E)**	**1000 ns**	**500 ns**	**333 ns**
Pulse Accumulator (in Gated Mode)				
$(E/2^6)$ $(E/2^{14})$	1 count overflow	64.0 µs 16.384 ms	32.0 µs 8.192 ms	21.33 µs 5.461 ms



Pulse Accumulator Block Diagram

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TMSK2 — Timer Interrupt Mask 2 **$1024**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

For a description of bits 7–6 and 1–0, refer to **Main Timer.**

PAOVI — Pulse Accumulator Overflow Interrupt Enable
0 = Pulse accumulator overflow interrupt disabled
1 = Interrupt requested when bit PAOVF of TFLG2 is set

PAII — Pulse Accumulator Interrupt Enable

NOTE

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2.
Ones in TMSK2 enable the corresponding interrupt sources.

Bits 3–2 — Not implemented; always read zero

TFLG2 — Timer Interrupt Flag 2 **$1025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Cleared by writing a one to the corresponding bit position(s). For a description of bits 7–6, refer to **Main Timer.**

PAOVF — Pulse Accumulator Overflow Flag
Set when PACNT changes from $FF to $00.

PAIF — Pulse Accumulator Input Edge Flag
Set each time a selected active edge is detected on the PAI input line.

Bits 3–0 — Not implemented; always read zero

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PACTL — Pulse Accumulator Control **$1026**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	PAEN	PAMOD	PEDGE	0	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

Bits 7 and 3 — Not implemented; always read zero

PAEN — Pulse Accumulator System Enable
- 0 = Pulse Accumulator disabled
- 1 = Pulse Accumulator enabled

PAMOD — Pulse Accumulator Mode
- 0 = Event counter
- 1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control
- 0 = Falling edges increment counter: high level enables accumulation
- 1 = Rising edges increment counter: low level enables accumulation

For a description of bits 2–0, refer to **Main Timer.**

PACNT — Pulse Accumulator Count **$1027**

Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0
U	U	U	U	U	U	U	U

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