# Multi-layer ceramic chip capacitors

# MCH02 (0402 (01005) size, chip capacitor)

#### Features

- 1) The world's smallest (0.4mm x 0.2mm), Ultra thin (0.2mm), Ultra light (0.08mg)
- 2) Suitable for mobile end products
- 3) Lead-free plating terminal
- 4) No polarity

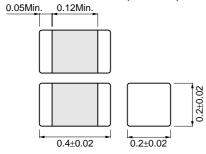
#### Quick Reference

The design and specifications are subject to change without prior notice. Please check the most recent technical specifications prior to placing orders or using the product. For more detail information regarding packaging style code, please check product designation.

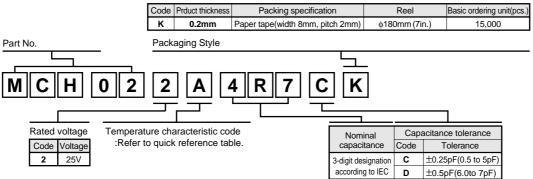
Thermal compensation

	Part No.	Size code	Tempera	ature characteristics (ppm/°C)	Operating temp. range (°C)	Rated voltage (V)	Capacitance(pF)	Capacitance tolerance	Thickness (mm)
New	MCH02	0402	A	0±250(CK)	-55 to +125	25 0.5 to 2.0 3.0 4.0 to 5.0	0.5 to 2.0	C(±0.25pF)	
				0±120(CJ)			3.0		
				0±60(CH)			4.0 to 5.0		0.2±0.02
							6.0 to 7.0	D(±0.5pF)	

#### ●External dimensions (Unit : mm)



# Product designation



#### **Product No. list**

#### ● Capacitance range

#### Thermal compensation

Canacitanas	Temp	erature	A · (CH) (CJ) (CK)Characteristics		
Capacitance (pF)	Rated vo	oltage (V)	25V		
(pi )	Tolerance	Product thickness (mm)	Product No.		
0.5	C(±0.25PF)	0.2 ± 0.02	MCH022A 0R5CK		
1.0			MCH022A 010CK		
2.0			MCH022A 020CK		
3.0			MCH022A 030CK		
4.0			MCH022A 040CK		
5.0			MCH022A 050CK		
6.0			MCH022A 060DK		
7.0	D(±0.5PF)		MCH022A 070DK		

## Performance and test method

No.	Items Performance		Test Method (As per JIS C 5101-1, JIS C 5101-10)		
1	Appearance and dimensions	No marked defects shall be allowed for appearance. Dimensions shall be as specified in the clause 4.	As per 4.4 of JIS C 5101-1. As per 4.5 of JIS C 5101-10 Using a Magnifier.		
2	Withstanding voltage	No dielectrical breakdown or other damage shall be allowed.	As per 4.6 of JIS C 5101-1. As per 4.6.4 of JIS C 5101-10 Voltage shall be applied as per Table1.  Table 1  Voltage  300% Rated voltage  Voltage shall be applied for 1 to 5s with 50mA charging and discharging curent.		
3	Insulation resistance	More than 10000MΩ	As per 4.5 of JIS C 5101-1. As per 4.6.3 of JIS C 5101-10 Measurements shall be made after 60+/-5s period of the rated voltage applied.		
4	Capacitance	Capacitance shall be within specified tolerance range.	As per 4.7 of JIS C 5101-1. As per 4.6.1 of JIS C 5101-10 Measurements shall be made under the conditions specified in Table 2.  Table 2  Frequency · Voltage  1+/-0.1MHz  1+/-0.1Vrms.		
5	Dielectric loss tangent	tan δ ≤ 100/(400+20 ⋅ C) ∗C=Capacitance(pF)	As per 4.8 of JIS C 5101-1 As per 4.6.2 of JIS C 5101-10 Measurements shall be made under the conditions specified in Table 2.		
6	Temperature characteristic	0+/-250ppm / °C (0.5 to +2pF) 0+/-120ppm / °C (3pF) 0+/-60ppm / °C (4 to +7pF) (-55°C to +125°CpF)	As per 4.24 of JIS C 5101-1. As per 4.7 of JIS C 5101-10 Temperature coefficient shall be calculated at 20°C and 85°C.		
7	Solderability	More than 3/4 of each end termination shall be covered with new solder.	As per 4.15.2 of JIS C 5101-1. As per 4.11 of JIS C 5101-10 The solder specified in JIS Z 3282 H63A shall be used. And the flux containing 25% rosin and ethanol solution shall be used. The specimens shall be immersed into the solder at 235+/-5°C for 2+/-0.5s So that both end terminations are completely under solder.		

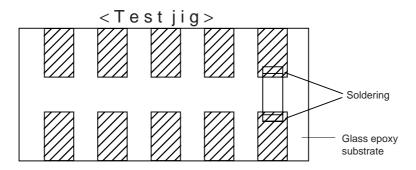


No.	Items		Performance	Test Method (As per JIS C 5101-1, JIS C 5101-10)
8	Resistance to solderin heat	Appearance	Without mechanical damage.	As per 4.14 of JIS C 5101-1. As per 4.10 of JIS C 5101-10 The solder specified in JIS Z 3282. H63A
		Change rate from initial value	Within +/-0.25pF	shall be used. The specimens shall be immersed into the solder at 260+/-5°C for 5+/-0.5s so that
		Dielectric loss tangent	Within specified initial value.	both end terminations are completely under the solder.  Pre-heating at 150+/–10°C for 1 to 2min Initial measurements prior to test shall be
		Insulation resistance	Within specified initial value.	performed after the thermal Pre-conditioning specified in Remarks (1). Final measurements shall be made after the specimens have been left at room
		Withstanding voltage	No defects shall be allowed.	temperature as per Table3.  Table3  Time  24+/-2 h
9	9 End termination adherence		Without peeling or sign of peeling shall be allowed on the end terminations.	As per 4.13 of JIS C 5101-1. As per 4.8 of JIS C 5101-10 A 1N weight for 10+/-1s shall be applied to the soldered specimens as shown by the arrow mark in the below sketch.  Applied pressure  Substrate
10	Bending strength	Appearance	Without mechanical damage.	As per 4.35 of JIS C 5101-1. As per 4.9 of JIS C 5101-10
	an en gar	Change rate from initial value	Within +/-0.5pF	Glass epoxy board with soldered specimens shall be bent till 1mm by 1.0mm/s.
11	Vibration	Appearance	Without mechanical damage.	As per 4.17 of JIS C 5101-1. The specimens shall be soldered on the
		Change rate from initial value	Within +/-0.25pF	specified test jig. Final measurements shall be made after the specimens have been left at room
		Dielectric loss tangent	Within specified initial value.	temperature as per Table3.  [Condition]  Directions : 2h each X, Y and Z directions

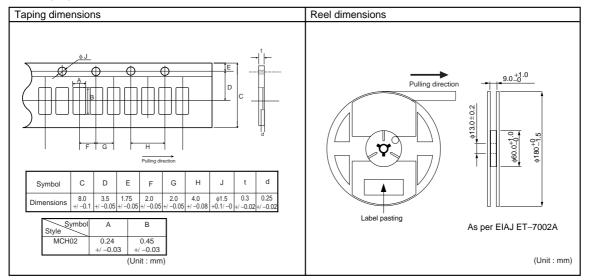
No.	Items		Performance	Test Method (As per JIS C 5101-1, JIS C 5101-10)			
12	Temperature cycling	Change rate from	Without mechanical damage.  Within +/-0.25pF	As per 4.16 of JIS C 5101-1. As per 4.12 of JIS C 5101-10 The specimens shall be soldered on the te jig shown in Remarks. Temperature cycle: 100cycles.			
		Dielectric loss tangent	Within specified initial value.	Final measurements shall be made after the specimens have been left at room temperature as per Table3.  Test condition			
		Insulation resistance	Within specified initial value.	Step         Temp. (°C)         Time (min)           1         Min operating temp.         30+/-3           2         Room temp.         ≤ 3			
		Withstanding voltage	No defects shall be allowed.	3 Max operating temp. 30+/-3 4 Room temp. ≤ 3  Table3			
				Time 24+/–2 h			
13	Humidity (Steady)	Appearance Change rate from initial value	Without mechanical damage.  Within +/-5.0pF	As per 4.22 of JIS C 5101-1  JIS C 5101-10  Test temperature: 60+/-2°C  Relative humidity: 90 to 95%  Test time: 500 +24/-0 h  Final measurements have been left at room temperature as per Table3.  Table3			
		Dielectric tangent	tan δ ≤ 100/(200+10 · C) *C=Capacitance(pF)				
		Insulation resistance	More than 1000MΩ	Time 24+/–2 h			
14	Humidity life test	Appearance	Without mechanical damage.	As per 4.22 of JIS C 5101-1 As per 4.14 of JIS C 5101-10 Test temperature: 60+/-2°C Relative humidity: 90 to 95% Voltage: Rated voltage			
	life test	Change rate from initial value	Within +/-0.75pF				
		Dielectric tangent	tan $\delta \le 100/(100+10 \cdot C/3)$ *C=Capacitance(pF)	Test time : 500 +24/–0 h Final measurements shall be made after the specimens have been left at room			
		Insulation resistance	More than $500 M\Omega$	temperature as per Table3.  Table3  Time  24+/-2 h			
15	Heat life test	Appearance	Without mechanical damage.	As per 4.23 of JIS C 5101-1.  As per 4.15 of JIS C 5101-10			
		Change rate from initial value	Within +/-0.3pF	Test temperature(°C) Voltage time (h)			
		Dielectric tangent	tan $\delta \le 100/(100+10 \cdot C)$ *C=Capacitance(pF)	125 200% Rated voltage +48/-0			
		Insulation resistance	More than 1000MΩ	Final measurements shall be made after the specimens have been left at room temperature  Table3  Time  24+/-2 h			



[Remarks]



# Packaging specification



## •Electrical characteristics curves

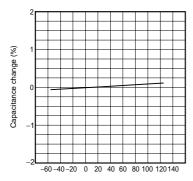


Fig.1 Temperature (°C)

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