Discontinued Product

OKI Semiconductor

This version: Jun. 1999
Previous version: Jun. 1998

MSM7653

NTSC/PAL Digital Video Encoder

GENERAL DESCRIPTION

The MSM7653 is a digital NTSC/PAL encoder. By inputting digital image data conforming to ITU Rec. 656 or ITURBT 601, it outputs selected analog composite video signals, analog S video signals. For the scanning system, interlaced or noninterlaced mode can be selected.
Since the MSM7653 is provided with pins dedicated to overlay function, text and graphics can be superimposed on a video signal.
In addition, this encoder has an internal 10-bit DAC. So, when compared with using a conventional analog encoder, the number of components, the board space, and points of adjustment can greatly be reduced, thereby realizing a low cost and high-accuracy system.
The MSM7653 provides the optional functions such as Macrovision Rev. 7.01 (note 1) (note 2) and Closed Caption Signal Generation Function.
The host interface provided conforms to Philips's I²C specifications, which reduces interconnections between this encoder and mounting components.
The internal synchronization signal generator (SSG) allows the MSM7653 to operate in master mode.

FEATURES

- Video signal system: NTSC/PAL
- Scanning system: interlaced/noninterlaced (NTSC : 262 lines/PAL : 312 lines)
- Input digital level: conforms to ITU-R601 (CCIR601)
- Input-output timing: conforms to ITU Rec. 656 or ITURBT 624-4
- Input signal sampling ratio : Y:Cb:Cr = 4:2:2
- Supported input formats
  · ITU Rec. 656
  · YCbCr 27 MHz format (8-bit input)
  · ITU-R601 13.5 MHz (8-bit (Y) + 8-bit (CbCr) input)
- Sampling frequency : 27 MHz
- Internal SSG circuit (Can operate as a master in other operation modes than CCIR Rec. 656 mode)
- Internal 3ch 10-bit DAC
- 3-bit title graphics can be displayed
- Color bar function
- I²C-bus host interface function
- 3.3 V single power supply (each I/O pin is 5 V tolerable)
- Closed caption function
- Macrovision Rev. 7.01
- Package
  56-pin plastic QFP (QFP56-P-910-0.65-2K) (Product name: MSM7653GS-2K)

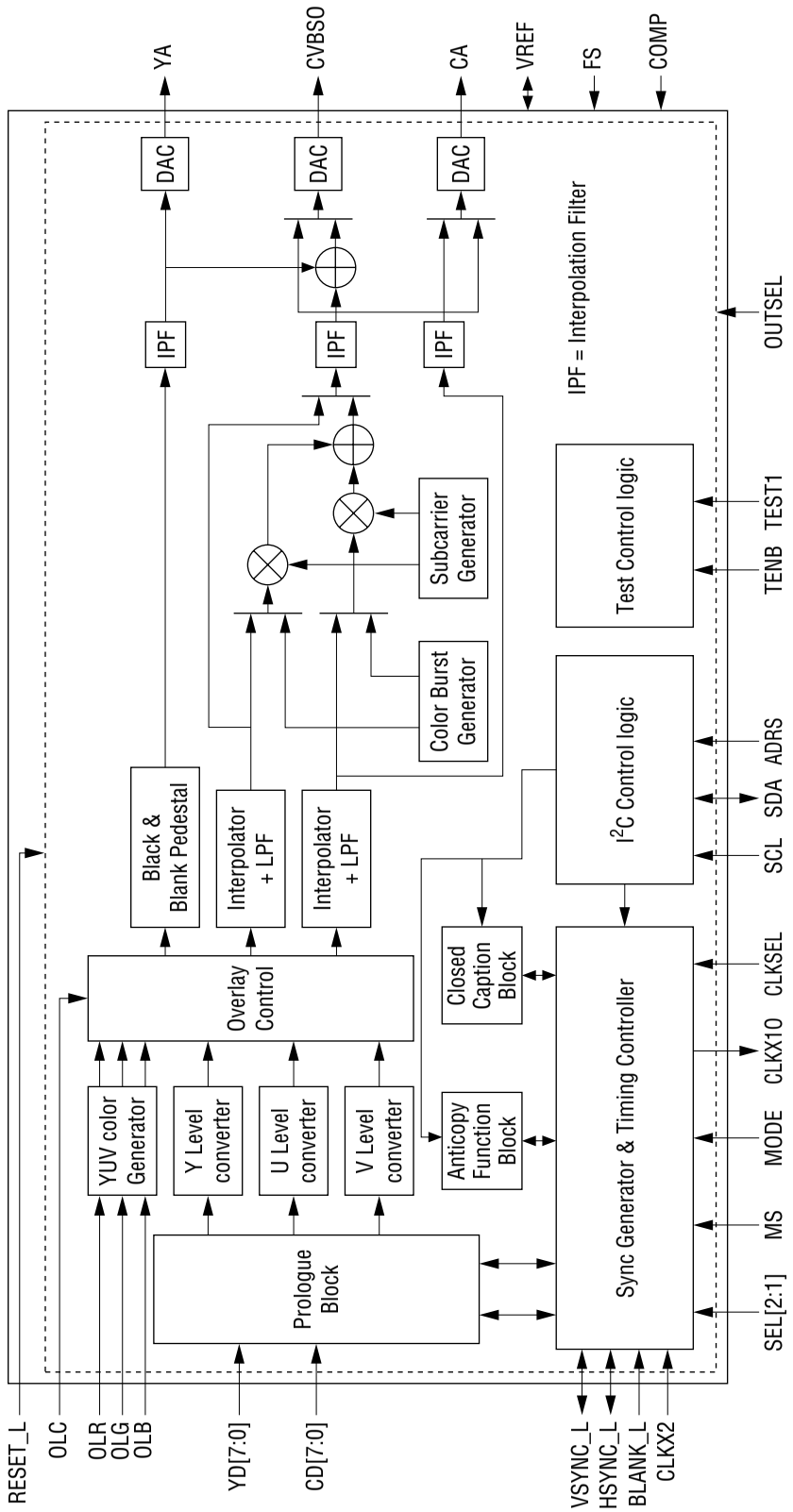
APPLICATIONS

- Set top box
- DVD
- Digital VTR

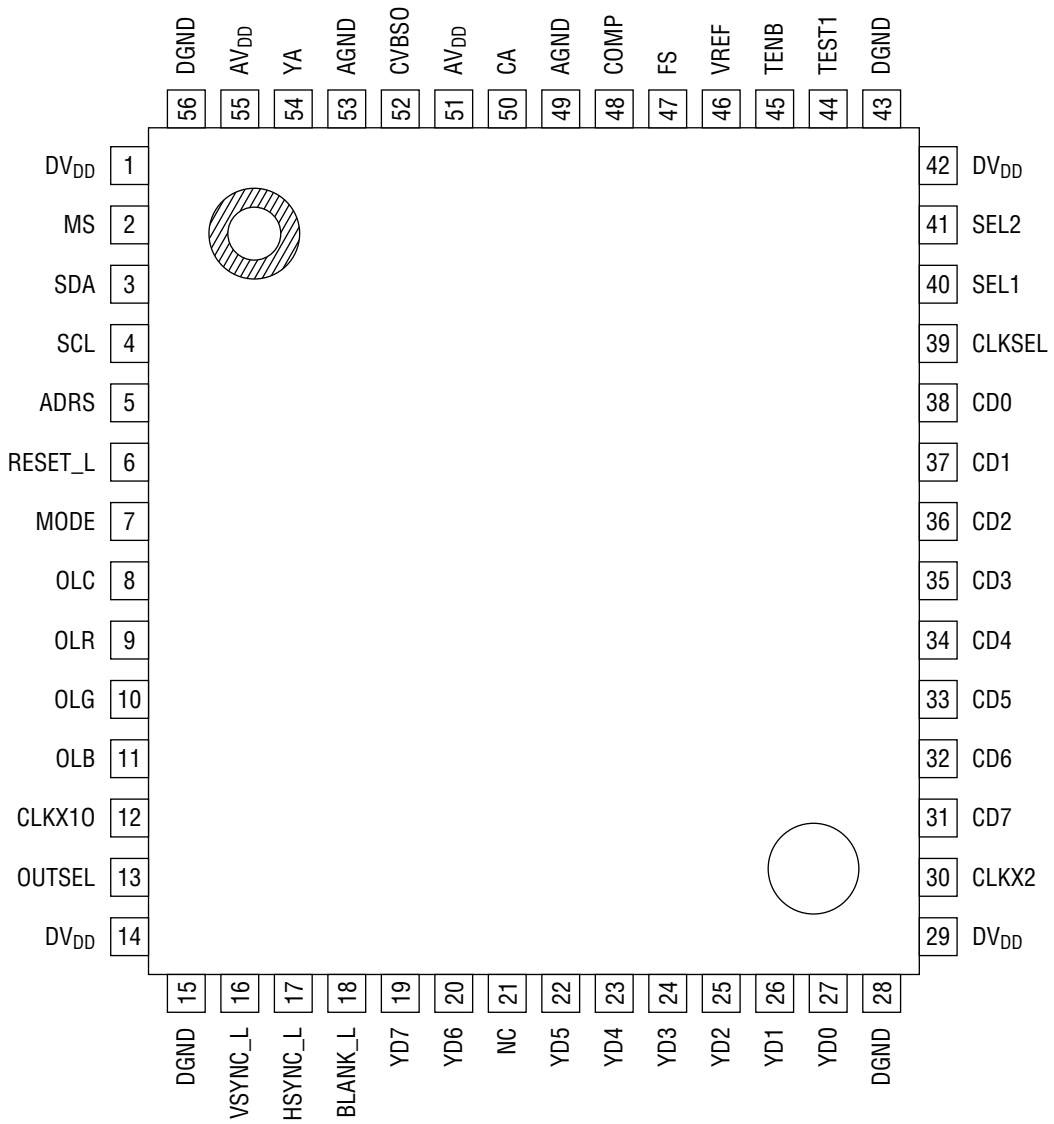
(Note 1) This device is protected by U.S. Patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. The use of Macrovision Corporation's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view uses only, unless otherwise authorized in writing by Macrovision. Reverse engineering or disassembly is prohibited.

(Note 2) This data sheet does not describe the register setting method of implementing Macrovision Corporation's anticopy function that this device provides.
Refer to MACROVISION ANTICOPY FUNCTION SETTING MANUAL for the anticopy function.

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC : No-connection pin

56-Pin Plastic QFP

PIN DESCRIPTIONS (1/2)

Pin	I/O	Symbol	Description
1		DV_{DD}	3.3 V digital power supply
2	I	MS	Selects between Master and Slave at 27 MHz or 13.5 MHz YCbCr operation. Pulled down
3	I/O	SDA	I^2C interface data bus
4	I	SCL	I^2C interface clock bus
5	I	ADRS	I^2C-bus Slave address setting pin ("0" : 1001100 / "1" : 1001110). Pulled down
6	I	RESET_L	System reset signal. Negative porality
7	I	MODE	Broadcasting mode select pin. "0" : NTSC/"1" : PAL. Pulled down
8	I	OLC	Transparent control signal. "1" indicates overlay signal. Normally fixed to "0".
9	I	OLR	Overlay text color (Red component). Normally fixed to "0".
10	I	OLG	Overlay text color (Green component). Normally fixed to "0".
11	I	OLB	Overlay text color (Blue component). Normally fixed to "0".
12	O	CLKX1O	13.5 MHz divided clock output signal
13	I	OUTSEL	Normally fixed to "0". Pulled down
14		DV_{DD}	3.3 V digital power supply
15		DGND	Digital GND
16	I/O	VSYNC_L	Vertical sync signal input/output pin (ITU656: O, YCbCr: I/O) Negative polarity
17	I/O	HSYNC_L	Horizontal signal input/output pin (ITU656 : O, YCbCr: I/O) Negative polarity
18	I	BLANK_L	Composite blank signal. Negative polarity. See the description on page 15 for the operating requirement.
19, 20	I	YD7 to YD6	MSB 2 bits of 8-bit digital image data input pins (for ITU656 and YCbCr 27 MHz). Level conforms to ITU-601. MSB 2 bits of 8-bit digital image luminance signal input pins (for YCbCr). Level conforms to ITU-601. YD7 is MSB.
21		NC	Not connected
22 to 27	I	YD5 to YD0	LSB 6 bits of 8-bit digital image data input pins (for ITU656 and YCbCr 27 MHz). Level conforms to ITU-601. LSB 6 bits of 8-bit digital image luminance signal input pins (for YCbCr). Level conforms to ITU-601. YD0 is LSB.
28		DGND	Digital GND
29		DV_{DD}	3.3 V digital power supply
30	I	CLKX2	Clock input pin (27 MHz)
31 to 38	I/O	CD7 to CD0	8bit digital image chrominance signal data input pins (13.5 MHz mode). Level conforms to ITU-601. Fixed to "0" for ITU Rec. 656, 27 MHz-YCbCr mode.
39	I	CLKSEL	Operation mode select pin. "0" : 27 MHz mode / "1" : 13.5 MHz mode.

PIN DESCRIPTIONS (2/2)

Pin	I/O	Symbol	Description
40	I	SEL1	Enable pin. Normally fixed to "0". Sleep mode "1" with TEST1 = "0" (See Page 32 for details)
41	I	SEL2	Interface select pin. ITU656 : "0", YCbCr 27 MHz : "1" (See Page 32 for details) Pulled down
42		DV_{DD}	3.3 V digital power supply
43		DGND	Digital GND
44	I	TEST1	Input pin1 for testing. Normally fixed to "0". (See Page 32 for details) Pulled down
45	I	TENB	Input pin2 for testing. Normally fixed to "0". Pulled down
46	I/O	VREF	Reference voltage for DAC
47	I	FS	DAC full scale adjustment pin.
48	I	COMP	DAC phase complement pin.
49		AGND	Analog GND
50	O	CA	Analog color chrominance signal output pin.
51		AV_{DD}	3.3 V analog power supply
52	O	CVBSO	Analog composite signal output pin.
53		AGND	Analog GND
54	O	YA	Analog luminance signal output pin.
55		AV_{DD}	3.3 V analog power supply
56		DGND	Digital GND

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	DV_{DD}	—	–0.3 to +4.5	V
	AV_{DD}	—	–0.3 to +4.5	
Input Voltage	V_I	DV_{DD} = 3.3 V	–0.3 to +5.5	V
Analog Output Current	I_O	—	50	mA
Power Consumption	P_W	—	600	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage (*1)	DV_{DD}	—	3.0	3.3	3.6	V
	AV_{DD}	—	3.0	3.3	3.6	
"H" Level Input Voltage	V_{IH}	—	2.2	—	—	V
"L" Level Input Voltage	V_{IL}	—	—	—	0.8	V
Operating Temperature 1	Ta1	DV_{DD} = AV_{DD} = 3.3 V	0	25	70	˚C
Operating Temperature 2	Ta2	DV_{DD} = AV_{DD} = 3.3 V DA output load = 37.5 Ω	0	25	65	˚C
External Reference Voltage	Vrefex	DV_{DD} = AV_{DD} = 3.3 V, Ta = 25˚C	—	1.25	—	V
DA Current Setting Resistance	Riadj	(*2)	—	385	—	Ω
DA Output Load Resistance	R_L	(*3)	—	75	—	Ω

(*1) Supply an equal voltage to both DV_{DD} and AV_{DD}.

(*2) A volume control resistor of approx. 500 Ω is recommendable for adjusting the output current. When a DA converter analog output is terminated with a 37.5 Ω load, Riadj = approx. 192 Ω.

(*3) Indicates the value when Riadj = 385 Ω (typical value).

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = 0 to 70°C, DV_{DD} = 3.3 V ±0.3 V, AV_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Level Output Voltage	V_{OH}	I_{OH} = –4 mA (*1)	0.7V_{DD}	—	—	V
"L" Level Output Voltage	V_{OL}	I_{OL} = 4 mA (*1) I_{OL} = 6 mA (*2)	—	—	0.4	V
Input Leakage Current	I_I	V_I = GND to DV_{DD}	–10	—	+10	µA
Output Leakage Current	I_O	V_I = GND to DV_{DD} (*3)	–10	—	+10	µA
Power Supply Current (operating)	I_{DDO}	—	—	120	140	mA
Power Supply Current (standby)	I_{DDS}	RESET_L = "L" CLKX2 = 0 MHz	—	60	65	mA
Power Supply Current (Sleep mode)	I_{DDSM}	SEL2 = "H"	0.03	0.05	0.5	mA
I²C-bus SDA Output Voltage	$SDAV_L$	Low level, I_{OL} = 3 mA	0	—	0.4	V
I²C-bus SDA Output Current	$SDAI_O$	During Acknowledge	3	—	—	mA
Internal Reference Voltage	Vrefin	—	—	1.25	—	V
DA Output Load Resistance	R_L	—		75		Ω
Integral Linearity	SINL	—		±2		LSB
Differential Linearity	SDNL	—		±1		LSB

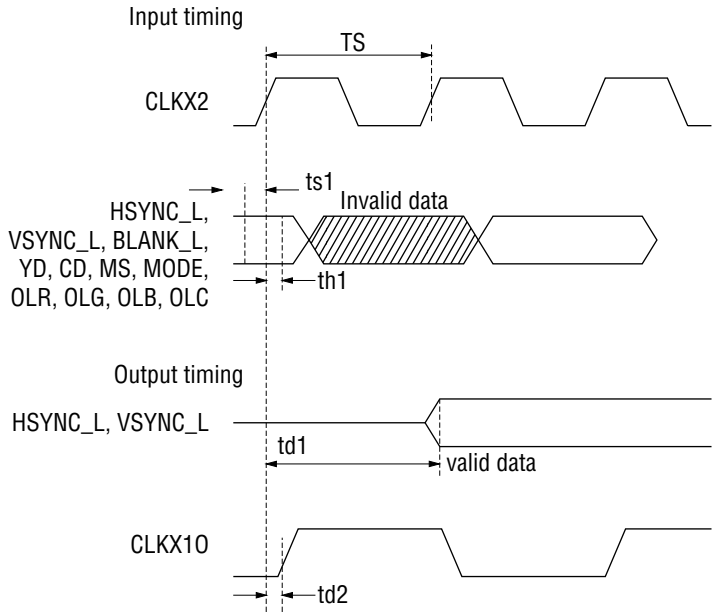
(*1) VSYNC_L, HSYNC_L, CD[7:0]
(*2) CLKX1O
(*3) SDA

AC Characteristics

(Ta = 0 to 70°C, DV_{DD} = 3.3 V ±0.3 V, AV_{DD} = 3.3 V ±0.3 V)

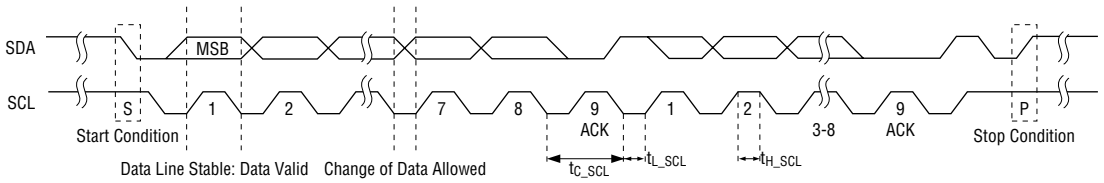
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKX2 Cycle Time	T_S	—	—	37.0	—	ns
Input Data Setup Time	t_{s1}	—	7	—	—	ns
Input Data Hold Time	t_{h1}	—	5	—	—	ns
Output Delay Time	t_{d1}	—	5	—	25	ns
CLKX1O Delay Time	t_{d2}	—	5	—	25	ns
I²C-bus Clock Cycle Time	t_{C_SCL}	Rpull_up = 4.7 kΩ	200	—	—	ns
I²C-bus High Level Cycle	t_{H_SCL}	Rpull_up = 4.7 kΩ	100	—	—	ns
I²C-bus Low Level Cycle	t_{L_SCL}	Rpull_up = 4.7 kΩ	100	—	—	ns

INPUT/OUTPUT TIMING



I²C-bus Interface Input/Output Timing

The following figure shows I²C-bus basic input/output timing.



I²C-bus Basic Input/Output Timing

BLOCK FUNCTIONAL DESCRIPTION

1. Prologue Block

This block separates input data at the ITU Rec.656 format into a luminance signal (Y) and a chrominance signal (Cb & Cr), and also generates information/concerning sync signals HSYNC_L, VSYNC_L, and BLANK_L.
This block separates input data at the 27 MHz YCbCr (8-bit input) format into a luminance signal (Y) and a chrominance signal (Cb & Cr).
This block separates input data at the 13.5 MHz YCbCr (16-bit input) format into a chrominance signal Cb and a chrominance signal Cr.
Of the processed input data, luminance and chrominance signals other than valid pixel data are replaced by 8'h10 and 8'h80 respectively.

2. Y Limiter Block

This block limits the luminance input signal by clipping the lower limit of an input signal outside the ITU601 Standard

- Signals are limited to YD = 16 when YD < 16.
- Signals are limited to TD = 254 when YD (input during a valid pixel period) = 255.

In other cases, signals are fed as is to next processing.

3. C Limiter Block

This block limits the chrominance signal by clipping the upper and lower limits of the input signal outside the ITU601 Standard.
CD = 1 when CD = 0 is input during a valid pixel period.
CD = 254 when CD = 255 is input during a valid pixel period.

- **Y Level Converter**
  Converts ITU-601 standard luminance signal level to DAC digital input level.

- **U Level Converter**
  Converts ITU-601 standard chrominance signal level to DAC digital input level.

- **V Level Converter**
  Converts ITU-601 standard chrominance signal level to DAC digital input level.

- **YUV Color Generator**
  This block generates luminance and chrominance signals from over lay color signals OLR, OLG and OLB. Control signals (CR [2:0]) control the output content (overlay or color bar) and output level (100%, 75%, 50%, 25%).

- **Overlay Control**
  This block selects input image data or YUV Color Generator output signals.
  It is determined by the level of the control signal (OLC, CR [2]), as shown below: (x : don't care)
  CR [2] = 1, OLC = x: Selects color bar signal (YUV Color Generator output signal).
  CR [2] = 0, OLC = 1: Selects overlay signal (YUV Color Generator output signal).
  CR [2] = 0, OLC = 0: Selects input image data.

- **Black & Blank Pedestal**
  This block adds sync signals at the luminance side to luminance signals.

- **Interpolator + LPF**
  This block executes data interpolation and the elimination of high frequency components by LPF for input chrominance signals.

- **I²C Control Logic**
  This is the serial interface block based on I²C standard of Phillips Corporation.
  Internal registers MR and CR can be set from the master side.
  When writing to the internal registers other than MR [2] (black level control) and CR [1:0] (overlay level), written contents are immediately set to them. It is during the vertical blanking period that written contents are set to MR [2] and CR [1:0].

- **Sync Generator & Timing Controller**
  This block generates sync signals and control signals.
  This block operates in slave mode, which performs external synchronization, and in master mode, which internally generates sync signals.

- **Color Burst Generator**
  Outputs U and V components of amplitude of burst signals.

- **Subcarrier Generator**
  Executes color subcarrier generation.

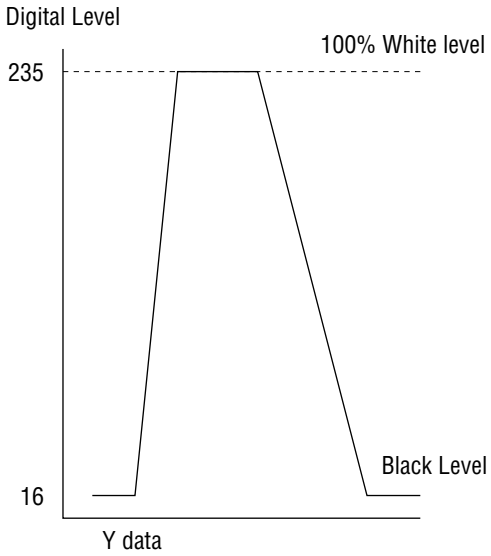
- **Interpolation Filter (IPF)**
  This block performs upsampling at CLKX2 (double speed CLKX1) for luminance signals and chrominance signals modulated with CLKX1. Interpolation processing is executed in this process.

- **Closed Caption Block**
  This block generates the signal for closed caption.

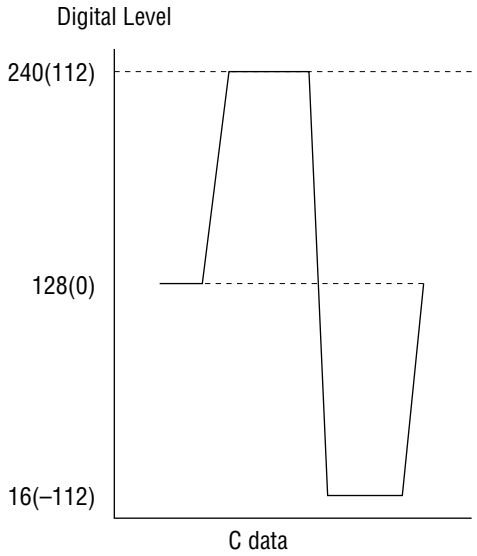
- **Anticopy Function Block**
  This block generates a macrovision anticopy signal.

INPUT DATA FORMAT

The signal level specified by the ITU601 is input.
When other signal levels than specified by the ITU601 are input, the luminance signal level is clipped to 16 to 254 and the chrominance signal level to 1 to 254.
For chrominance signal input, the offset binary and 2's complement formats are available by setting of internal registers.



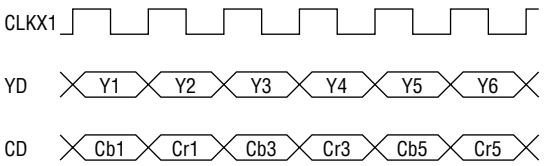
Input luminance signal level



Input chrominance signal level

Basic Pixel Sampling Ratio

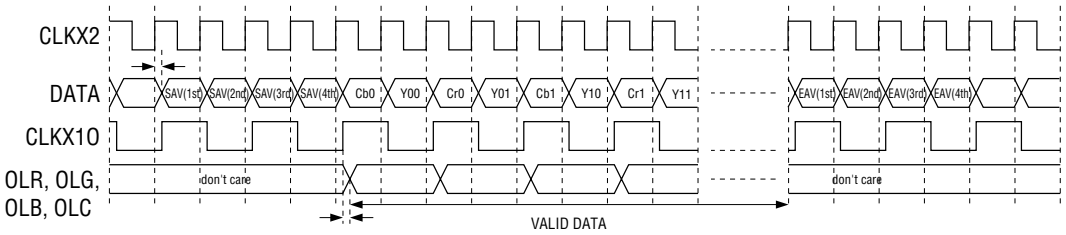
4:2:2 is supported.



4:2:2 sampling
at 8bit Y/8bit CbCr input

INPUT TIMING (ITUR656 input)

The input data is fed in the encoder at the rising edge of a clock pulse.



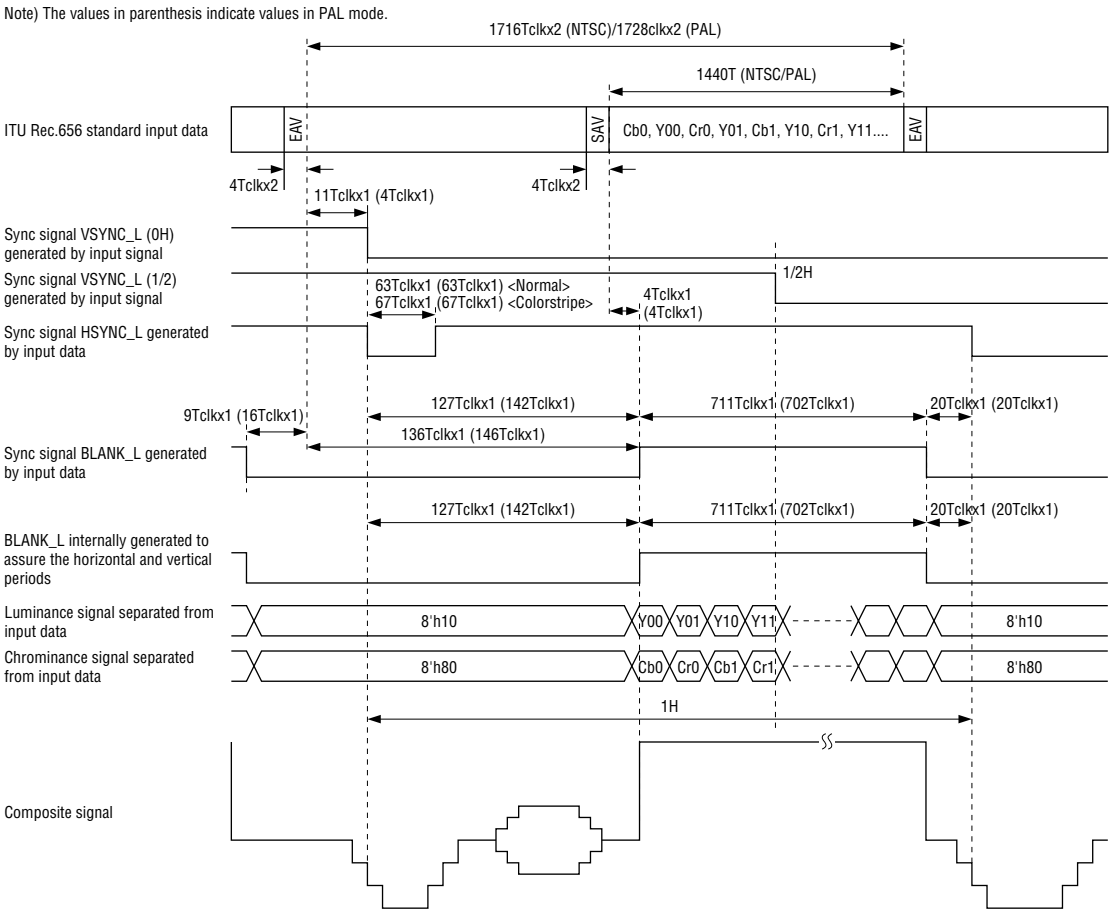
Input Timing

RELATIONSHIP BETWEEN BLANK SIGNAL AND INPUT IMAGE DATA

The blank signal is generated by the ITU Rec.656 standard input data. The input image data is valid when the blank signal is "H".

VALID DATA RANGE

According to the ITU Rec.656 standard, the pixel data immediately from SAV (4th word) to a fixed value before EVA is valid.
The following figure shows the relationship between the input data at the CCIR Rec.656 format and the sync, luminance, chrominance signals which are processed inside the encoder.



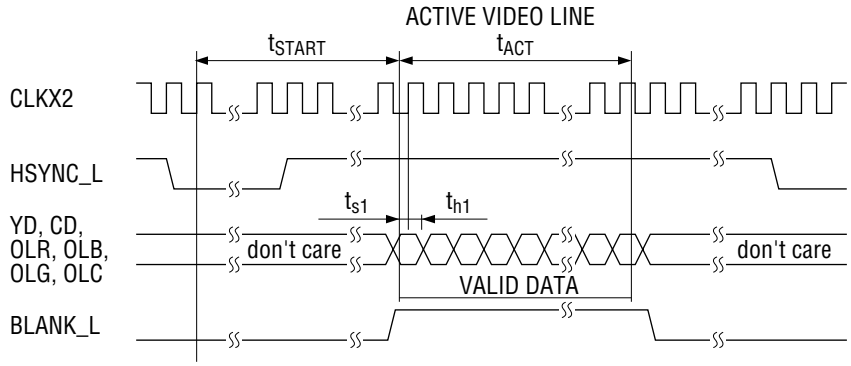
Relationship between input data and sync signal, luminance signal, chrominance signals

CLOCK TIMING2 (8bit Y/8bit CbCr input)

Input Data Timing

Input data and sync signals are fed into the encoder at the rising edge of CLKX2.

Input data is handled as valid pixel data when t_{START} passes after the falling edge of HSYNC_L. Chrominance signal of input data at this time is regarded as Cb.



Video data input timing

Input data is recognized as valid pixel data when input signal BLANK_L is "H" in the t_{ACT} period. When BLANK_L is "H" during the blanking period, however, input data is not output as valid pixel data since processing to maintain blanking period is internally in-progress.

The values of t_{START} differ slightly between in master mode and in slave mode. The values of t_{START} are as follows.

In YCbCr format input mode, the values of t_{START} are the same, in 8 bit (Y) + 8 bit (CbCr) mode or in 8 bit (YCbCr) mode.

In master mode

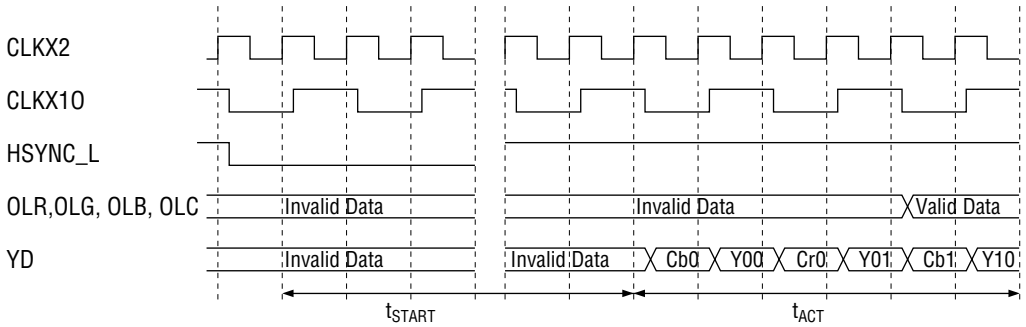
Operation mode	t_{STA}(Ts)
ITU 601 NTSC	250
ITU 601 PAL	280

In slave mode

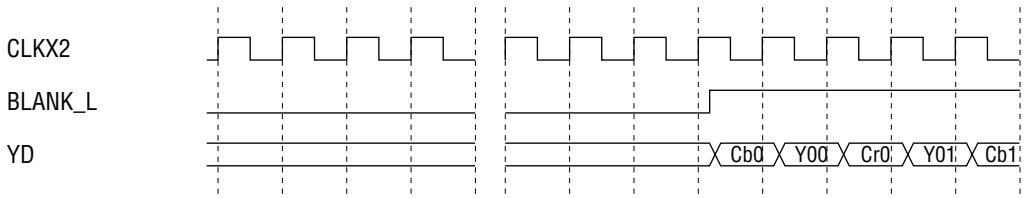
Operation mode	t_{STA}(Ts)
ITU 601 NTSC	260
ITU 601 PAL	290

$t_{STA} - t_{S1} = t_{START}$

Timing of Input Data to HSYNC_L

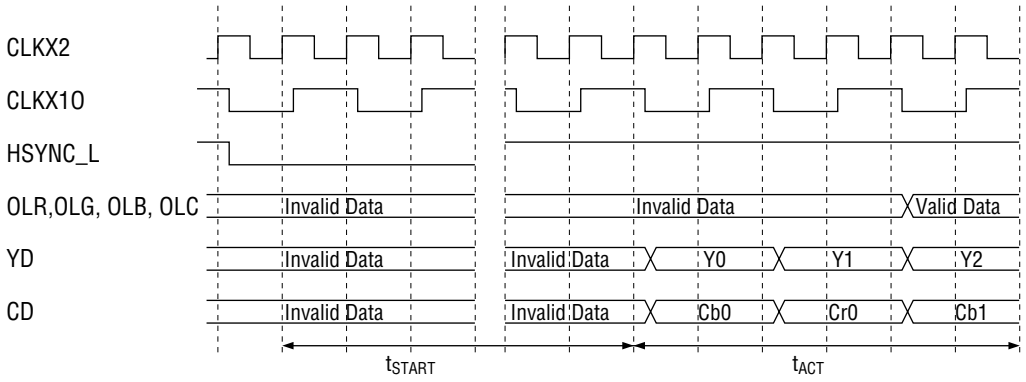


Input Timing when BLANK_L is Input

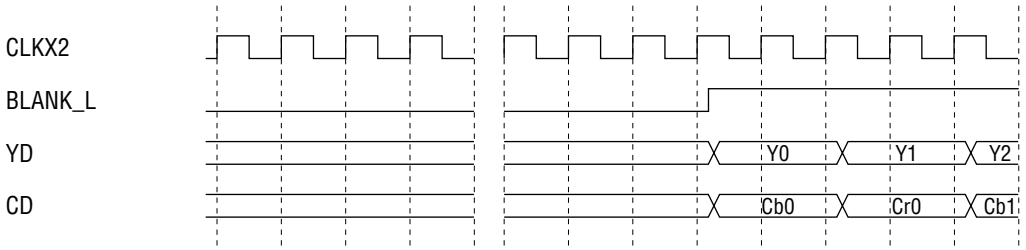


Input timing at 27 MHz in YCbCr format

Timing of Input Data to HSYNC_L



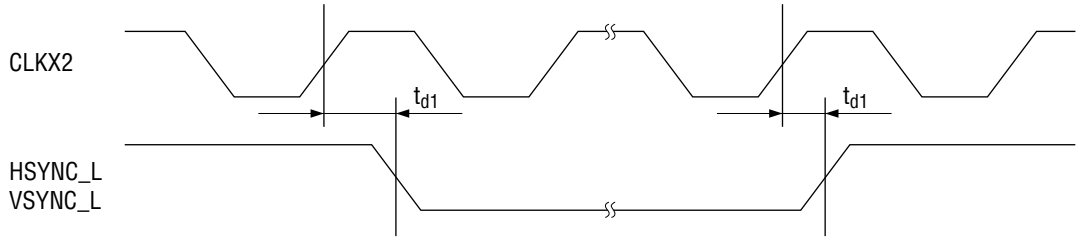
Input Timing when BLANK_L is Input



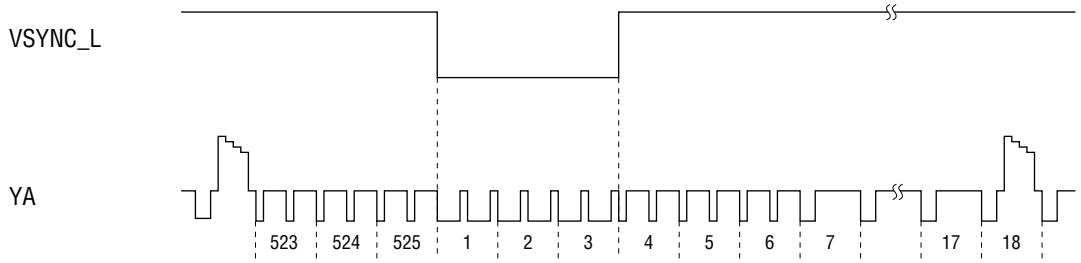
Input timing at 13.5 MHz in YCbCr format

Internal Synchronization Output Timing

Output timing of HSYNC_L and VSYNC_L in master mode is as follows.



Output timing of internal synchronization, HSYNC_L and VSYNC_L

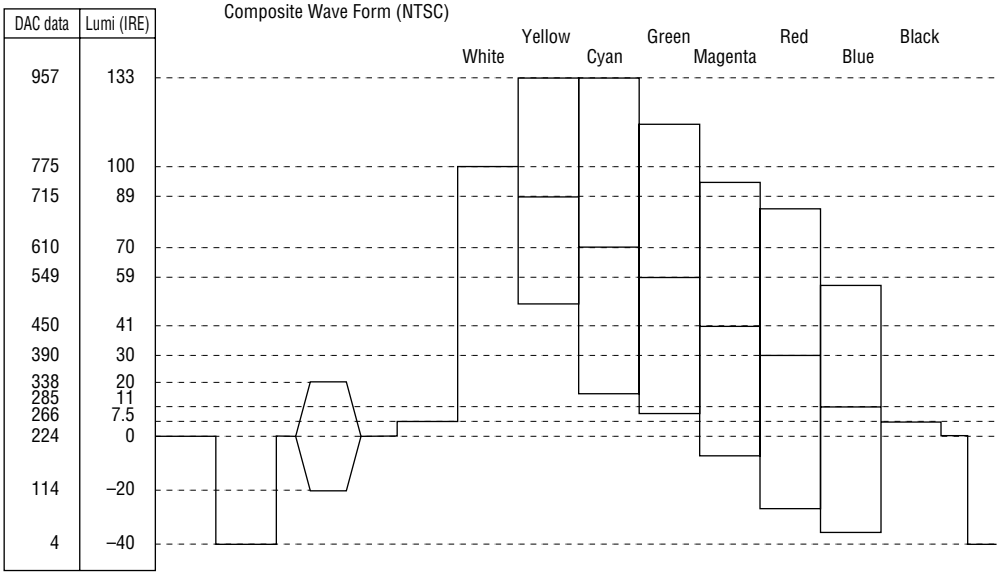


Output timing of internal synchronization VSYNC_L

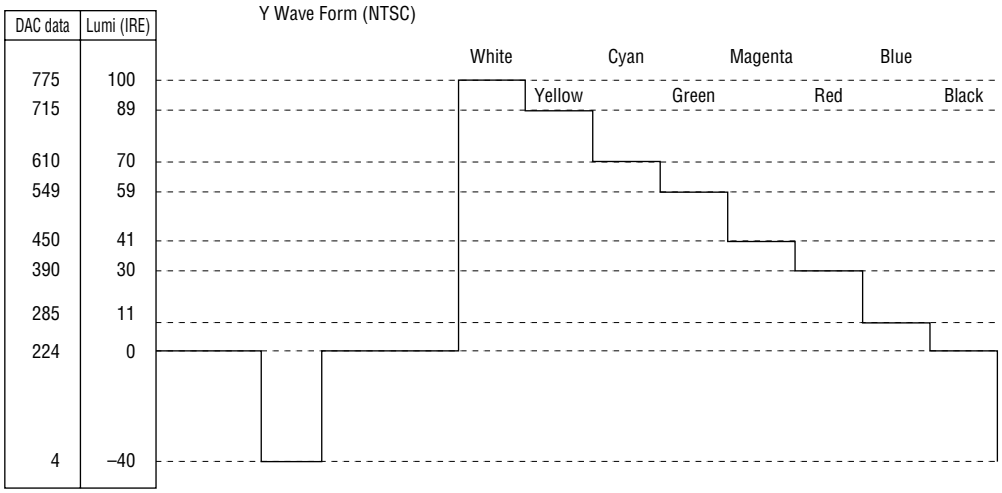
OUTPUT FORMAT

The timing conforms to the ITU624 standard.
In the NTSC operation mode, the existence/non-existence of setup level is selected by setting of internal regsiters.

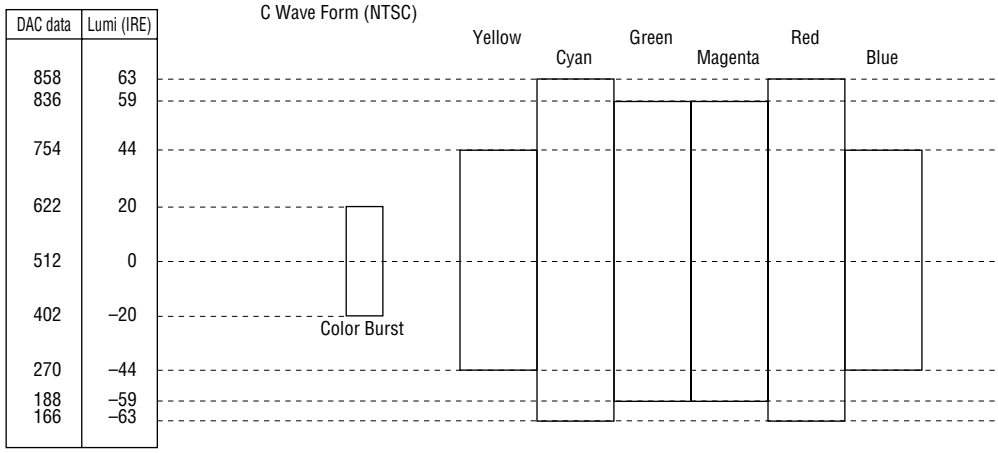
Data level on the DAC input terminal:
When the contents of 100% luminance order color bar are input into the encoder, the input level is as follows.



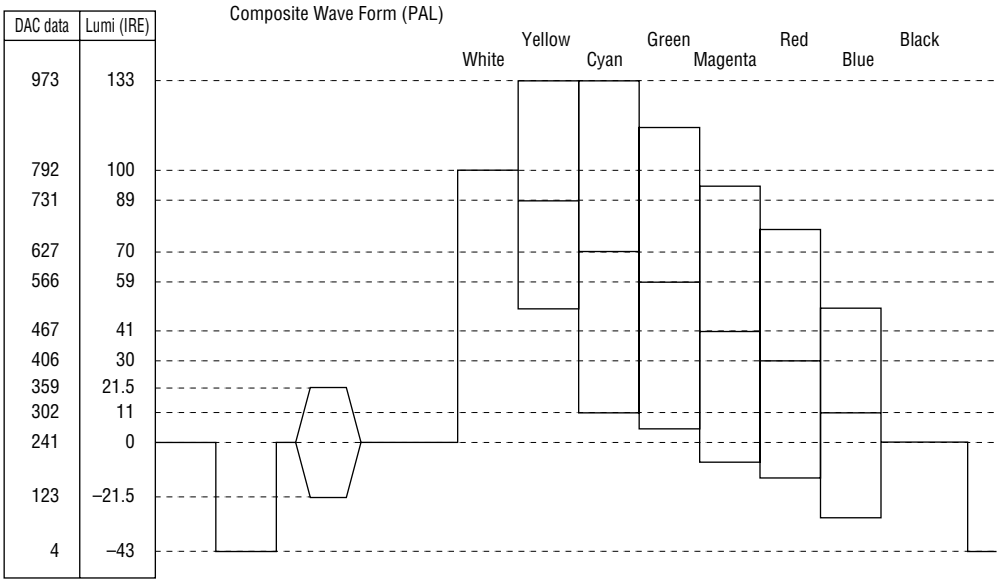
NTSC Composite Signal (Setup 7.5)



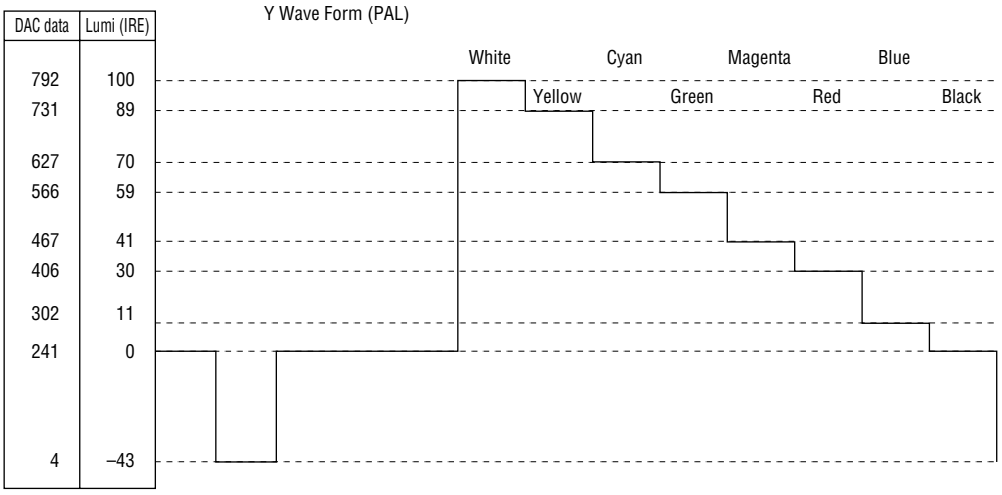
NTSC Y Signal Output (Setup 0)



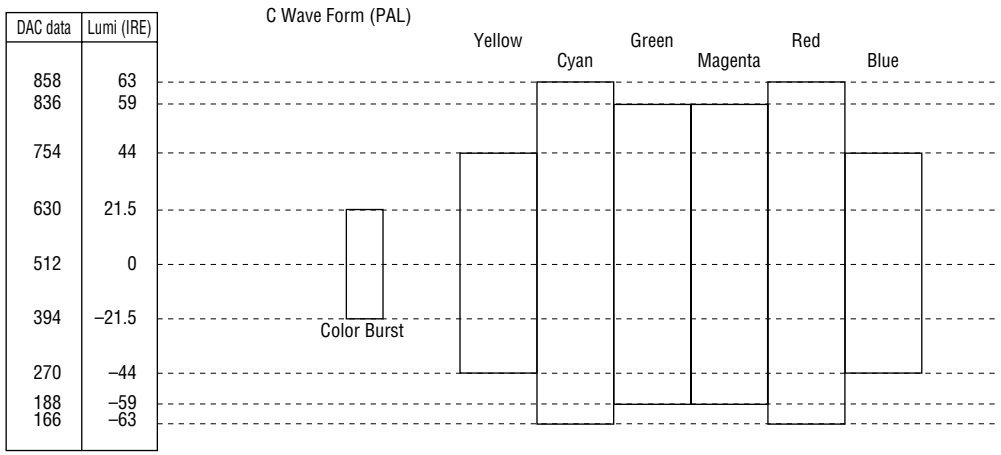
NTSC C Signal Output



PAL Composite Signal

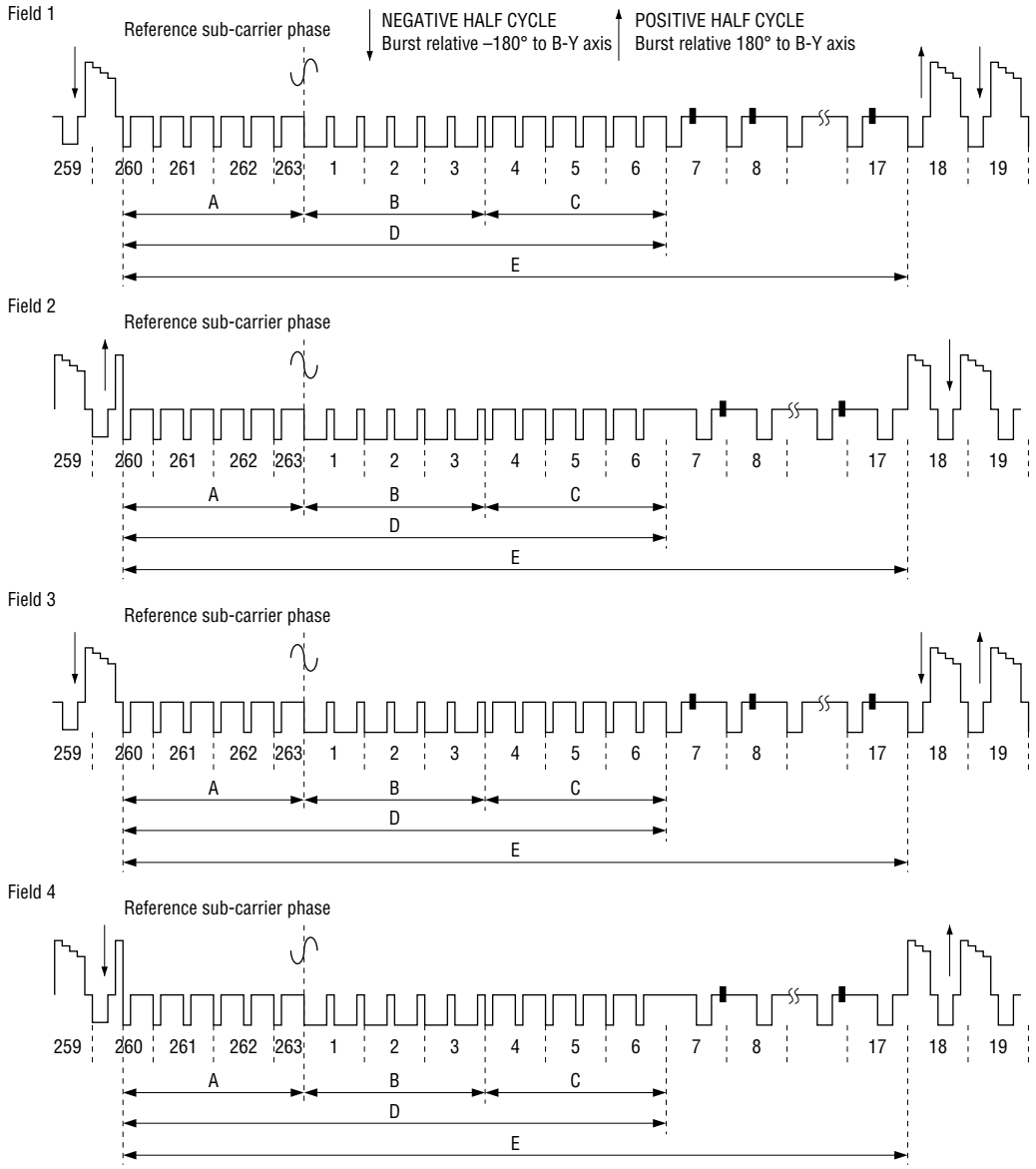


PAL Y Signal Output



PAL C Signal Output

NTSC (Interlaced)

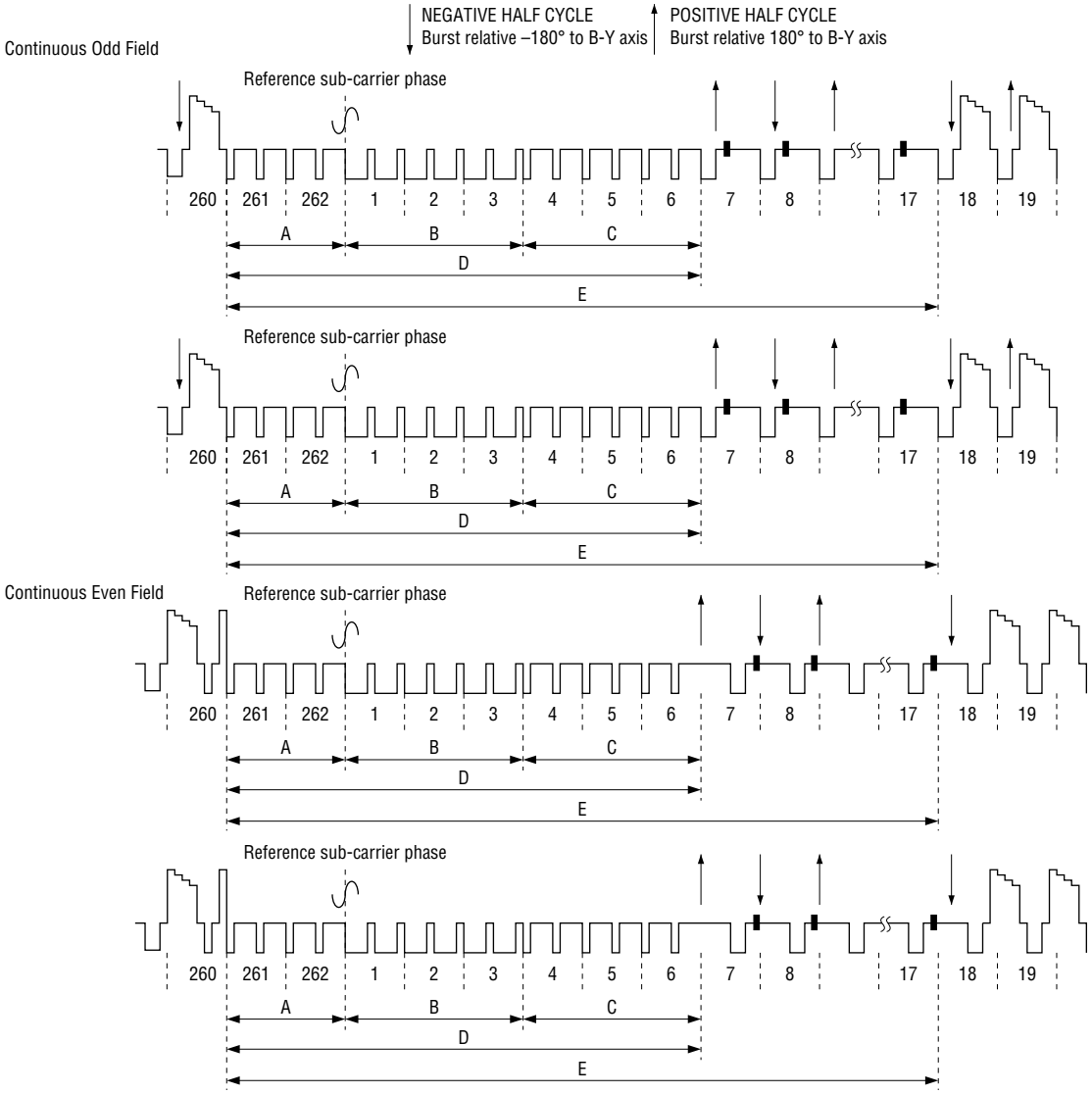


Output timing (Interlaced NTSC)

Symbol	Name	Period
		Odd field (Even field)
A	First equalizing pulse period (3H)	259.5 to 262.5H
B	Vertical synchronization period (3H)	1 to 3H
C	Second equalizing pulse period (3H)	4 to 6H
D	Burst pause period	1 to 6,259.5 to 262.5H
E	Vertical blanking period (20H)	1 to 17,259.5 to 262.5H

Output timing (Interlaced NTSC)

NTSC (Non-interlaced)

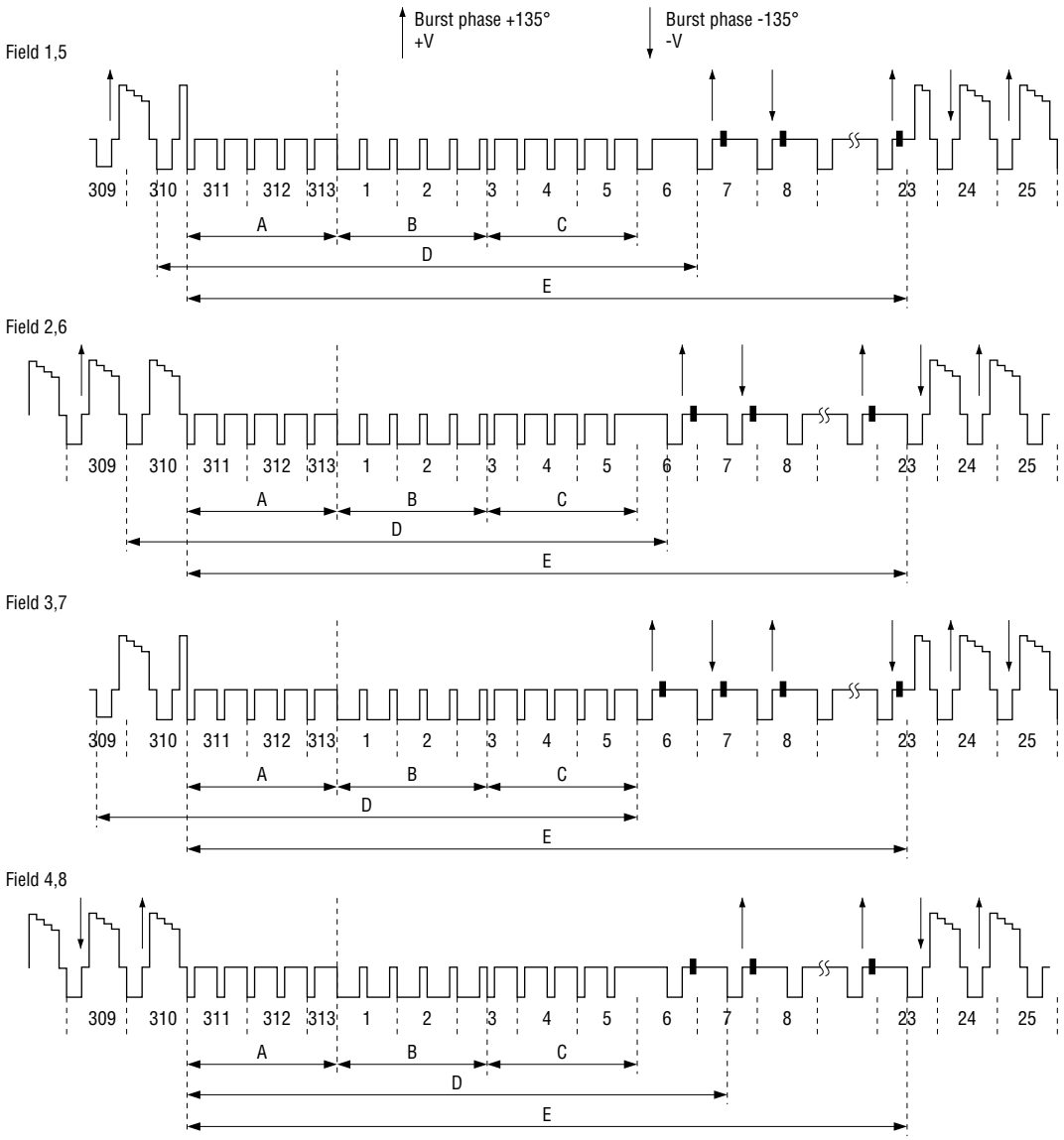


Output timing (Non-interlaced NTSC)

Symbol	Name	Period
		Continuous odd • even field
A	First equalizing pulse period (2H)	261 to 262H
B	Vertical synchronization period (3H)	1 to 3H
C	Second equalizing pulse period (2H)	4 to 6H
D	Burst pause period	261 to 6H
E	Vertical blanking period (19H)	261 to 17H

Output timing (Non-interlaced NTSC)

PAL (Interlaced)

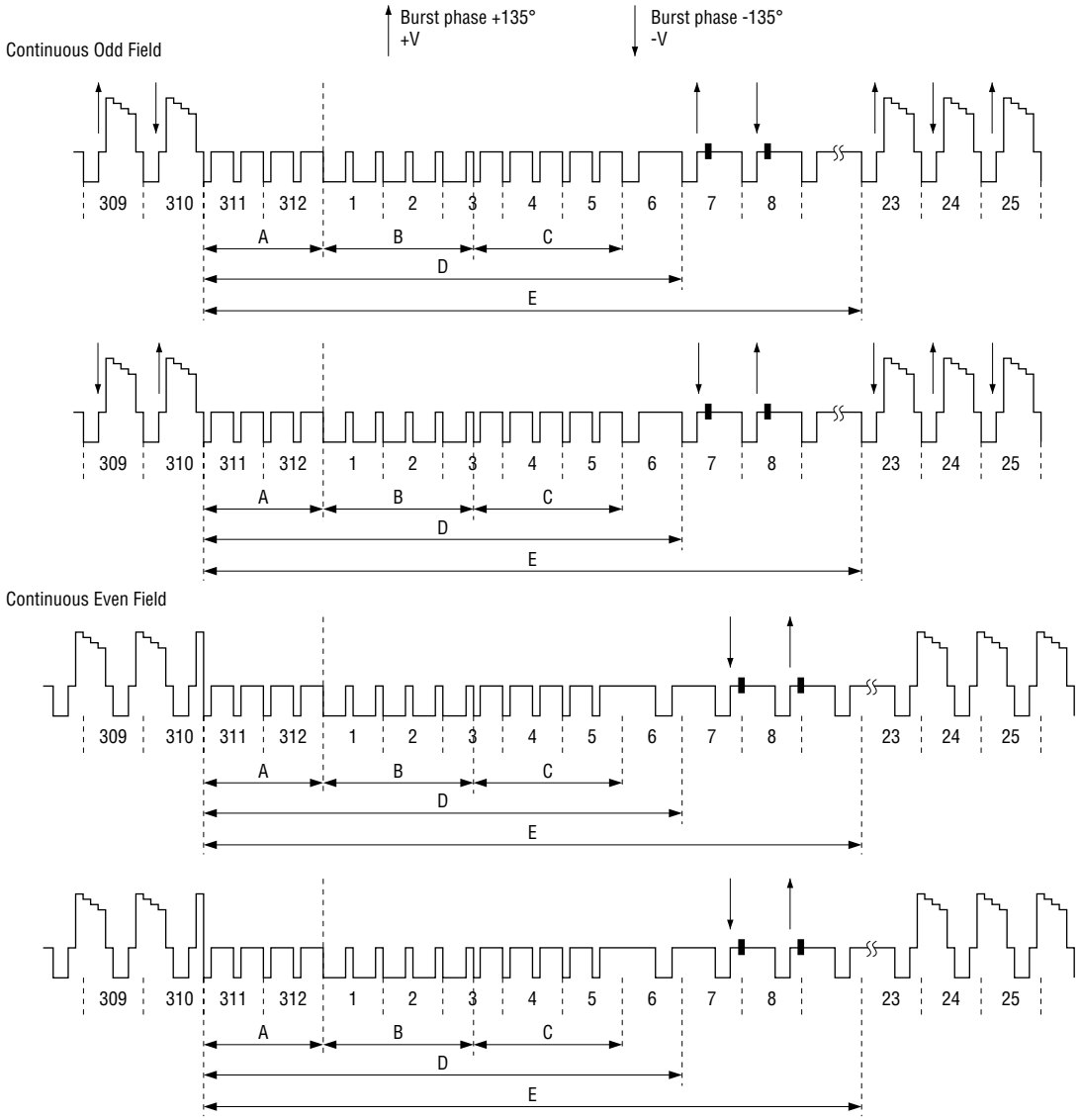


Output timing (Interlaced PAL)

Symbol	Name	Period			
		Field 1,5	Field 2,6	Field 3,7	Field 4,8
A	First equalizing pulse period (2.5H)	311 to 312.5H	311 to 312.5H	311 to 312.5H	311 to 312.5H
B	Vertical synchronization period (2.5H)	1 to 2.5H	1 to 2.5H	1 to 2.5H	1 to 2.5H
C	Second equalizing pulse period (2.5H)	2.5 to 5H	2.5 to 5H	2.5 to 5H	2.5 to 5H
D	Burst pause period	1 to 6,310 to 312.5H	1 to 5.5,308.5 to 312.5H	1 to 5,311 to 312.5H	1 to 6.5,309.5 to 312.5H
E	Vertical blanking period (25H)	1 to 22.5,311 to 312.5H	1 to 22.5,311 to 312.5H	1 to 22.5,311 to 312.5H	1 to 22.5,311 to 312.5H

Output timing (Interlaced PAL)

PAL (Non-interlaced)

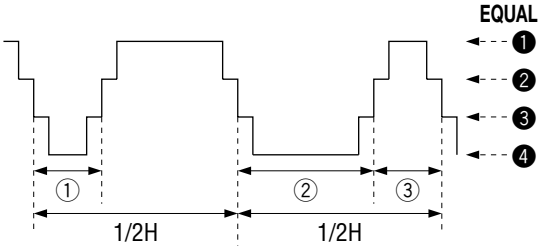


Output timing (Non-interlaced PAL)

Symbol	Name	Period
		Continuous odd • even field
A	First equalizing pulse period (2H)	311 to 312H
B	Vertical synchronization period (2.5H)	1 to 2.5H
C	Second equalizing pulse period (2.5H)	2.5 to 5H
D	Burst pause period	311 to 6H
E	Vertical blanking period (24H)	311 to 22H

Output timing (Non-interlaced PAL)

<Equalizing pulse, vertical synchronization period>



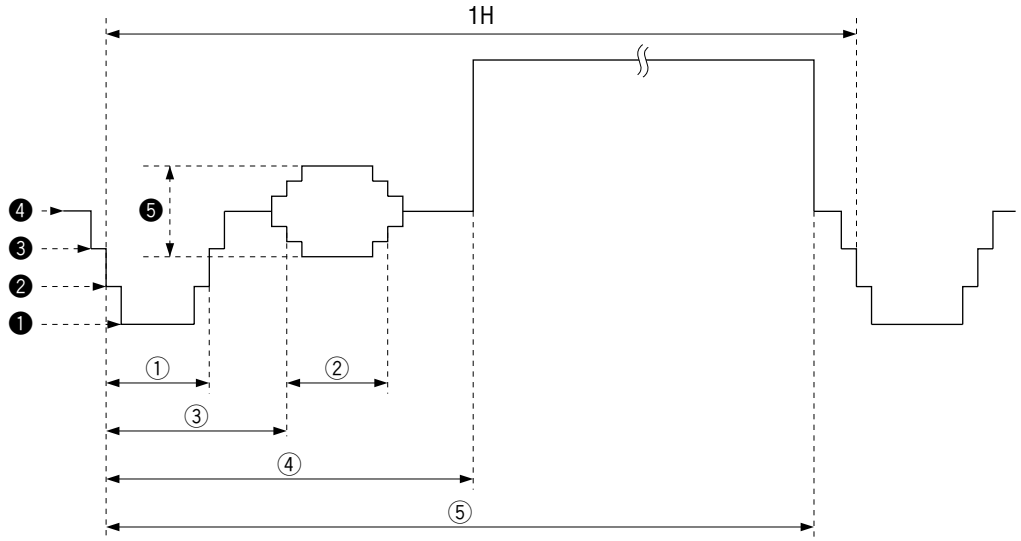
①Equalizing pulse width
②Vertical sync pulse width
③Serration

❶Blanking level
❷(synchronizing + blanking level) × (2/3)
❸(synchronizing + blanking level) × (1/3)
❹Synchronzing level

Setting content of equalizing pulse vertical synchronization period (Ts is sampling clock cycle in each mode)

	①	②	③	1/2H
ITU 601 NTSC	31Ts	365Ts	64Ts	429Ts
ITU 601 PAL	32Ts	369Ts	63Ts	432Ts

<Horizontal blanking period>



①Horizontal sync pulse width
②Burst signal output period
③Burst signal start
④Horizontal blanking period (excluding front porch)
⑤Front porch start

❶Synchronzing level
❷(synchronizing + blanking level) × (1/3)
❸(synchronizing + blanking level) × (2/3)
❹Blanking level
❺Peak to peak value of burst

Horizontal blanking period

Setting content of horizontal blanking period (Ts is sampling clock cycle in each mode)

	①	②	③	④	⑤	Total dots/1H
ITU601 NTSC	63Ts	31Ts	71Ts	127Ts	838Ts	858
ITU601 PAL	63Ts	31Ts	75Ts	142Ts	844Ts	864

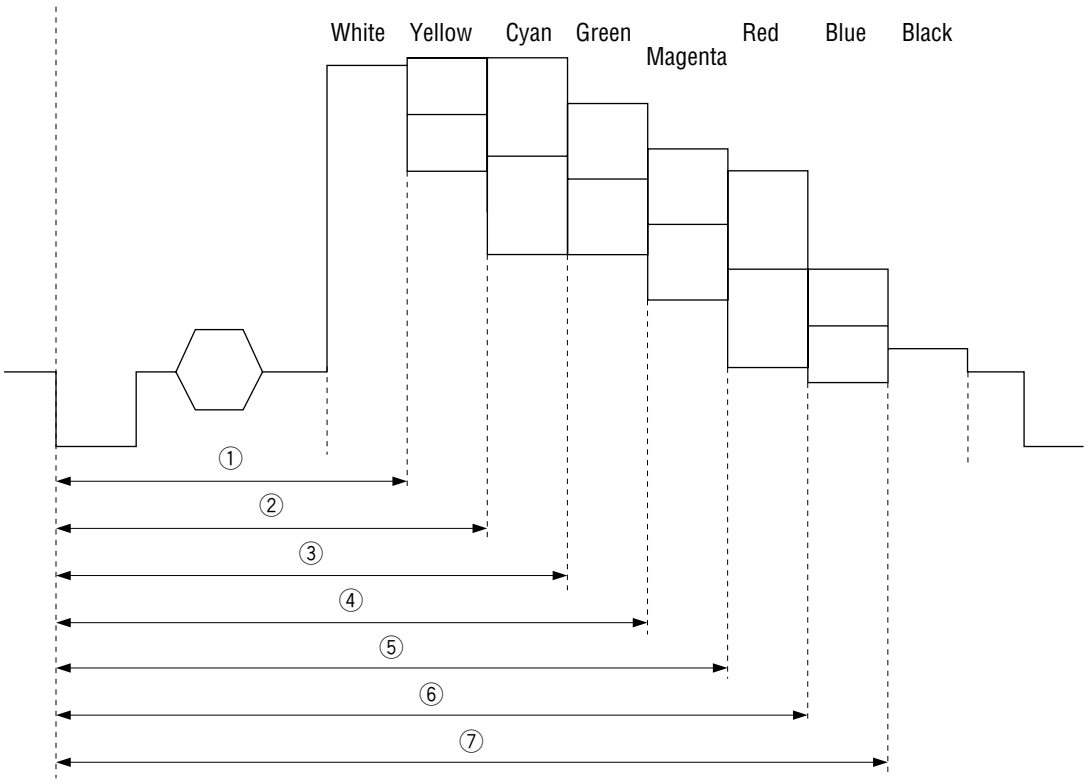
Setting content of horizontal blanking period

Setup Level Setting

When the NTSC operation mode is selected, one of the two kinds of setup level can be selected by setting of registers.
When the setup level 0 is selected, the Black-to-White is 100IRE.
When the setup level 7.5IRE is selected, the Black-to-White is 92.5IRE.
However, this setup function is valid only for the NTSC mode and invalid for the PAL mode.

Color Bar Generation Function

25%, 50%, 75% or 100% luminance order color bar is output by setting internal registers. The output timings for each color bar color is as follows.



Output timing of each color bar color

Operation mode	hblank	①	②	③	④	⑤	⑥	⑦	1H
ITU601 NTSC	127Ts	216Ts	305Ts	394Ts	483Ts	572Ts	661Ts	750Ts	858Ts
ITU601 PAL	142Ts	230Ts	318Ts	406Ts	494Ts	582Ts	670Ts	757Ts	864Ts

(Ts : sampling block period)

Contents of color bar output timing setting

I²C BUS FORMAT

Basic input format of I²C-bus interface is shown below.

S	Slave Address	A	Subaddress	A	Data 0	A	.....	Data n	A	P

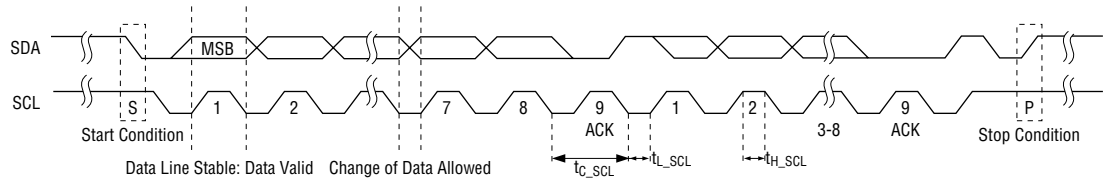
Symbol	Description
S	Start condition
Slave Address	Slave address 1000100X (ADRS pin : 0) or 1000110X (ADRS pin : 1), the 8th bit is R (1)/W (0) signal.
A	Acknowledge. Generated by slave
Subaddress	Subaddress byte
Data n	Data byte and acknowledge continues until data byte stop condition is met.
P	Stop condition

As described above, it is possible to read and write data from subaddress to subaddress continuously. Reading from and writing to discontinuous addresses is performed by repeating the Acknowledge and Stop condition formats after Data 0.

If one of the following matters occurs, the encoder will not return "A" (Acknowledge).

- The slave address does not match.
- A non-existent subaddress is specified.
- The read/write attribute of a register does not match "X" (read : 1/write : 0 control bit).

The input timing is shown below.



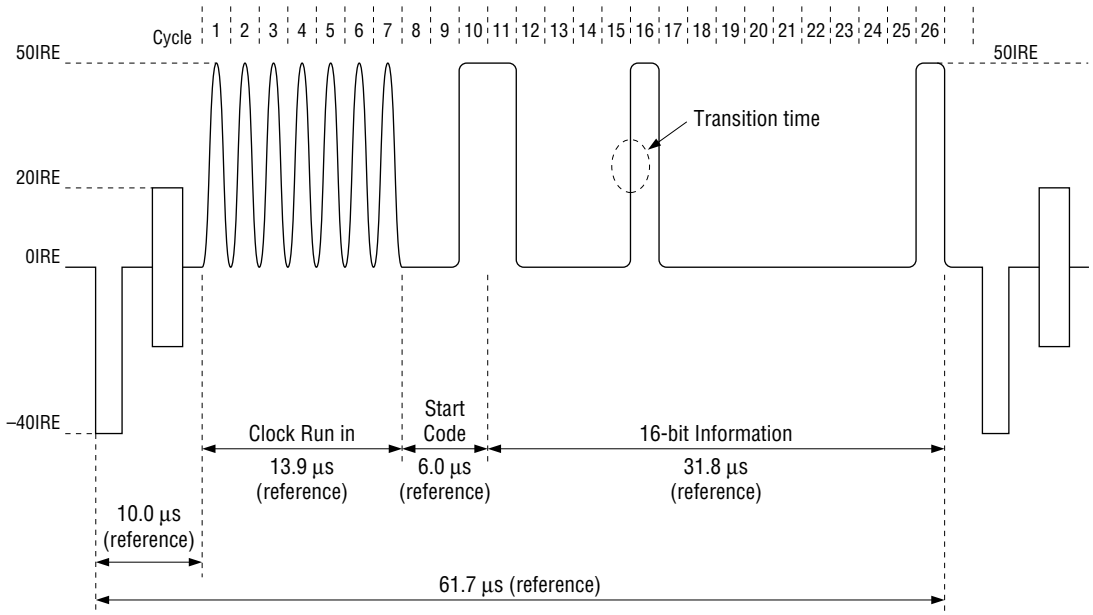
I²C-bus Basic Input/Output Timing

CLOSED CAPTION FUNCTION

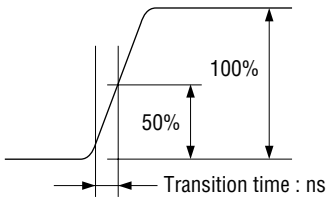
The closed caption function based on the NCI standard is available.
The caption information on each line is multiplexed as a 26-cycle signal which is synchronized at 503 kHz. Each cycle is described below.

Cycles 1 to 7	Clock-Run-in period	7-cycle clock signal to synchronize caption data with caption information.
Cycles 8 to 10	Start Code	Fixed signal with logical level "001"
Cycles 11 to 26	Caption Information	2-byte multiplex information with combination of the ASCII code bits 0 - 6 and the 7ODD parity bit. The first byte is multiplexed in cycles 11 to 18 and the second byte is multiplexed in cycles 19 to 26, starting from LSB.

The output timing when data is multiplexed by the closed caption function is shown below.



Caption signal



Transition time

INTERNAL REGISTERS

The register (ID number) for the Anticopy function and the register (CCSTAT) for the closed caption are read-only registers.
The other registers are write-only registers.
Details of the internal registers are described below. (Values marked * are set by default.)

Register name	R/W	Sub-address	Default value		Item to be set	Description
MR	Write	00	00	MR[4]	Override	Switching between the external terminal and
(Mode register)	Only					internal register settings (for the operation mode)
						*0 : External pin setting enabled
						1 : Internal register setting enabled
				MR[3]	Chroma format	Chrominance signal input format
						*0 : Offset binary
						1 : 2's complement
				MR[2]	Black level control	Black level setup
						Note : Valid in NTSC mode only
						*0 : Black level 0IRE
						1 : Black level 7.5IRE
				MR[1]	Master/Slave	Master or slave operation select
						*0 : Slave
						1 : Master
				MR[0]	Video mode select	Operation mode switching
						*0 : ITU601 NTSC
						1 : ITU601 PAL (Note 1)
CR	Write	01	03	CR[4]	Undefined	—
(Command Register)	Only			CR[3]	Interlace	Scanning method
						*0 : Interlace
						1 : Non-interlace
				CR[2]	Color bar	Adjusting luminance order color bar output control
						*0 : Input image data or overlay data
						1 : Luminance order color bar
				CR[1:0]	Overlay level	Overlay signal/adjusting luminance order color
						bar output level control
						*00 : 100%
						01 : 75%
						10 : 50%
						11 : 25%

(Note 1) When the MR[4] register is set to "1" to enable the settings of the internal registers, the settings of pin 7 (MODE) and the MR[0] register should be the same.

Register name	R/W	Sub-address	Default value		Item to be set	Description
CCEN	Write Only	02	00	CCEN[1:0]	Closed Caption Enable	Closed caption function on/off control *0 : C.C. encoding off 1 : Odd field encoding on 2 : Even field encoding on 3 : Both field encoding on
CCLN	Write Only	03	11	CCLN[4:0]	Closed Caption Line Number	Closed caption data insertion line number setting NTSC : CCLN + 4 PAL : CCLN + 1
CCODT0	Write Only	04	00	CCODT0[7:0]	1st byte of C.C. data, ODD field	First byte closed caption data in odd-number field
CCODT1	Write Only	05	00	CCODT1[7:0]	2nd byte of C.C. data, ODD field	Second byte closed caption data in odd-number field
CCEDT0	Write Only	06	00	CCEDT0[7:0]	1st byte of C.C. data, EVEN field	First byte closed caption data in even-number field
CCEDT1	Write Only	07	00	CCEDT1[7:0]	2nd byte of C.C. data, EVEN field	Second byte closed caption data in even-number field
CCSTAT	Read Only	08	00	CCSTAT[0]	Odd field C.C. status	odd-number field status *0 : CCODT0, CCODT1 writing completed 1 : ODD Field C.C. bytes ENCODE completed
				CCSTAT[1]	Odd field C.C. status	Even-number field status *0 : CCEDT0, CCEDT1 writing completed 1 : EVEN Field C.C. bytes ENCODE completed

OPERATION MODE SETTING BY PIN CONTROL

The contents of control using TEST1, SEL1, SEL2, CLKSEL, and MS are shown below.

TEST1	0 : Normal operation	1 : Test mode
SEL1	0 : Normal operation	1 : Sleep mode
SEL2	0 : ITU Rec. 656	1 : Y Cb Cr
CLKSEL	0 : 27 MHz	1 : 13.5 MHz
MS	0 : Slave	1 : Master

TEST1	SEL1	SEL2	CLKSEL	MS	Operation mode
0	0	0	0	0	ITUR656 Slave
0	0	0	1	0	13.5 MHz YCbCr Slave
0	0	0	1	1	13.5 MHz YCbCr Master
0	0	1	0	0	27 MHz YCbCr Slave
0	0	1	0	1	27 MHz YcbCr Master
0	1	x	x	x	Sleep Mode

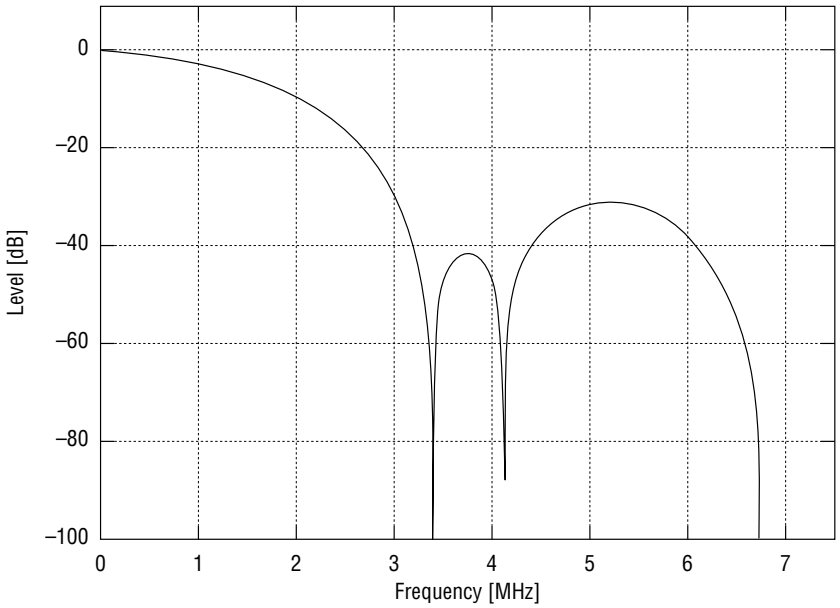
x : don't care

FILTER CHARACTERISTICS

The characteristics of LPF used for color signal processing and interpolation filters used for upsampling processing are shown below.

LPF for 422 color signals

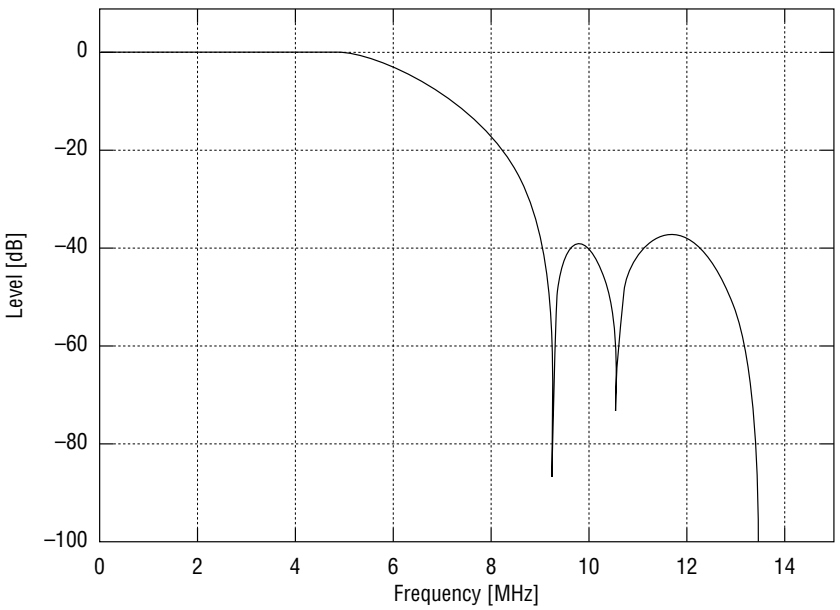
The following shows the characteristics when the clock frequency is 13.5 MHz.



422 Interpolation + LPF Frequency Characteristic

Interpolation

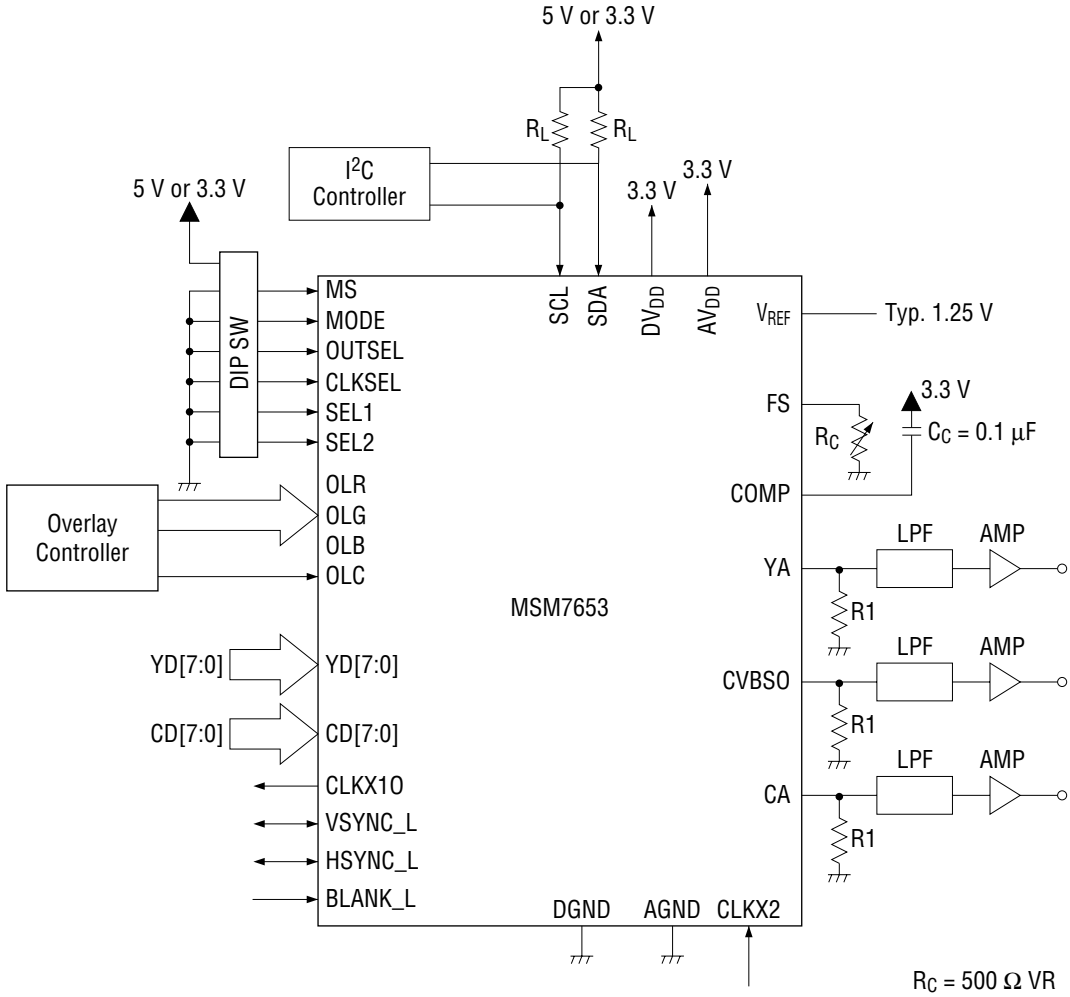
The following shows the characteristics when the clock frequency is 27 MHz.



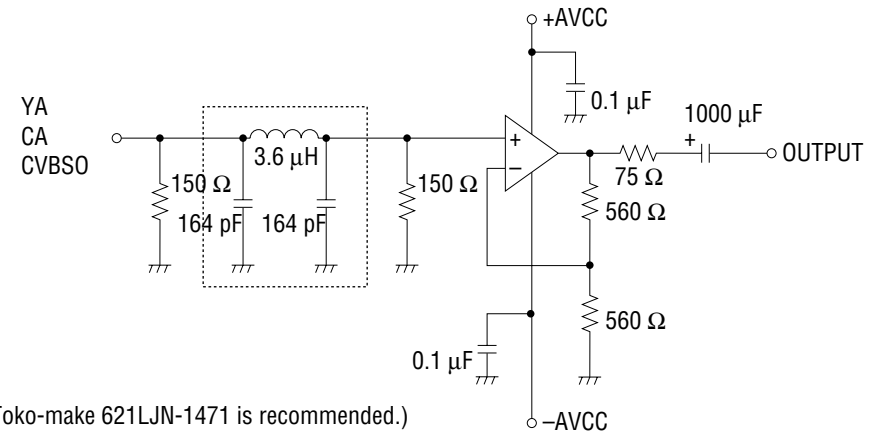
Up Sampling Filter Frequency Characteristic

(Note) The characteristics of these filters are based on design data.

APPLICATION CIRCUIT EXAMPLE



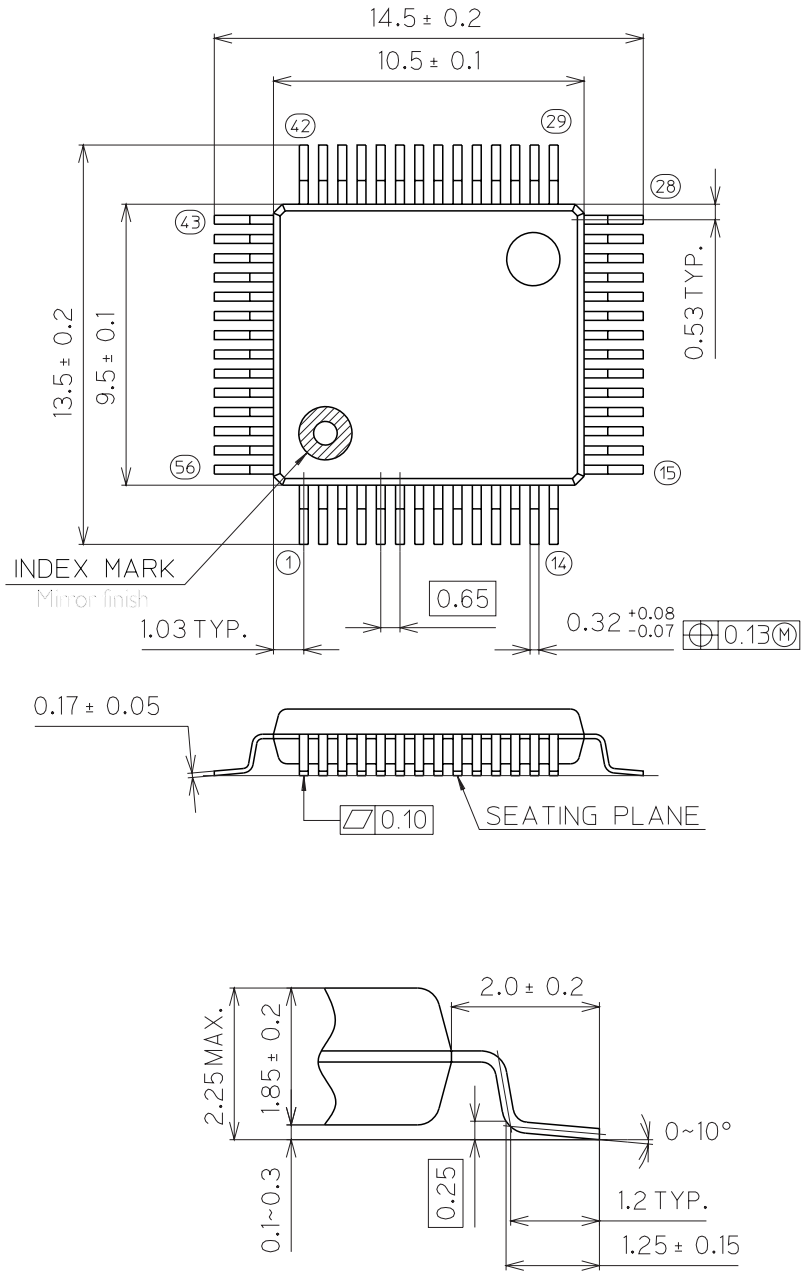
Recommended Analog Output Circuit



Note: The termination of a DA converter analog output with a 37.5 Ω load eliminates need for an AMP.

PACKAGE DIMENSIONS

(Unit : mm)



56-Pin Plastic QFP

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