DRAM

1 MEG x 4 DRAM

STATIC-COLUMN

FEATURES

- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 275mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), and HIDDEN
- STATIC-COLUMN access cycle

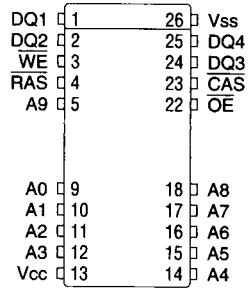
OPTIONS

OPTIONS	MARKING
• Timing	
70ns access	-7
80ns access	-8
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic ZIP (350 mil)	Z

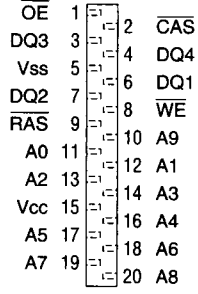
- Part Number Example: MT4C4003JDJ-7

PIN ASSIGNMENT (Top View)

20-Pin SOJ
(DC-1)



20-Pin ZIP
(DB-2)



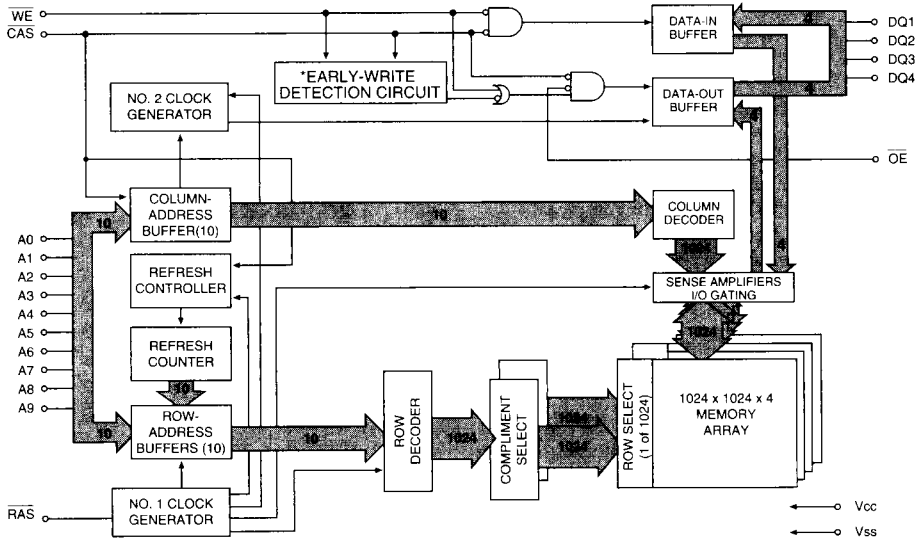
GENERAL DESCRIPTION

The MT4C4003J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin(s), data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

STATIC-COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. After the first read, any column-address transition will result in new data-out. Unlike PAGE-MODE, which requires $\overline{CAS}$ to be toggled for each successive PAGE-MODE access, STATIC-COLUMN allows $\overline{CAS}$ to be left LOW for successive STATIC-COLUMN accesses. Returning $\overline{RAS}$ HIGH terminates the STATIC-COLUMN operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
STATIC-COLUMN



***NOTE:** 1. $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
2. $\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data-In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
STATIC-COLUMN	1st Cycle	L	L	H	L	ROW	COL	Data-Out
READ	2nd Cycle	L	L	H	L	n/a	COL	Data-Out
STATIC-COLUMN	1st Cycle	L	L	L	X	ROW	COL	Data-In
EARLY-WRITE	2nd Cycle	L	L	L	X	n/a	COL	Data-In
STATIC-COLUMN	1st Cycle	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
READ-WRITE	2nd Cycle	L	L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data-Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	100	90	mA	3, 4, 28
OPERATING CURRENT: STATIC-COLUMN Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC4}	70	60	mA	3, 4, 28
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	100	90	mA	3, 28
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	100	90	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5.V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	130		150		ns	
READ-WRITE cycle time	^tRWC	185		205		ns	
STATIC-COLUMN READ or WRITE cycle time	^tSC	40		45		ns	
STATIC-COLUMN READ-WRITE cycle time	^tSRWC	100		110		ns	
Access time from $\overline{RAS}$	^tRAC		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20	ns	15
Output Enable	^tOE		20		20	ns	23
Access time from column-address	^tAA		35		40	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (STATIC-COLUMN)	^tRASC	70	200,000	80	200,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		ns	16
$\overline{CAS}$ precharge time (STATIC-COLUMN)	^tCP	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
Row-address setup time	^tASR	0		0		ns	
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		ns	
Column-address hold time	^tCAH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	75		85		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	35		40		ns	
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		ns	
Output buffer turn-off delay	^tOFF	3	20	3	20	ns	20, 29
Column-address hold time (referenced to $\overline{RAS}$)	^tAWR	55		60		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	21, 27
Write command hold time	^tWCH	15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	55		60		ns	
Write command pulse width	^tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

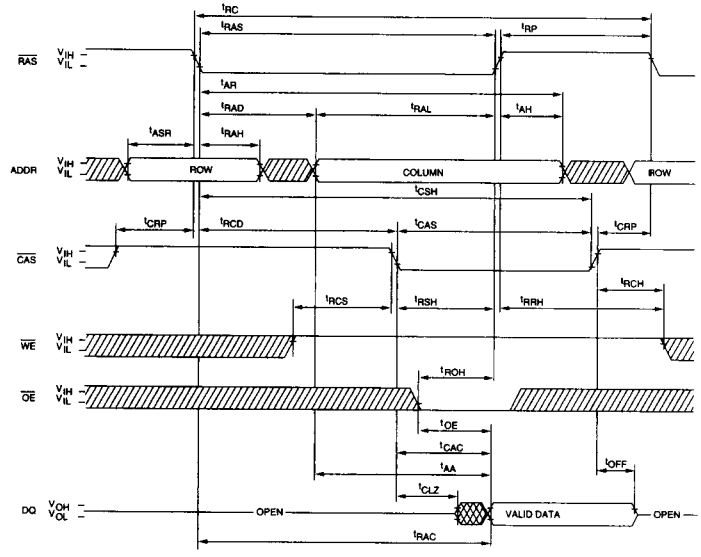
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command to $\overline{CAS}$ lead time	^tCWL	20		20		ns	
Data-in setup time	^tDS	0		0		ns	22
Data-in hold time	^tDH	15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	100		110		ns	21
Column-address to $\overline{WE}$ delay time	^tAWD	65		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	50		50		ns	21
Transition time (rise or fall)	^tT	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^tREF		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	25
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	25
$\overline{WE}$ hold time (WCBR test cycle)	^tWTH	10		10		ns	25
$\overline{WE}$ setup time (WCBR test cycle)	^tWTS	10		10		ns	25
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		ns	
Output disable	^tOD		20		20	ns	27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	20		20		ns	26
Write inactive time	^tWI	10		10		ns	
Previous WRITE to column-address delay time	^tLWAD	20	30	20	35	ns	
Previous WRITE to column-address hold time	^tAHLW	65		75		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	^tROH	10		10		ns	
Output data hold time from column-address	^tAOH	5		5		ns	
Output data enable from WRITE	^tOW	^tAA + 5		^tAA + 5		ns	
Access time from last WRITE	^tALW	65		75		ns	
Column-address hold time referenced to $\overline{RAS}$ HIGH	^tAH	5		10		ns	
$\overline{CAS}$ pulse width in STATIC-COLUMN mode	^tCSC	^tCAS		^tCAS		ns	

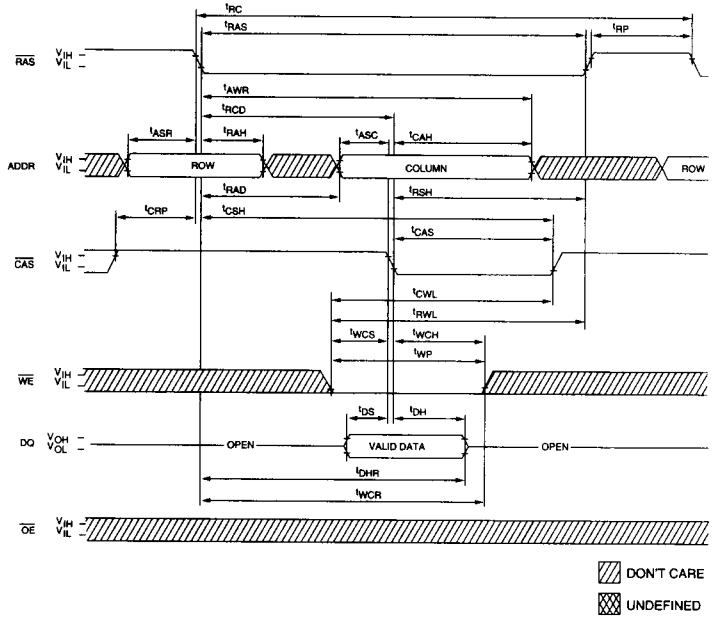
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY-WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
28. Column-address changed one while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$= V_{IH}
29. The 3ns minimum is a parameter guaranteed by design.

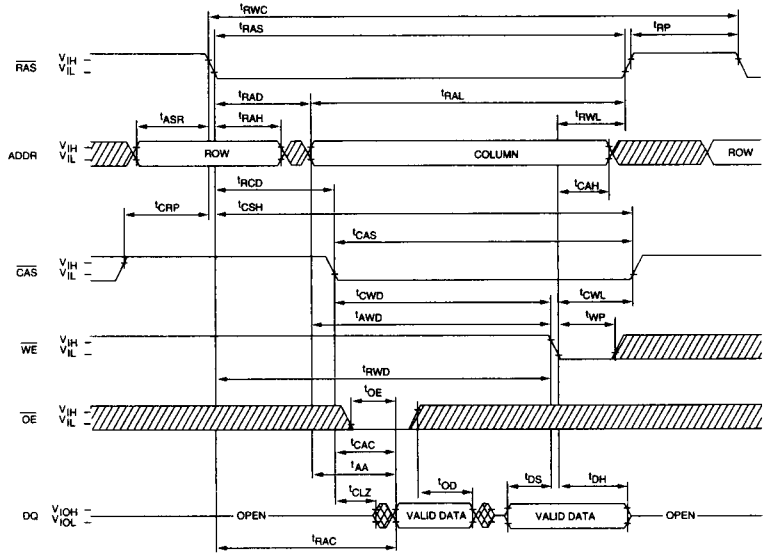
READ CYCLE



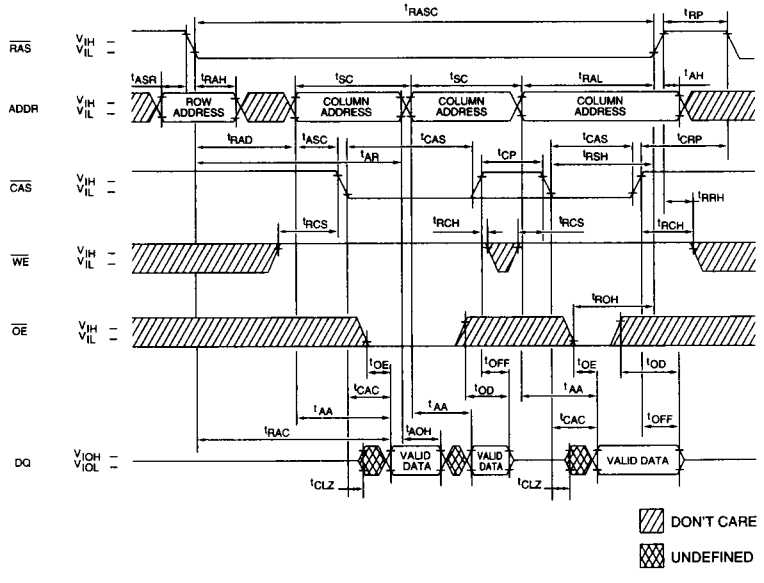
EARLY-WRITE CYCLE



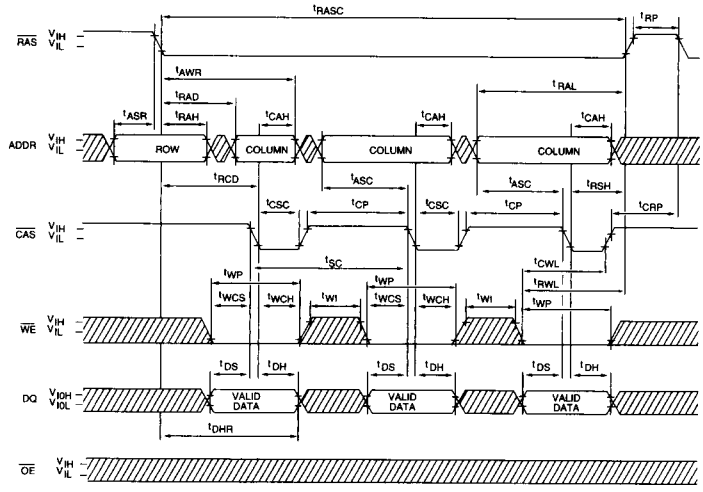
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



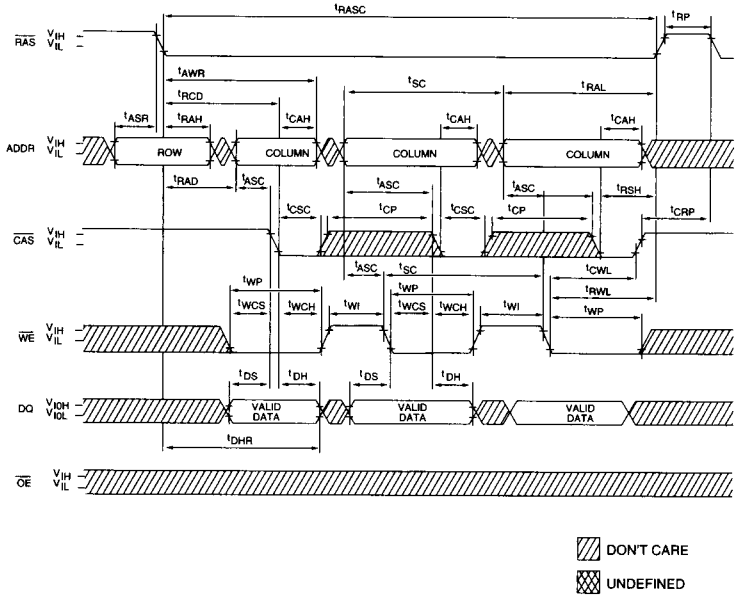
STATIC-COLUMN READ CYCLE



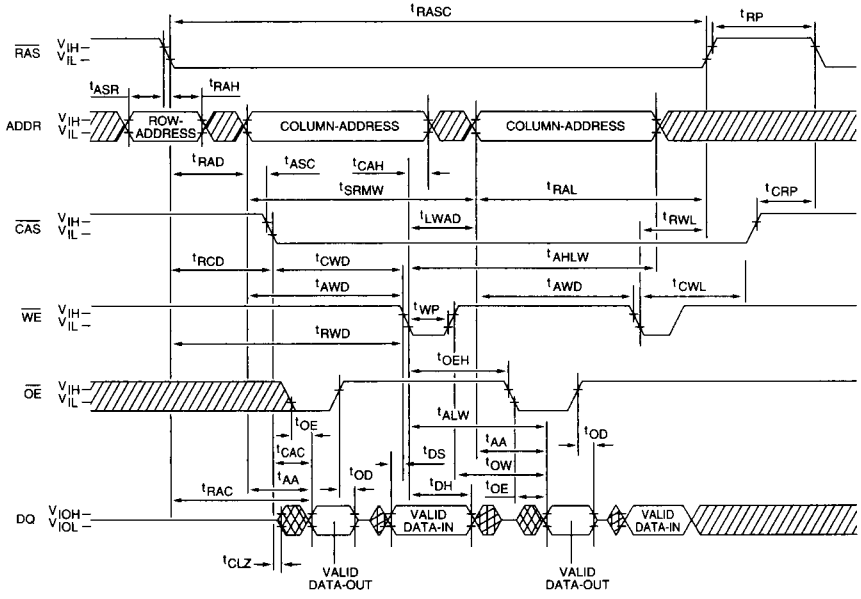
STATIC-COLUMN EARLY-WRITE CYCLE
(CAS-Controlled)



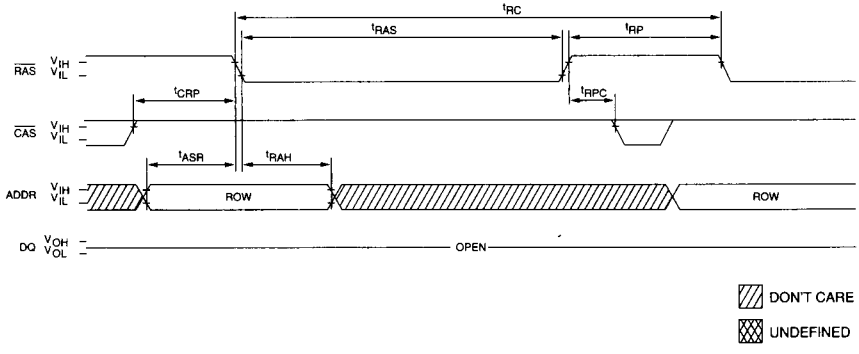
STATIC-COLUMN EARLY-WRITE CYCLE
(WE-Controlled)



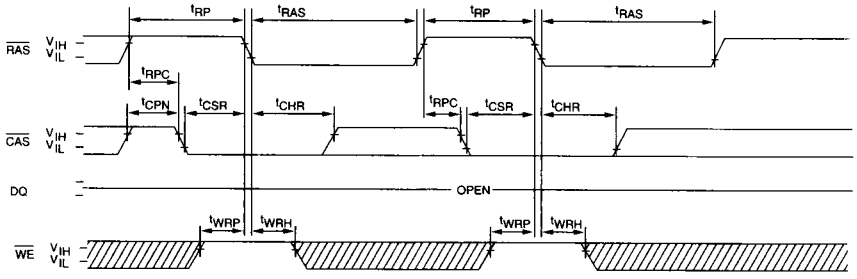
STATIC-COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



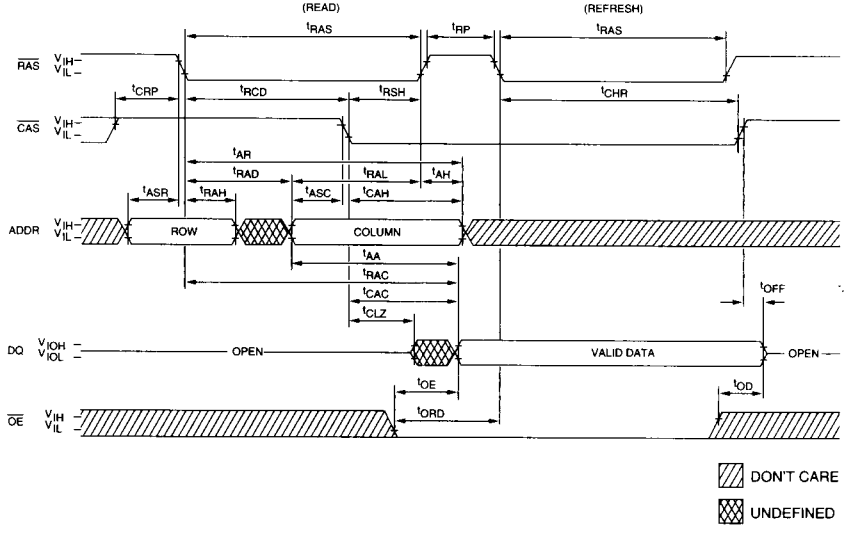
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9; WE = DON'T CARE)



CBR REFRESH CYCLE
(A0-A9 and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



DRAM

4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh cycle of the 1 Meg is the CBR REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{WE}$ pin held at a voltage HIGH level.

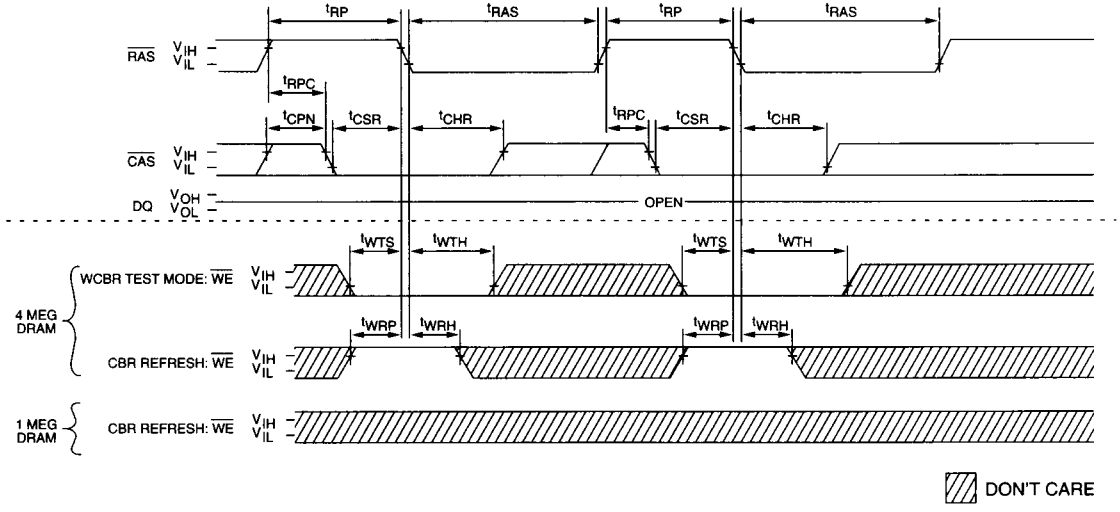
A CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC-specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{RAS}$-ONLY REFRESH or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC-specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY REFRESH cycle or a CBR REFRESH cycle ($\overline{WE}$ held HIGH).

SUMMARY

1. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH.
2. The eight $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or CBR REFRESH cycles ($\overline{WE}$ held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR