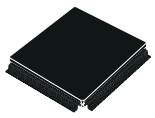
MTC20455

QUAD ADSL DMT TRANSCEIVER

- Quad DMT modem ATM framer
- Supports ANSI T1.413 issue 2, ITU G.992.1, and G.992.2 standards
- Low power consumption (1W for four lines)
- Standard Utopia level 2 ATM interface
- 160 PQFP Package
- 160 LFBGA Package



PQFP160

LFBGA160

ORDERING NUMBERS:

Part Numbers	Package	Temperature
MTC20455PQ-I	160 pin PQFP	-40 to +85°C
MTC20455MB-I	160 pin LFBGA	-40 to +85°C
Can also be ordered using kit number MTK20450		

DESCRIPTION

The MTC20455 is the DMT modem and ATM Framer of the MTK20450 Quad Rate adaptive ADSL DynaMiTe chipset. When used in conjunction with the MTC20454 or MTC20154 analog front-end, the product supports ANSI T1.413 release 2, ITU G.992.1 and G.992.2 (G.Lite) ADSL specifications through software configuration. It provides a cell based UTOPIA Level 2 ATM data interface.

The MTC20455 performs the DMT modulation, demodulation, Reed-Solomon encoding, bit interleaving and trellis coding for four ADSL modems. The ATM section provides framing functions for the generic and ATM Transmission Convergence (TC) layers. The generic TC consists of data scrambling and Reed-Solomon error corrections, with and without interleaving.

The MTC20455 is controlled and configured by the MTC20136 Transceiver Controller. All programmable coefficients and parameters are loaded by the Controller. The MTC20136 also controls the initialisation procedure and performs the monitoring and adaptive functions during operation.

Figure 1. Block Diagram

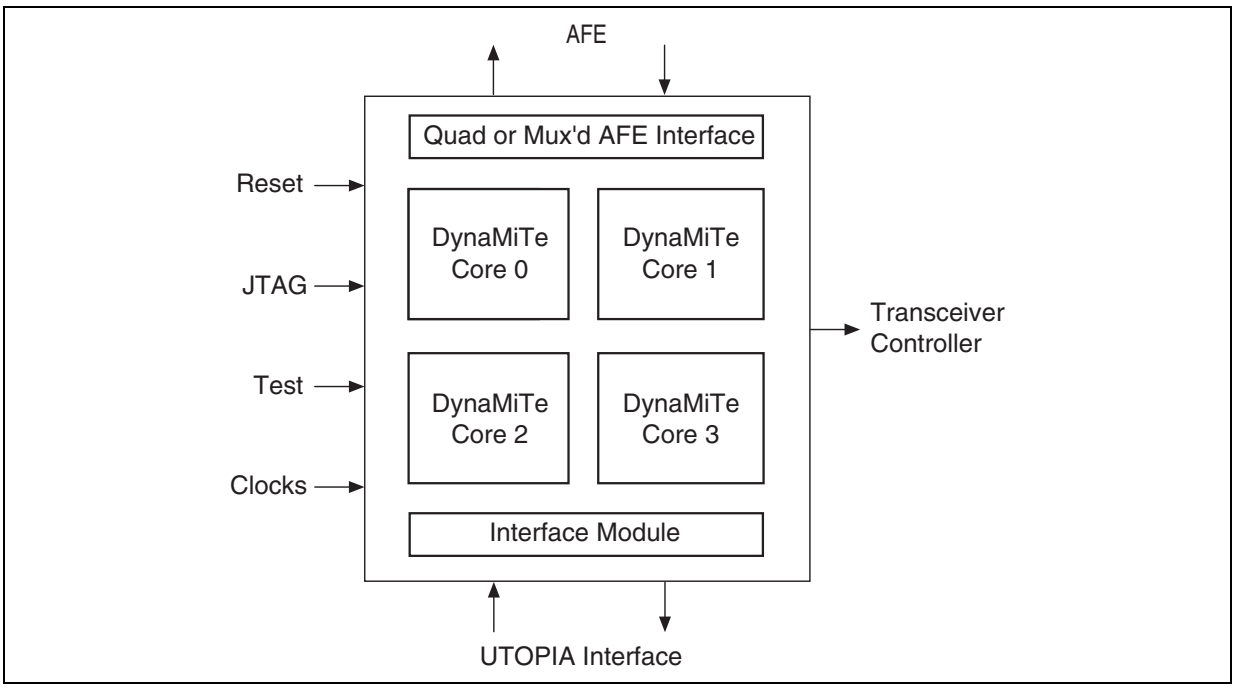


Figure 2. PQF160 package pin out

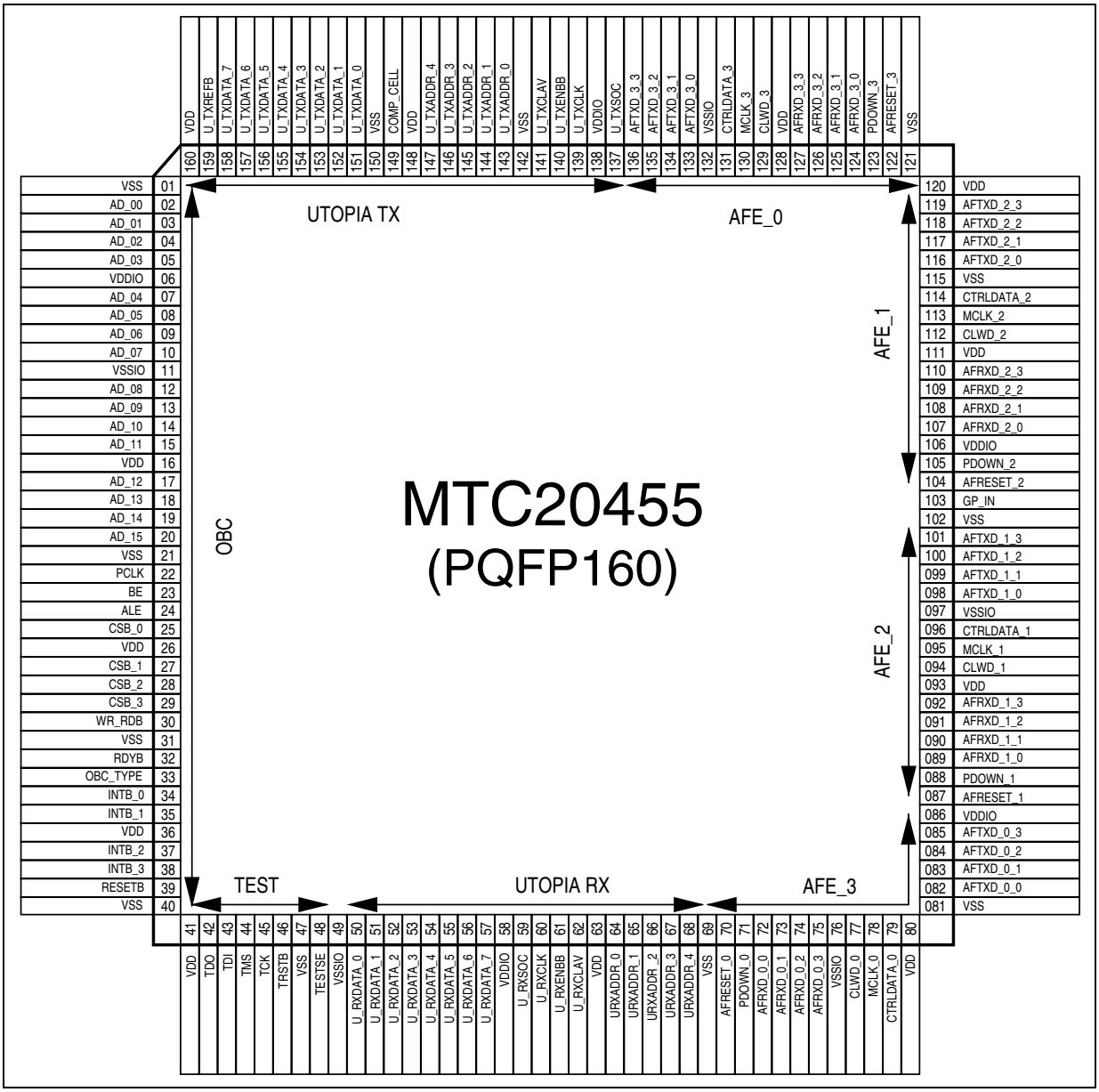


Table 1. I/O types

Type	Function
I	Input
I-PD	Input with internal pull down resistor
I-PU	Input with internal pull up resistor
O	Output
OZ	Tri-state output
B	Bidirectional
G	Ground
P	Power

Table 2. I/O driver function

Driver	Function
BD4STARP_TC	CMOS bi-directional, 4mA, schmitt trigger on input, active slew rate control, 3.3V capable
BD8STARP_TC	CMOS bi-directional, 8mA, schmitt trigger on input, active slew rate control, 3.3V capable
TLCHT_TC	TTL input, 3.3V compatible
TLCHTDQ_TC	TTL input, 3.3V compatible, pull down, IDDq control
TLCHTUQ_TC	TTL input, 3.3V compatible, pull up, IDDq control

Table 3. PQFP 160 pin list

Pin #	Signal Name	Signal type	Technology	Description
1	VSS	G		
2	AD_00	B	BD8STARP_TC	Address/Data Bus
3	AD_01	B	BD8STARP_TC	Address/Data Bus
4	AD_02	B	BD8STARP_TC	Address/Data Bus
5	AD_03	B	BD8STARP_TC	Address/Data Bus
6	VDDIO	P		VSSIO+3.3V
7	AD_04	B	BD8STARP_TC	Address/Data Bus
8	AD_05	B	BD8STARP_TC	Address/Data Bus
9	AD_06	B	BD8STARP_TC	Address/Data Bus
10	AD_07	B	BD8STARP_TC	Address/Data Bus
11	VSSIO	G		
12	AD_08	B	BD8STARP_TC	Address/Data Bus
13	AD_09	B	BD8STARP_TC	Address/Data Bus
14	AD_10	B	BD8STARP_TC	Address/Data Bus
15	AD_11	B	BD8STARP_TC	Address/Data Bus
16	VDD	P		VSS+1.8V
17	AD_12	B	BD8STARP_TC	Address/Data Bus
18	AD_13	B	BD8STARP_TC	Address/Data Bus
19	AD_14	B	BD8STARP_TC	Address/Data Bus
20	AD_15	B	BD8STARP_TC	Address/Data Bus
21	VSS	G		
22	PCLK	I	TLCHT_TC	Processor Clock
23	BE	I	TLCHT_TC	Address bit 1
24	ALE	I	TLCHT_TC	Address Latch
25	CSB_0	I	TLCHT_TC	Chip select line 0
26	VDD	P		VSS+1.8V
27	CSB_1	I	TLCHT_TC	Chip select line 1
28	CSB_2	I	TLCHT_TC	Chip select line 2
29	CSB_3	I	TLCHT_TC	Chip select line 3
30	WR_RDB	I	TLCHT_TC	Write/Not read
31	VSS	G		
32	RDYB	OZ	BD4STARP_TC	Ready indication
33	OBC_TYPE	I-PD	TLCHTDQ_TC	I960/Generic selection
34	INTB_0	O	BD4STARP_TC	Requests OBC interrupt service line 0

Table 3. PQFP 160 pin list (continued)

Pin #	Signal Name	Signal type	Technology	Description
35	INTB_1	O	BD4STARP_TC	Requests OBC interrupt service line 1
36	VDD	P		VSS+1.8V
37	INTB_2	O	BD4STARP_TC	Requests OBC interrupt service line 2
38	INTB_3	O	BD4STARP_TC	Requests OBC interrupt service line 3
39	RESETB	I	TLCHT_TC	Hard reset
40	VSS	G		
41	VDD	P		VSS+1.8V
42	TDO	OZ	BD4STARP_TC	Boundary scan out
43	TDI	I-PU	TLCHTUQ_TC	Boundary scan in
44	TMS	I-PU	TLCHTUQ_TC	Tap controller signal
45	TCK	I-PD	TLCHTDQ_TC	Boundary scan clock
46	TRSTB	I-PD	TLCHTDQ_TC	Not reset of Tap controller
47	VSS	G		
48	TESTE	I-PD	TLCHTDQ_TC	Enables scan test mode
49	VSSIO	G		
50	U_RXDATA_0	OZ	BD8STARP_TC	Utopia receive data bus
51	U_RXDATA_1	OZ	BD8STARP_TC	Utopia receive data bus
52	U_RXDATA_2	OZ	BD8STARP_TC	Utopia receive data bus
53	U_RXDATA_3	OZ	BD8STARP_TC	Utopia receive data bus
54	U_RXDATA_4	OZ	BD8STARP_TC	Utopia receive data bus
55	U_RXDATA_5	OZ	BD8STARP_TC	Utopia receive data bus
56	U_RXDATA_6	OZ	BD8STARP_TC	Utopia receive data bus
57	U_RXDATA_7	OZ	BD8STARP_TC	Utopia receive data bus
58	VDDIO	P		VSSIO+3.3V
59	U_RXSOC	OZ	BD8STARP_TC	Utopia receive start of cell
60	U_RXCLK	I	TLCHT_TC	Utopia receive clock
61	U_RXENBB	I	TLCHT_TC	Utopia receive not enable
62	U_RXCLAV	OZ		Utopia receive cell available
63	VDD	P		VSS+1.8V
64	U_RXADDR_0	I	TLCHT_TC	Utopia receive address
65	U_RXADDR_1	I	TLCHT_TC	Utopia receive address
66	U_RXADDR_2	I	TLCHT_TC	Utopia receive address
67	U_RXADDR_3	I	TLCHT_TC	Utopia receive address
68	U_RXADDR_4	I	TLCHT_TC	Utopia receive address
69	VSS	G		
70	AFRESET_0	O	BD4STARP_TC	MTC20455 Reset line 0
71	PDOWN_0	O	BD4STARP_TC	MTC20455 power down line 0
72	AFRXD_0_0	I	TLCHT_TC	Receive data nibble line 0
73	AFRXD_0_1	I	TLCHT_TC	Receive data nibble line 0
74	AFRXD_0_2	I	TLCHT_TC	Receive data nibble line 0
75	AFRXD_0_3	I	TLCHT_TC	Receive data nibble line 0
76	VSSIO	G		
77	CLWD_0	I	TLCHT_TC	Start of word indication line 0

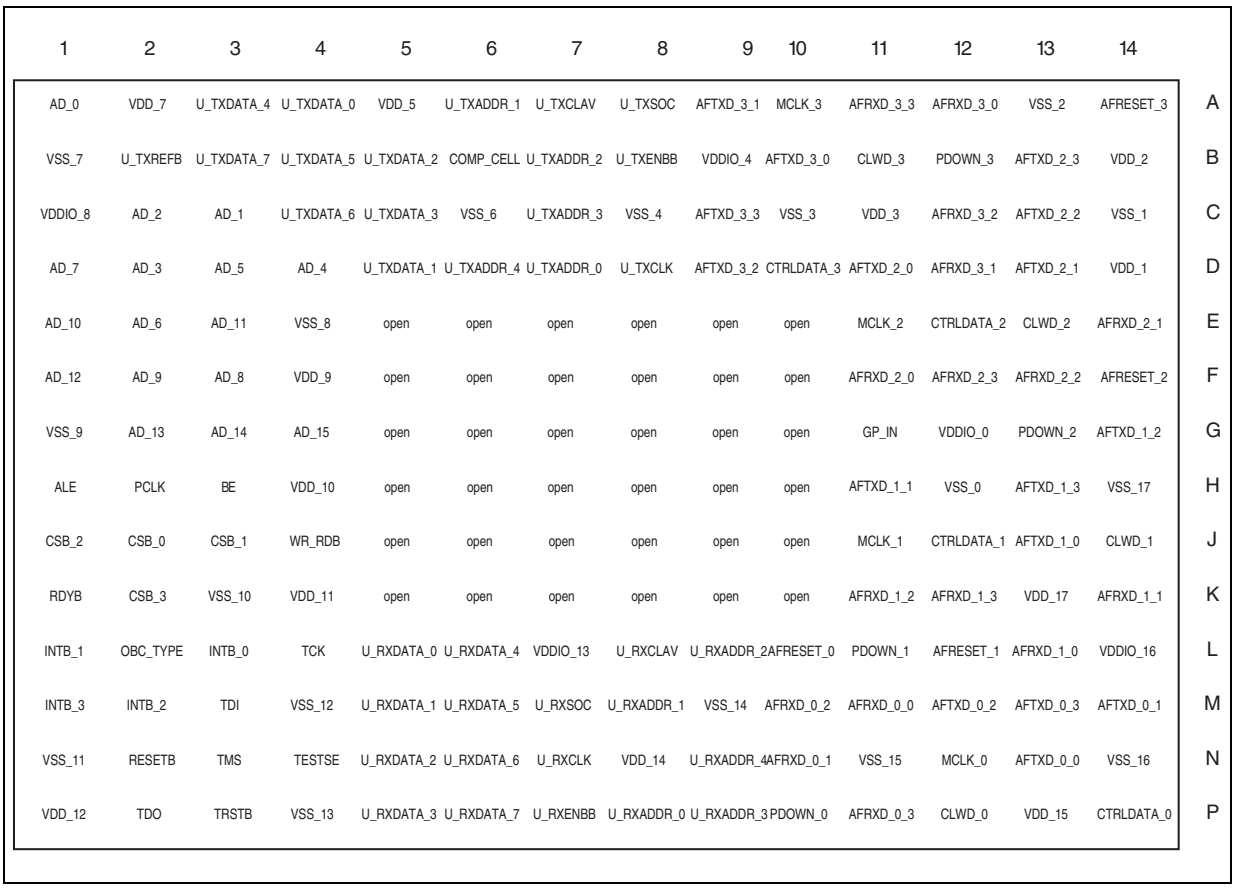
Table 3. PQFP 160 pin list (continued)

Pin #	Signal Name	Signal type	Technology	Description
78	MCLK_0	I	TLCHT_TC	Master clock line 0
79	CTRLDATA_0	O	BD4STARP_TC	Serial data transmit channel line 0
80	VDD	P		VSS+1.8V
81	VSS	G		
82	AFTXD_0_0	O	BD4STARP_TC	Transmit data nibble line 0
83	AFTXD_0_1	O	BD4STARP_TC	Transmit data nibble line 0
84	AFTXD_0_2	O	BD4STARP_TC	Transmit data nibble line 0
85	AFTXD_0_3	O	BD4STARP_TC	Transmit data nibble line 0
86	VDDIO	P		VSSIO+3.3V
87	AFRESET_1	O	BD4STARP_TC	MTC20455 Reset line 1
88	PDOWN_1	O	BD4STARP_TC	MTC20455 power down line 1
89	AFRXD_1_0	I	TLCHT_TC	Receive data nibble line 1
90	AFRXD_1_1	I	TLCHT_TC	Receive data nibble line 1
91	AFRXD_1_2	I	TLCHT_TC	Receive data nibble line 1
92	AFRXD_1_3	I	TLCHT_TC	Receive data nibble line 1
93	VDD	P		VSS+1.8V
94	CLWD_1	I	TLCHT_TC	Start of word indication line 1
95	MCLK_1	I	TLCHT_TC	Master clock line 1
96	CTRLDATA_1	O	BD4STARP_TC	Serial data transmit channel line 1
97	VSSIO	G		
98	AFTXD_1_0	O	BD4STARP_TC	Transmit data nibble line 1
99	AFTXD_1_1	O	BD4STARP_TC	Transmit data nibble line 1
100	AFTXD_1_2	O	BD4STARP_TC	Transmit data nibble line 1
101	AFTXD_1_3	O	BD4STARP_TC	Transmit data nibble line 1
102	VSS	G		
103	GP_IN	I-PD	TLCHTDQ_TC	General purpose input for DspFe test
104	AFRESET_2	O	BD4STARP_TC	MTC20455 Reset line 2
105	PDOWN_2	O	BD4STARP_TC	MTC20455 power down line 2
106	VDDIO	P		VSSIO+3.3V
107	AFRXD_2_0	I	TLCHT_TC	Receive data nibble line 2
108	AFRXD_2_1	I	TLCHT_TC	Receive data nibble line 2
109	AFRXD_2_2	I	TLCHT_TC	Receive data nibble line 2
110	AFRXD_2_3	I	TLCHT_TC	Receive data nibble line 2
111	VDD	P		VSS+1.8V
112	CLWD_2	I	TLCHT_TC	Start of word indication line 2
113	MCLK_2	I	TLCHT_TC	Master clock line 2
114	CTRLDATA_2	O	BD4STARP_TC	Serial data transmit channel line 2
115	VSS	G		
116	AFTXD_2_0	O	BD4STARP_TC	Transmit data nibble line 2
117	AFTXD_2_1	O	BD4STARP_TC	Transmit data nibble line 2
118	AFTXD_2_2	O	BD4STARP_TC	Transmit data nibble line 2
119	AFTXD_2_3	O	BD4STARP_TC	Transmit data nibble line 2
120	VDD	P		VSS+1.8V

Table 3. PQFP 160 pin list (continued)

Pin #	Signal Name	Signal type	Technology	Description
121	VSS	G		
122	AFRESET_3	O	BD4STARP_TC	MTC20455 Reset line 3
123	PDOWN_3	O	BD4STARP_TC	MTC20455 power down line 3
124	AFRXD_3_0	I	TLCHT_TC	Receive data nibble line 3
125	AFRXD_3_1	I	TLCHT_TC	Receive data nibble line 3
126	AFRXD_3_2	I	TLCHT_TC	Receive data nibble line 3
127	AFRXD_3_3	I	TLCHT_TC	Receive data nibble line 3
128	VDD	P		VSS+1.8V
129	CLWD_3	I	TLCHT_TC	Start of word indication line 3
130	MCLK_3	I	TLCHT_TC	Master clock line 3
131	CTRLDATA_3	O	BD4STARP_TC	Serial data transmit channel line 3
132	VSSIO	G		
133	AFTXD_3_0	O	BD4STARP_TC	Transmit data nibble line 3
134	AFTXD_3_1	O	BD4STARP_TC	Transmit data nibble line 3
135	AFTXD_3_2	O	BD4STARP_TC	Transmit data nibble line 3
136	AFTXD_3_3	O	BD4STARP_TC	Transmit data nibble line 3
137	U_TXSOC	I	TLCHT_TC	Utopia transmit start of cell
138	VDDIO	P		VSSIO+3.3V
139	U-TXCLK	I	TLCHT_TC	Utopia transmit clock
140	U_TXENBB	I	TLCHT_TC	Utopia transmit not enable
141	U_TXCLAV	OZ	BD8STARP_TC	Utopia transmit cell available
142	VSS	G		
143	U_TXADDR_0	I	TLCHT_TC	Utopia transmit address
144	U_TXADDR_1	I	TLCHT_TC	Utopia transmit address
145	U_TXADDR_2	I	TLCHT_TC	Utopia transmit address
146	U_TXADDR_3	I	TLCHT_TC	Utopia transmit address
147	U_TXADDR_4	I	TLCHT_TC	Utopia transmit address
148	VDD	P		VSS+1.8V
149	COMP_CELL	O	COMPENSATION_VSS	Resistance for compensation cell
150	VSS	G		
151	U_TXDATA_0	I	TLCHT_TC	Utopia transmit data bus
152	U_TXDATA_1	I	TLCHT_TC	Utopia transmit data bus
153	U_TXDATA_2	I	TLCHT_TC	Utopia transmit data bus
154	U_TXDATA_3	I	TLCHT_TC	Utopia transmit data bus
155	U_TXDATA_4	I	TLCHT_TC	Utopia transmit data bus
156	U_TXDATA_5	I	TLCHT_TC	Utopia transmit data bus
157	U_TXDATA_6	I	TLCHT_TC	Utopia transmit data bus
158	U-TXDATA_7	I	TLCHT_TC	Utopia transmit data bus
159	U_TXREFB	I	TLCHT_TC	8kHz from network
160	VDD	P		VSS+1.8V

Figure 3. LFBGA160 package pin out (Sachem4 top view)



1	2	3	4	5	6	7	8	9	10	11	12	13	14	
AD_0	VDD_7	U_TXDATA_4	U_TXDATA_0	VDD_5	U_TXADDR_1	U_TXCLAV	U_TXSOC	AFTXD_3_1	MCLK_3	AFRXD_3_3	AFRXD_3_0	VSS_2	AFRESET_3	A
VSS_7	U_TXREFB	U_TXDATA_7	U_TXDATA_5	U_TXDATA_2	COMP_CELL	U_TXADDR_2	U_TXENBB	VDDIO_4	AFTXD_3_0	CLWD_3	PDOWN_3	AFTXD_2_3	VDD_2	B
VDDIO_8	AD_2	AD_1	U_TXDATA_6	U_TXDATA_3	VSS_6	U_TXADDR_3	VSS_4	AFTXD_3_3	VSS_3	VDD_3	AFRXD_3_2	AFTXD_2_2	VSS_1	C
AD_7	AD_3	AD_5	AD_4	U_TXDATA_1	U_TXADDR_4	U_TXADDR_0	U_TXCLK	AFTXD_3_2	CTRLDATA_3	AFTXD_2_0	AFRXD_3_1	AFTXD_2_1	VDD_1	D
AD_10	AD_6	AD_11	VSS_8	open	open	open	open	open	open	MCLK_2	CTRLDATA_2	CLWD_2	AFRXD_2_1	E
AD_12	AD_9	AD_8	VDD_9	open	open	open	open	open	open	AFRXD_2_0	AFRXD_2_3	AFRXD_2_2	AFRESET_2	F
VSS_9	AD_13	AD_14	AD_15	open	open	open	open	open	open	GP_IN	VDDIO_0	PDOWN_2	AFTXD_1_2	G
ALE	PCLK	BE	VDD_10	open	open	open	open	open	open	AFTXD_1_1	VSS_0	AFTXD_1_3	VSS_17	H
CSB_2	CSB_0	CSB_1	WR_RDB	open	open	open	open	open	open	MCLK_1	CTRLDATA_1	AFTXD_1_0	CLWD_1	J
RDYB	CSB_3	VSS_10	VDD_11	open	open	open	open	open	open	AFRXD_1_2	AFRXD_1_3	VDD_17	AFRXD_1_1	K
INTB_1	OBC_TYPE	INTB_0	TCK	U_RXDATA_0	U_RXDATA_4	VDDIO_13	U_RXCLAV	U_RXADDR_2	AFRESET_0	PDOWN_1	AFRESET_1	AFRXD_1_0	VDDIO_16	L
INTB_3	INTB_2	TDI	VSS_12	U_RXDATA_1	U_RXDATA_5	U_RXSOC	U_RXADDR_1	VSS_14	AFRXD_0_2	AFRXD_0_0	AFTXD_0_2	AFTXD_0_3	AFTXD_0_1	M
VSS_11	RESETB	TMS	TESTSE	U_RXDATA_2	U_RXDATA_6	U_RXCLK	VDD_14	U_RXADDR_4	AFRXD_0_1	VSS_15	MCLK_0	AFTXD_0_0	VSS_16	N
VDD_12	TDO	TRSTB	VSS_13	U_RXDATA_3	U_RXDATA_7	U_RXENBB	U_RXADDR_0	U_RXADDR_3	PDOWN_0	AFRXD_0_3	CLWD_0	VDD_15	CTRLDATA_0	P

Table 4. LFBGA 160 pin list

Pin #	Signal Name	Signal type	Technology	Description
B1	VSS	G		
A1	AD_00	B	BD8STARP_TC	Address/Data Bus
C3	AD_01	B	BD8STARP_TC	Address/Data Bus
C2	AD_02	B	BD8STARP_TC	Address/Data Bus
D2	AD_03	B	BD8STARP_TC	Address/Data Bus
C1	VDDIO	P		VSSIO+3.3V
D4	AD_04	B	BD8STARP_TC	Address/Data Bus
D3	AD_05	B	BD8STARP_TC	Address/Data Bus
E2	AD_06	B	BD8STARP_TC	Address/Data Bus
D1	AD_07	B	BD8STARP_TC	Address/Data Bus
E4	VSSIO	G		
F3	AD_08	B	BD8STARP_TC	Address/Data Bus
F2	AD_09	B	BD8STARP_TC	Address/Data Bus
E1	AD_10	B	BD8STARP_TC	Address/Data Bus
E3	AD_11	B	BD8STARP_TC	Address/Data Bus

Table 4. LFBGA 160 pin list (continued)

Pin #	Signal Name	Signal type	Technology	Description
F4	VDD	P		VSS+1.8V
F1	AD_12	B	BD8STARP_TC	Address/Data Bus
G2	AD_13	B	BD8STARP_TC	Address/Data Bus
G3	AD_14	B	BD8STARP_TC	Address/Data Bus
G4	AD_15	B	BD8STARP_TC	Address/Data Bus
G1	VSS	G		
H2	PCLK	I	TLCHT_TC	Processor Clock
H3	BE	I	TLCHT_TC	Address bit 1
H1	ALE	I	TLCHT_TC	Address Latch
J2	CSB_0	I	TLCHT_TC	Chip select line 0
H4	VDD	P		VSS+1.8V
J3	CSB_1	I	TLCHT_TC	Chip select line 1
J1	CSB_2	I	TLCHT_TC	Chip select line 2
K2	CSB_3	I	TLCHT_TC	Chip select line 3
J4	WR_RDB	I	TLCHT_TC	Write/Not read
K3	VSS	G		
K1	RDYB	OZ	BD4STARP_TC	Ready indication
L2	OBC_TYPE	I-PD	TLCHTDQ_TC	I960/Generic selection
L3	INTB_0	O	BD4STARP_TC	Requests OBC interrupt service line 0
L1	INTB_1	O	BD4STARP_TC	Requests OBC interrupt service line 1
K4	VDD	P		VSS+1.8V
M2	INTB_2	O	BD4STARP_TC	Requests OBC interrupt service line 2
M1	INTB_3	O	BD4STARP_TC	Requests OBC interrupt service line 3
N2	RESETB	I	TLCHT_TC	Hard reset
N1	VSS	G		
P1	VDD	P		VSS+1.8V
P2	TDO	OZ	BD4STARP_TC	Boundary scan out
M3	TDI	I-PU	TLCHTUQ_TC	Boundary scan in
N3	TMS	I-PU	TLCHTUQ_TC	Tap controller signal
L4	TCK	I-PD	TLCHTDQ_TC	Boundary scan clock
P3	TRSTB	I-PD	TLCHTDQ_TC	Not reset of Tap controller
M4	VSS	G		
N4	TESTE	I-PD	TLCHTDQ_TC	Enables scan test mode
P4	VSSIO	G		
L5	U_RXDATA_0	OZ	BD8STARP_TC	Utopia receive data bus
M5	U_RXDATA_1	OZ	BD8STARP_TC	Utopia receive data bus
N5	U_RXDATA_2	OZ	BD8STARP_TC	Utopia receive data bus
P5	U_RXDATA_3	OZ	BD8STARP_TC	Utopia receive data bus
L6	U_RXDATA_4	OZ	BD8STARP_TC	Utopia receive data bus
M6	U_RXDATA_5	OZ	BD8STARP_TC	Utopia receive data bus
N6	U_RXDATA_6	OZ	BD8STARP_TC	Utopia receive data bus
P6	U_RXDATA_7	OZ	BD8STARP_TC	Utopia receive data bus
L7	VDDIO	P		VSSIO+3.3V

Table 4. LFBGA 160 pin list (continued)

Pin #	Signal Name	Signal type	Technology	Description
M7	U_RXSOC	OZ	BD8STARP_TC	Utopia receive start of cell
N7	U_RXCLK	I	TLCHT_TC	Utopia receive clock
P7	U_RXENBB	I	TLCHT_TC	Utopia receive not enable
L8	U_RXCLAV	OZ		Utopia receive cell available
N8	VDD	P		VSS+1.8V
D11	AFTXD_2_0	O	BD4STARP_TC	Transmit data nibble line 2
D13	AFTXD_2_1	O	BD4STARP_TC	Transmit data nibble line 2
C13	AFTXD_2_2	O	BD4STARP_TC	Transmit data nibble line 2
B13	AFTXD_2_3	O	BD4STARP_TC	Transmit data nibble line 2
B14	VDD	P		VSS+1.8V
A13	VSS	G		
A14	AFRESET_3	O	BD4STARP_TC	MTC20455 Reset line 3
B12	PDOWN_3	O	BD4STARP_TC	MTC20455 power down line 3
A12	AFRXD_3_0	I	TLCHT_TC	Receive data nibble line 3
D12	AFRXD_3_1	I	TLCHT_TC	Receive data nibble line 3
C12	AFRXD_3_2	I	TLCHT_TC	Receive data nibble line 3
A11	AFRXD_3_3	I	TLCHT_TC	Receive data nibble line 3
C11	VDD	P		VSS+1.8V
B11	CLWD_3	I	TLCHT_TC	Start of word indication line 3
A10	MCLK_3	I	TLCHT_TC	Master clock line 3
D10	CTRLDATA_3	O	BD4STARP_TC	Serial data transmit channel line 3
C10	VSSIO	G		
B10	AFTXD_3_0	O	BD4STARP_TC	Transmit data nibble line 3
A9	AFTXD_3_1	O	BD4STARP_TC	Transmit data nibble line 3
D9	AFTXD_3_2	O	BD4STARP_TC	Transmit data nibble line 3
C9	AFTXD_3_3	O	BD4STARP_TC	Transmit data nibble line 3
A8	U_TXSOC	I	TLCHT_TC	Utopia transmit start of cell
B9	VDDIO	P		VSSIO+3.3V
D8	U-TXCLK	I	TLCHT_TC	Utopia transmit clock
B8	U_TXENBB	I	TLCHT_TC	Utopia transmit not enable
A7	U_TXCLAV	OZ	BD8STARP_TC	Utopia transmit cell available
C8	VSS	G		
D7	U_TXADDR_0	I	TLCHT_TC	Utopia transmit address
A6	U_TXADDR_1	I	TLCHT_TC	Utopia transmit address
B7	U_TXADDR_2	I	TLCHT_TC	Utopia transmit address
C7	U_TXADDR_3	I	TLCHT_TC	Utopia transmit address
D6	U_TXADDR_4	I	TLCHT_TC	Utopia transmit address
A5	VDD	P		VSS+1.8V
B6	COMP_CELL	O	COMPENSATION_VSS	Resistance for compensation cell
C6	VSS	G		
A4	U_TXDATA_0	I	TLCHT_TC	Utopia transmit data bus
D5	U_TXDATA_1	I	TLCHT_TC	Utopia transmit data bus
B5	U_TXDATA_2	I	TLCHT_TC	Utopia transmit data bus

Table 4. LFBGA 160 pin list (continued)

Pin #	Signal Name	Signal type	Technology	Description
C5	U_TXDATA_3	I	TLCHT_TC	Utopia transmit data bus
A3	U_TXDATA_4	I	TLCHT_TC	Utopia transmit data bus
B4	U_TXDATA_5	I	TLCHT_TC	Utopia transmit data bus
C4	U_TXDATA_6	I	TLCHT_TC	Utopia transmit data bus
B3	U-TXDATA_7	I	TLCHT_TC	Utopia transmit data bus
B2	U_TXREFB	I	TLCHT_TC	8kHz from network
A2	VDD	P		VSS+1.8V

ELECTRICAL SPECIFICATIONS GENERIC

The values presented in the following table apply for all inputs and/or outputs unless specified otherwise. Specifically they are not influenced by the choice between CMOS or TTL levels.

Table 5. I/O Buffers generic DC Characteristics

DC Electrical Characteristics **All voltages are referenced to Vss, unless otherwise specified, positive current is towards the device**						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
IIN	Input leakage current	VIN = VSS, VDDIO, no pull up/pull down	-1		1	µA
IOZ	Tristate leakage current	VIN = VSS, VDDIO,	-1		1	µA
		no pull up/pull down				
IPU	Pull up current	VIN = VSS	-15	-46.7	-100	µA
IPD	Pull down current	VIN = VDDIO	12.5	39.4	90	µA
Rpu	Pull up resistance	VIN = VSS	35	70.5	200	kOhm
RPD	Pull down resistance	VIN = VDDIO	40	83.7	240	kOhm
IDC	Static current fromVDDIO	NORMAL MODE	1.7			µA
		COREOFF MODE (no VDD)	11.6			µA
		IDDQ MODE (VDDIO <2.5)	-			µA

Table 6. IO buffers dynamic characteristic

DC Electrical Characteristics, important for transient but measured at (near) DC. **All voltages are referenced to VSS, unless otherwise specified, positive current is towards the device**						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
CIN	Input capacitance	@f = 1 MHz			5	pF
dI/dt	Current derivative	8 mA driver, (active slew rate control)	20		50	mA/ns
Ipeak	Peak current	8 mA driver, (active slew rate control)		85		mA
COUT	Output capacitance (also bidirectional and tristate drivers)	@f = 1MHz			7	pF

Input/Output CMOS Generic Characteristics

The values presented in the following table apply for all CMOS inputs and/ or outputs unless specified otherwise.

Table 7. TTL IO buffers generic characteristics

DC Electrical Characteristics All voltages are referenced to VSS, unless otherwise specified, positive current is towards the device						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
VIL	Low level input voltage				0.2*VDD	V
VIH	High level input voltage		0.8*vDD			V
VHY	Schmitt trigger hysteresis	slow edge <1V/µs only for SCHMITT	0.8			V
VOL	Low level output voltage	IOUT = XMa*			0.4	V
VOH	High level output voltage	IOUT = -Xma*	0.85*vDD			V

* The reference current is dependent on the exact buffer chosen and is part of the buffer name. The available values are 4 and 8mA.

Input/Output TTL Generic Characteristics

The values presented in the following table apply for all TTL inputs and/or outputs unless specified otherwise.

Table 8. TTL IO buffers generic characteristics

DC Electrical Characteristics, important for transient but measured at (near) DC. All voltages are referenced to VSS, unless otherwise specified, positive current is towards the device						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
VIL	Low level input voltage				0.8	V
VIH	High level input voltage		2.0			V
VILHY	Low level threshold, falling	slow edge < 1V/µs	0.9		1.35	V
VIHHY	High level threshold, rising	slow edge < 1V/µs	1.3		1.9	V
VHY	Schmitt trigger hysteresis	slow edge <1V/µs	0.4		0.7	V
VOL	Low level output voltage	IOUT = XMa*			0.4	V
VOH	High level output voltage	IOUT = -Xma*	2.4			V

* The reference current is dependent on the exact buffer chosen and is part of the buffer name. The available values are 2,4, and 8mA.

Operating Conditions

Table 9. Operating Conditions

Maximum ratings						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
VDDIO	IO Supply voltage		3.0	3.3	3.6	V
VDD	Core Supply voltage		1.62	1.8	2.0	V
TA	Ambient temperature 1m/s airflow		-40		+85	°C
P	Power dissipation				1000	mW

Functional Description

Fig.4 shows the global block diagram of the MTC20455. The functions can be grouped into the following:

- DMT modems
- Quad or single AFE interface
- Utopia interface
- Controller interface
- Miscellaneous

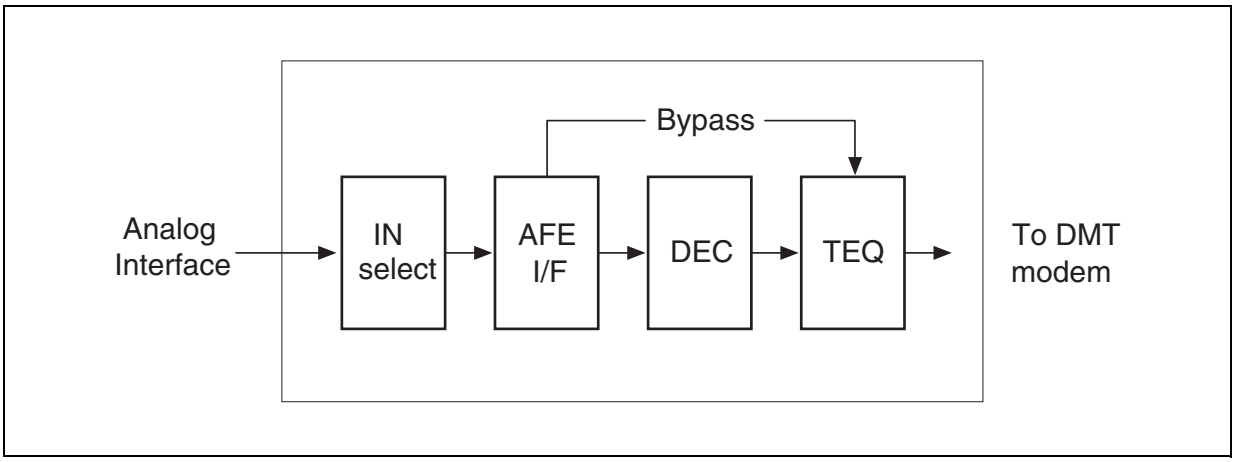
DMT Modem Description

The following section essentially describes the sequence of actions for the receive direction, corresponding functions for the transmit direction are readily derived.

DSP Front-End

The DSP Front-End contains 4 parts in the receive direction: the Input Selector, the Analog Front-End Interface, the Decimator and the Time Equaliser. The input selector is used internally to enable test loopbacks inside the chip. The Analog Front-End Interface transfers 1 6-bits word, multiplexed on 4 input/output signals. As a result, 4 clock cycles are needed to transfer 1 word. The Decimator receives the 16-bits samples at 8.8 MHz (as sent by the Analog Front-End chip) and reduces this rate to 2.2 MHz. The Time Equaliser (TEQ) module is an FIR filter with programmable coefficients. Its main purpose is to reduce the effect of Inter-Symbol Interference (ISI) by shortening the channel impulse response. Both the Decimator and TEQ can be bypassed. In the transmit direction, the DSP Front-End includes: sidelobe filtering, clipping, delay equalisation and interpolation. The sidelobe filtering and delay equalisation are implemented by IIR filters, reducing the effect of echo in FDM systems. Clipping is a statistical process limiting the amplitude of the output signal, optimising the dynamic range of the AFE. The interpolator receives data at 2.2 MHz and generates samples at a rate of 8.8 MHz.

Figure 4. DSP Front-End



DMT Modem

This computational module is a programmable DSP unit. Its instruction set enables functions like FFT, IFFT, Scaling, Rotor and Frequency Equali-sation (FEQ). This block implements the core of the DMT algorithm as specified in ANSI T1.413. In the RX path, the 512-point FFT transforms the time-domain DMT symbol into a frequency domain representation which can be further decoded by the subsequent de-mapping stages. After the first stage time / domain equalisation and FFT block – an essentially ICI (InterCarrier Interference) – free carrier information stream has been obtained.

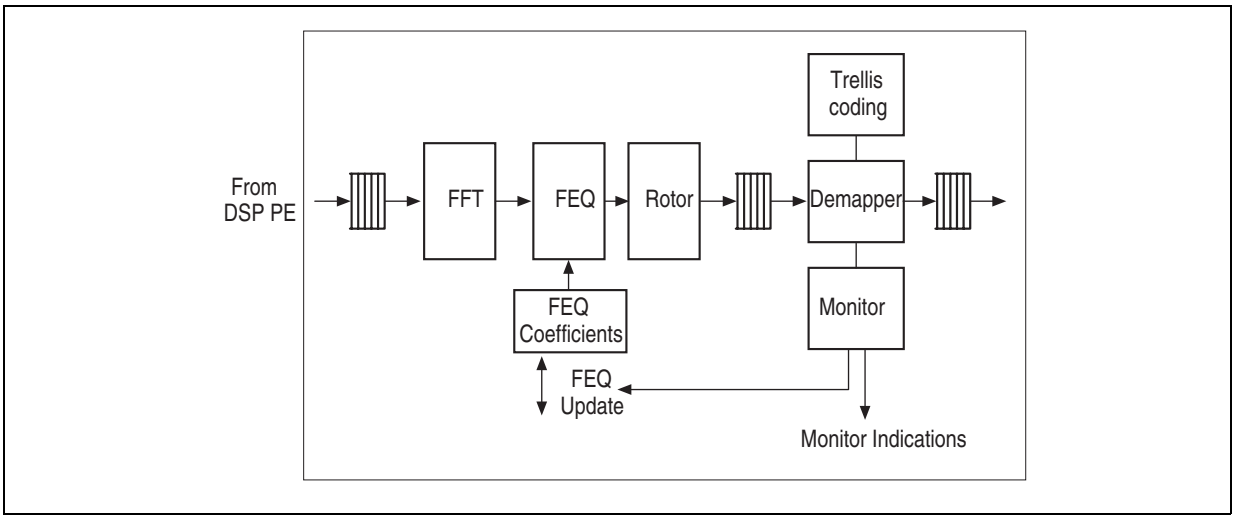
This stream is still affected by carrier-specific channel distortion resulting in an attenuation of the signal

amplitude and a rotation of the signal phase. To compensate for these effects, the FFT is followed by a Frequency domain equaliser (FEQ) and a Rotor (phase shifter).

In the TX path, the IFFT transforms the DMT symbol generated in the frequency domain by the mapper into a time domain representation. The IFFT block is preceded by a Fine Tune Gain and a Rotor stage, allowing for a compensation of the possible frequency mismatch between the master clock frequency and the transmitter clock frequency (which may be locked to another reference).

The FFT module is a slave DSP engine controlled by the transceiver controller. It works off line and communicates with the other blocks via buffers controlled by the DSTU (DMT Symbol Timing Unit)block. The DSP executes a program stored in a RAM area, a very flexible implementation open for future enhancements.

Figure 5. DMT Modem



DPLL

The Digital PLL module receives a metric for the phase error of the pilot tone. In general, the clock frequencies at the transmitter and receiver do not match exactly. The phase error is filtered and integrated by a low pass filter, yielding an estimation of the frequency offset. Various processes can use this estimate to deal with the frequency mismatch. In particular, small accumulated phase errors can be compensated in the frequency domain by a rotation of the received code constellation (Rotor). Larger errors are compensated in the time domain by inserting or deleting clock cycles in the sample input sequence.

Mapper/Demapper, Monitor, Trellis Coding, FEQ Update

The Demapper converts the constellation points computed by the FFT to a block of bits. This essentially consists in identifying a point in a 2D QAM constellation plane. The Demapper supports trellis coded demodulation and provides a Viterbi maximum likelihood estimator. When the trellis is active, the Demapper receives an indication for the most likely constellation subset to be used. In the transmit direction, the Mapper performs the inverse operation, mapping a block of bits into one constellation point (in a complex x+jy representation) which is passed to the IFFT block. The Trellis Encoder generates redundant bits to improve the robustness of the transmission, using a 4-Dimensional Trellis Coded Modulation scheme.

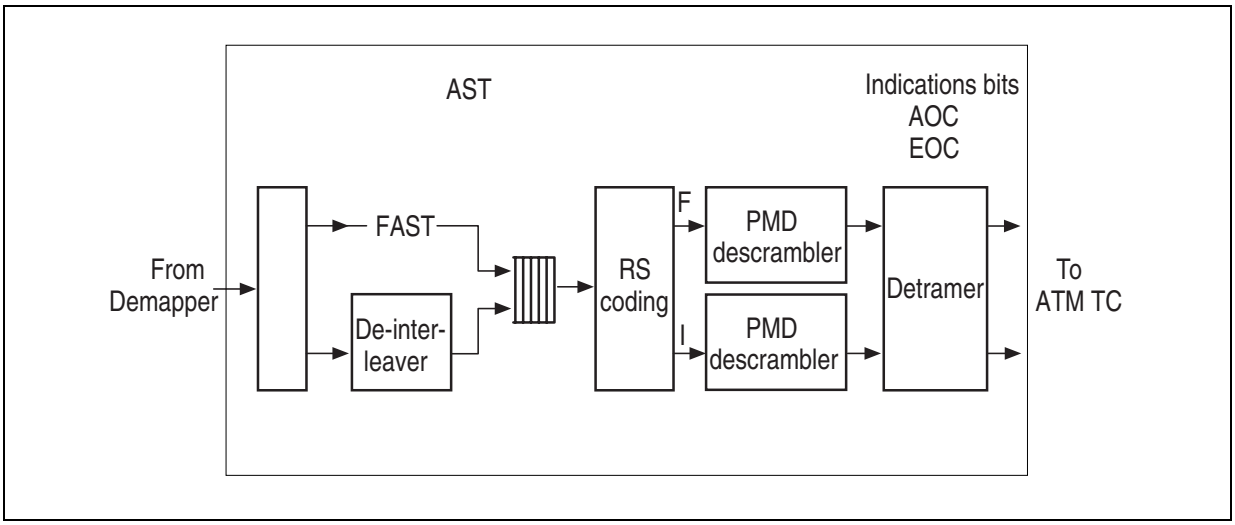
The Monitor computes error parameters for carriers specified in the Demapper process. Those parameters can be used for updates of adaptive filters coefficients, clock phase adjustments, error detection, etc. A series of values is constantly monitored, such as signal power, pilot phase deviations, symbol erasures generation, loss of frame, etc.

Generic TC Layer Functions

These functions relate to byte oriented data streams. They are completely described in ANSI T1.413. Additions described in the Issue 2 of this specification are also supported. The data received from the demapper is split into two paths, one dedicated to an interleaved data flow, the other one for a non-interleaved data flow. These data flows are also referred to as slow and fast data flows. The interleaving/-de-interleaving is used to increase the error correcting capabilityof block codes for error bursts. After de-interleaving (if applicable), the data flow enters a Reed-Solomon error correcting code decoder, able to correct a number of bytes containing bit errors. The decoder also uses the information of previous receiving stages that may have detected the errored bytes and have labelled them with an “erasure” indication. Each time the RS decoder detects and corrects errors in a RS codeword, an RS correction event is generated. The occurrence of such events can be signalled to the management layer. After leaving the RS decoder, the corrected byte stream is descrambled in the PMD (Physical Medium Dependent) descramblers.

Two descramblers are used, for interleaved and non-interleaved data flows. These are defined in ANSI T1.413. After descrambling, the data flows enter the Deframer that extracts and processes bytes to support physical layer-related functions according to ANSI T1.413. The ADSL frames indeed contain physical layer-related information in addition to the data passed to the higher layers. In particular, the deframer extracts the EOC (Embedded Operations Channel), the AOC (ADSL Overhead Control) and the indicators bits and passes them to the appropriate processing unit (e.g. the transceiver controller). The deframer also performs a CRC check (Cyclic Redundancy Check) on the received frame and generates events in case of error detection. Event counters can be read by management processes. The outputs of the deframer are an interleaved and a fast data stream. These data streams can either carry ATM cells or another type of traffic. In the latter case, the ATM specific TC layer functional block, described hereafter, is bypassed and the data stream is directly presented at the input of the interface module.

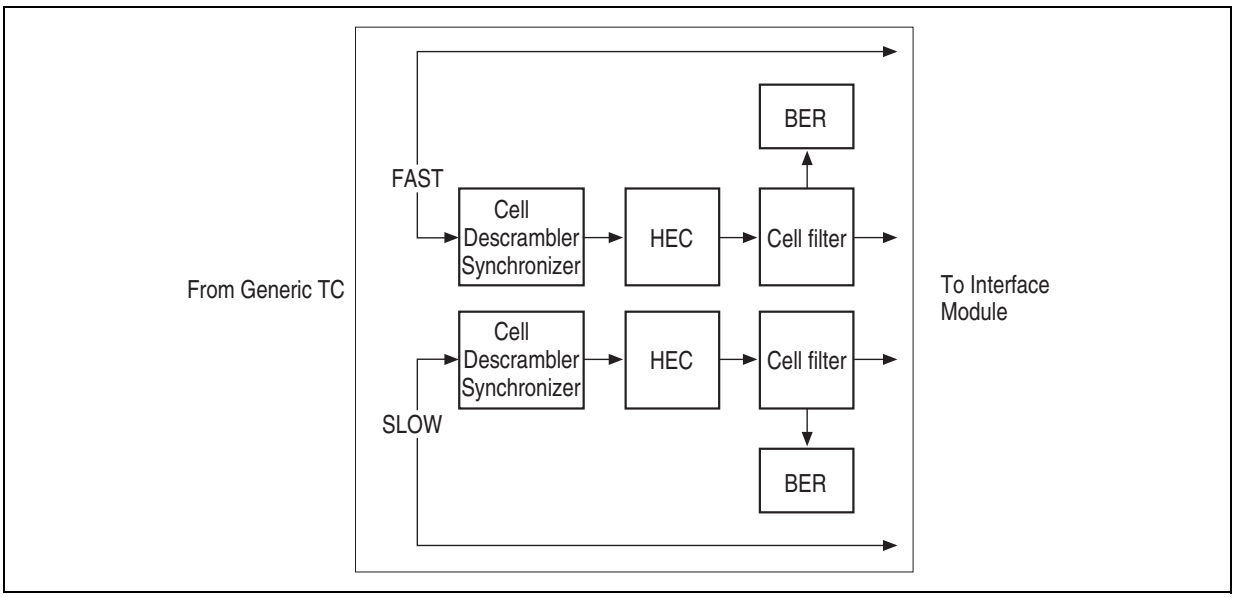
Figure 6. Generic TC Layer Functions



ATM Specific TC Layer Functions

The 2 byte streams (fast and slow) are received from the byte-based processing unit. When ATM cells are transported, this block provides basic cell functions such as cell synchronisa-tion, cell payload descrambling, idle/-unassigned cell filter, cell Header Error Correction (HEC) and detection. The cell processing happens according to ITU-T I.163 standard. Provision is also made for BER measurements at this ATM cell level. When non cell oriented byte streams are transported, the cell processing unit is not active.

Figure 7. ATM Specific TC Layer Functions



DMT Symbol Timing Unit (DSTU)

The DSTU interfaces with various modules, like DSP Front-End, FFT/IFFT, Mapper/Demapper, RS, Monitor and Transceiver Controller. It consists of a real time and a scheduler module. The real time unit generates a time-base for the DMT symbols (sample counter), superframes (symbol counter) and hyperframes (sync counter). The timebases can be modified by various control features. They are continuously fine-tuned by the DPLL module. The DSTU schedulers execute a program, controlled by program opcodes and a set of variables, the most important of which are real time counters. The transmit and receive sequencers are completely independent and run different programs. An independent set of variables is assigned to each of them. The sequencer programs can be updated in real time.

Interface Module

The interface module collects cells (from the cell-based function module) or a byte stream (from the deframer). Cells are stored in FIFO's (424 bytes or 8 cells wide, transmit buffers have the same size), from which they are extracted by the interface submodule, providing an Utopia level 2 interface.

Analog Front-End Control Interface

The Analog Front-End Interface is designed to be connected to the MTC20154 or MTC20454 Analog Front-End component Transmit Interface The 16 bit words are multiplexed on 4 AFTXD output signals. As a result 4 cycles are needed to transfer 1 word. Refer to Table 10 for the bit/pin allocation for the 4 cycles. The first of 4 cycles is identified by the CLWD signal (Fig.7). The Analog Front-End fetches the 16 bit word to be multiplexed on AFTXD from the Tx Digital Front-End module.

Table 10. Bits assigned to pins/time slot for single line interface

	Cycle 0	Cycle 1	Cycle 2	Cycle 3
AFRXD_i[0]	b0	b4	b8	b12
AFRXD_i[1]	b1	b5	b9	b13
AFRXD_i[2]	b2	b6	b10	b14
AFRXD_i[3]	b3	b7	b11	b15
GP_IN	t0	t1	t2	t3

Table 11. Bits assigned to pins/time slot for muxed-line interface

Cycles	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	line 0		line 1		line 2		line 3		line 0		line 1		line 2		line 3	
AFRXD_1[0]	b0	b4	b0	b4	b0	b4	B0	b4	b8	b12	b8	b12	b8	b12	b8	b12
AFRXD_1[1]	b1	b5	b1	b5	b1	b5	b1	b5	b9	b13	b9	b13	b9	b13	b9	b13
AFRXD_1[2]	b2	b6	b2	b6	b2	b6	b2	b6	b10	b14	b10	b14	b10	b14	b10	b14
AFRXD_1[3]	b3	b7	b3	b7	b3	b7	b3	b7	b11	b15	b11	b15	b11	b15	b11	b15

Receive Interface

The 16 bit receive word is multiplexed on 4 AFRXD input signals. As a result 4 cycles are needed to transfer 1 word. Refer to Table 11 for the bit/pin allocation for the 4 cycles. The first of 4 cycles is identified by the CLWD signal. (Fig.9). The CLWD must repeat after 4 MCLK cycles.

Figure 8. Receive word timing diagram for single line Interface

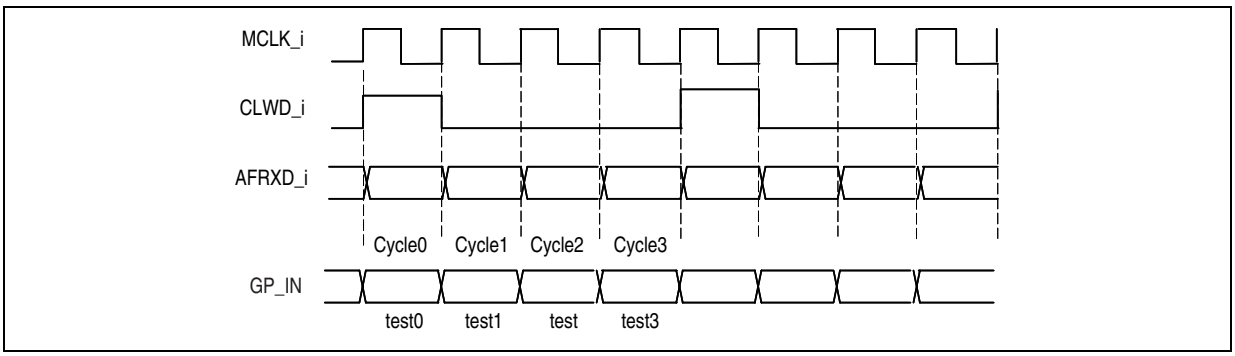


Figure 9. Receive word timing diagram for muxed line interface

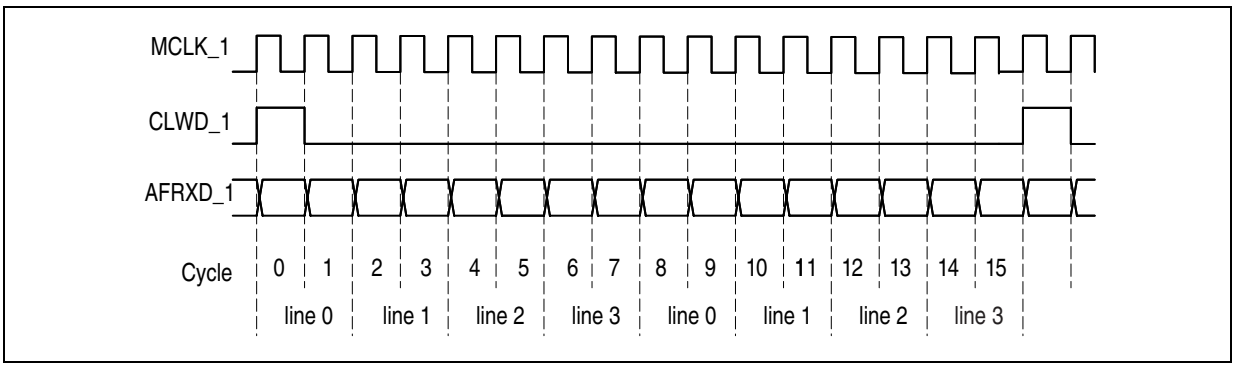


Table 12. Transmitted bits assigned to signal/time slot for single-line interface

	Cycle 0	Cycle 1	Cycle 2	Cycle 3
AFTXD_I[0]	b0	b4	b8	b12
AFTXD_I[1]	b1	b5	b9	b13
AFTXD_I[2]	b2	b6	b10	b14
AFTXD_I[3]	b3	b7	b11	b15
POWER_DOWN_i	t0	t1	t2	t3

Table 13. Transmitted bits assigned to signal/time slot for muxed-line interface

Cycles	0	1	2	3	4	5	6	7
	line 0		line 1		line 2		line 3	
AFTXD_1[0]	b0	b8	b0	b8	b0	b8	b0	b8
AFTXD_1[1]	b1	b9	b1	b9	b1	b9	b1	b9
AFTXD_1[2]	b2	b10	b2	b10	b2	b10	b2	b10
AFTXD_1[3]	b3	b11	b3	b11	b3	b11	b3	b11
AFTXD_2[0]	b4	b12	b4	b12	b4	b12	b4	b12
AFTXD_2[1]	b5	b13	b5	b13	b5	b13	b5	b13
AFTXD_2[2]	b6	b14	b6	b14	b6	b14	b6	b14
AFTXD_2[3]	b7	b15	b7	b15	b7	b15	b7	b15

Table 14. MCLK, AC Electrical Characteristics

AC Electrical Characteristics for MCLK_i						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
F	Clock Frequency			35.328		MHz
Tper	Clock Period			28.3		ns
Th	Clock duty cycle		40		60	%

Table 15. AFTXD AC Electrical Characteristics

AC Electrical Characteristics for AFTXD_i						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Tva	Data valid time	20 pF load			16	ns
Tha	Data hold time	20 pF load	4			ns

Table 16. CTRLDATA AC Electrical Characteristics

AC Electrical Characteristics for CTRLDATA_i						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Tvb	Data valid time	20 pF load			20	ns
Thb	Data hold time	20 pF load	4			ns

Figure 10. Analog front end receive interface timing diagram

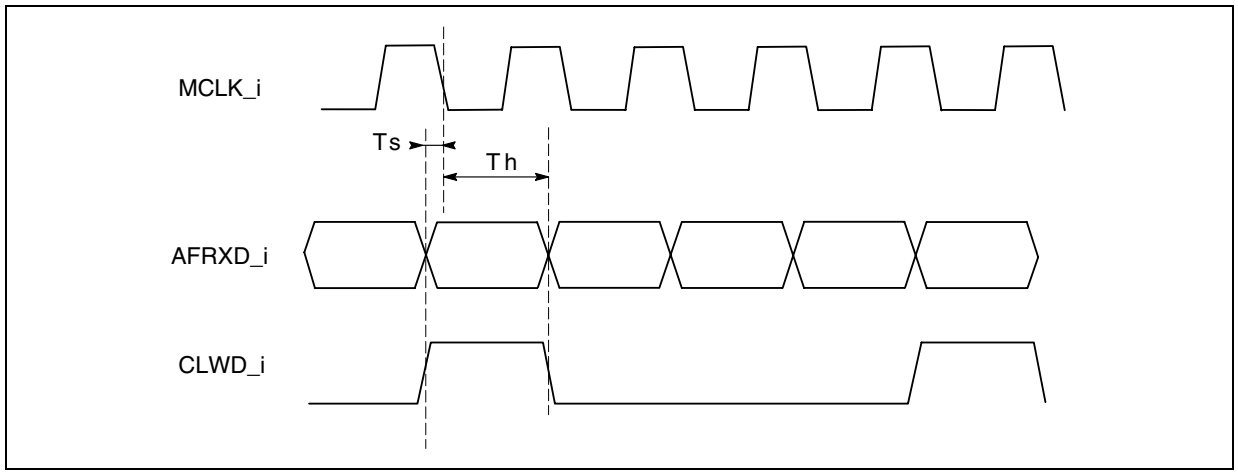


Table 17. AFRXD AC Electrical Characteristics

AC Electrical Characteristics for AFRXD						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Ts	Data setup time		5			ns
Th	Data setup time		1			ns

Digital Interface

With a Utopia Level 2 Interface the ATM forum takes the ATM layer chip as a reference. It defines the direction from ATM to physical layer as the Transmit direction. The direction from physical layer to ATM direction is referred to as the receive direction. Fig.9 shows the interconnection between ATM and PHY layer devices. Tx reference and Rx reference are supported for network timing.

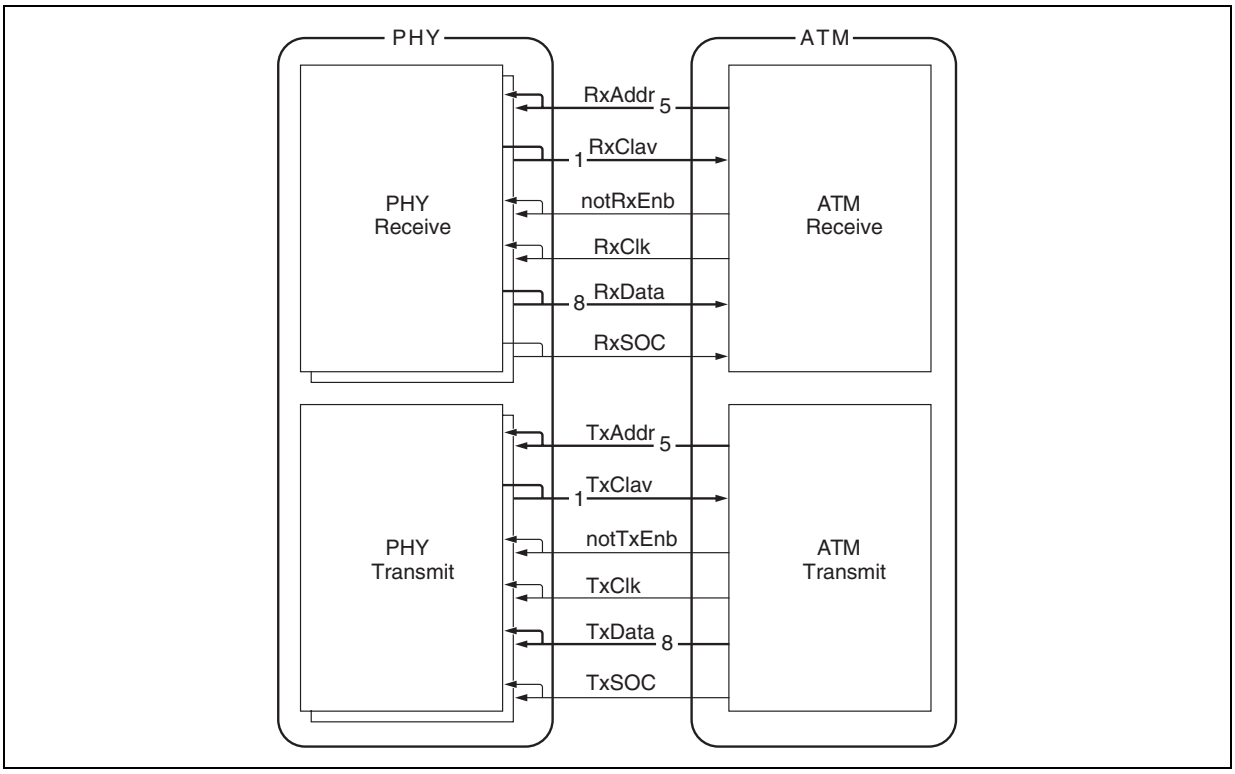
The UTOPIA interface transfers one byte in a single clock cycle, as a result cells are transferred in 53 clock cycles. Both transmit and receive interfaces are synchronised on clocks generated by the ATM layer chip, and as no specific relationship between Receive and Transmit clock is assumed, they must be regarded as mutually asynchronous clocks. Flow control signals are available to match the bandwidth constraints of the physical layer and the ATM layer.

The UTOPIA level 2 supports point to multi-point configurations by introducing an addressing capability and by making a distinction between polling and selecting a device:

– the ATM chip polls a specific physical layer chip by putting its address on the address bus when the enable (notTxEnb/notRxEnb) line is asserted. The addressed physical layer answers the next cycle via a cell available line (TxClav/RxClav) reflecting its status at that time.

– the ATM chip selects a specific physical layer chip by putting its address on the address bus when the enable line is deasserted and asserting the enable line on the next cycle. The addressed physical layer chip will be the target or source of the next cell transfer.

Figure 11. Signals at Utopia Level 2 Interface



Utopia Level 2 Signals

The physical layer chip sends cell data towards the ATM layer chip. The ATM layer chip polls the status of the FIFO of the physical layer chip. Refer to Table 6 for a list of interface signals. The cell exchange proceeds like:

a) The physical layer chip signals the availability of a cell by asserting RxClav when polled by the ATM chip.

b) The ATM chips selects a physical layer chip, then starts the transfer by asserting notRxEnb.

c) If the physical layer chip has data to send, it puts them on the RxData line the cycle after it sampled notRxEnb active. It also advances the offset in the cell. If the data transferred is the first byte of a cell, RxSOC is 1b at the time of the data transfer, 0b otherwise.

d) The ATM chip accepts the data when they are available. If RxSOC was 1b during the transfer, it resets its internal offset pointer to the value 1, otherwise it advances the offset in the cell.

MTC20455 Utopia Level 2 MPHY Operation

Utopia level 2 MPHY operation can be done by various interface schemes. The MTC20455 supports only the required mode, this mode is referred to as «operation with 1 TxClav and 1 RxClav.»

PHY Device Identification

The MTC20455 holds 2 PHY layer Utopia ports, one is dedicated to the fast data channel, the other one to the interleaved data channel. The associated PHY address is specified by the PHY_ADDR_x fields the Utopia PHY address register. Beware that an incorrect address configuration may lead to bus conflicts.

MTC20136 Transceiver Controller Interface

Table 18. All signals

Symbol	Parameter	Min	Typ	Max	Unit
tr, tf	Rise and Fall time (10% - 90%)			3	ns
Ci	Input load			10	pF
Co	Output load			20	pF

Figure 12. PCLK Clock frequency

Symbol	Parameter	Min	Typ	Max	Unit
f	PCLK clock frequency	8		33	MHz

Table 19. Address with respect to ALE

Symbol	Parameter	Min	Typ	Max	Unit
tr,tf	Rise and Fall time (10% - 90%)			4	ns
Talew	ALE pulse width	12			ns
Tavs	Address valid setup time	7			ns
Tavh	Address valid hold time	8			ns

Figure 13. Address and ALE timing diagram

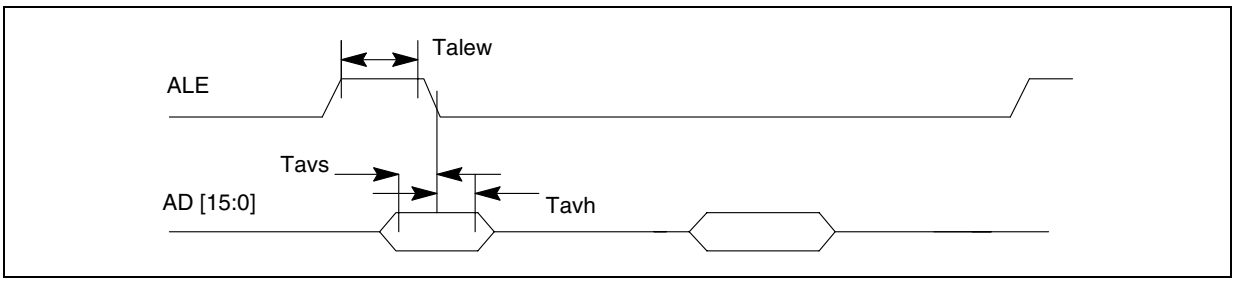


Table 20. Data input with respect to clock

Symbol	Parameter	Min	Max	Unit
Tdh	Data write hold time	3		ns
Tds	Data write setup time	10		ns

Table 21. Data output with respect to clock

Symbol	Parameter	Min	Max	Unit
Tzd	Data active delay from clock, Z to data	3	20	ns
Tdz	Data inactive delay from clock, data to Z	3	20	ns

Table 22. WR_RDB input specification with respect to PCLK

Symbol	Parameter	Min	Max	Unit
Twrs	setup WR_RDB to clock	10		ns
Twrh	hold WR_RDB to clock	3		ns

Table 23. CSB input specification with respect to PCLK

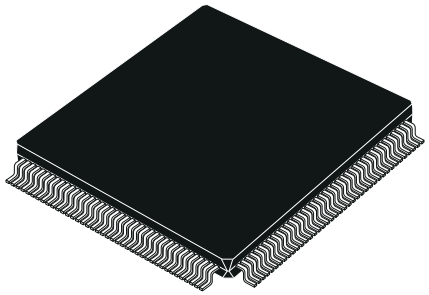
Symbol	Parameter	Min	Max	Unit
Twrs	setup CSB to clock	10		ns
Twrh	hold CSB to clock	3		ns

Table 24. RDYB output with respect to PCLK

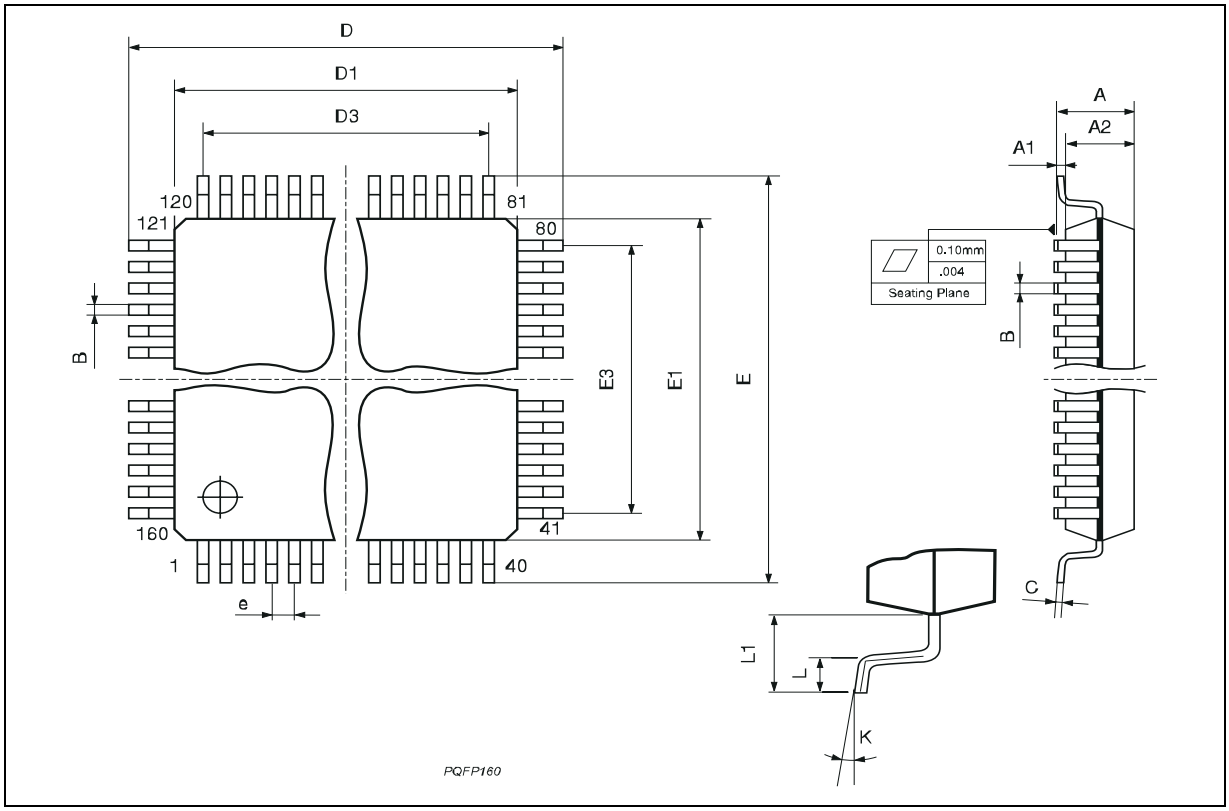
Symbol	Parameter	Min	Max	Unit
Tzrd	RDYB active delay from clock, Z to 0	3	19	ns
Trdz	RDYB inactive delay from clock, 0 to Z	3	19	ns

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.07			0.160
A1	0.25			0.010		
A2	3.17	3.42	3.67	0.125	0.135	0.144
B	0.22		0.38	0.009		0.015
C	0.13		0.23	0.005		0.009
D	30.95	31.20	31.45	1.219	1.228	1.238
D1	27.90	28.00	28.10	1.098	1.102	1.106
D3		25.35			0.998	
e		0.65			0.026	
E	30.95	31.20	31.45	1.219	1.228	1.238
E1	27.90	28.00	28.10	1.098	1.102	1.106
E3		25.35			0.998	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA

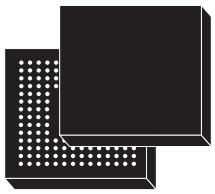


PQFP160



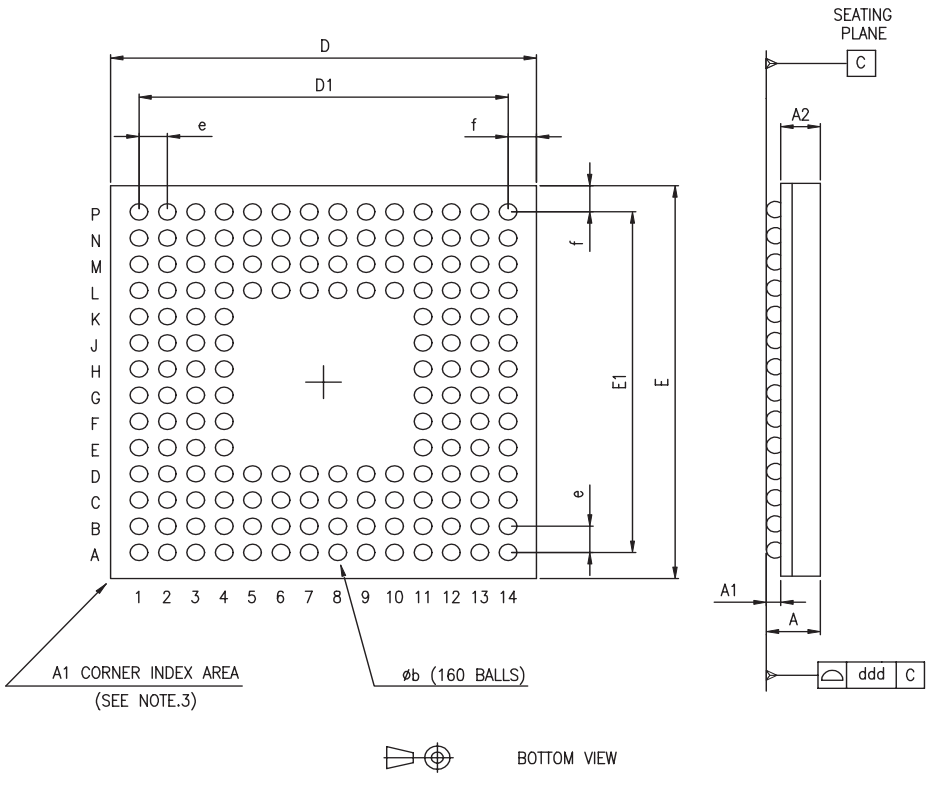
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.210		1.700	0.047		0.067
A1	0.270			0.010		
A2		1.120			0.044	
b	0.450	0.500	0.550	0.018	0.02	0.021
D	11.85	12.00	12.15	0.466	0.472	0.478
D1		10.40			0.409	
E	11.85	12.00	12.15	0.466	0.472	0.478
E1		10.40			0.409	
e	0.720	0.800	0.880	0.028	0.031	0.034
f	0.650	0.800	0.950	0.025	0.031	0.037
ddd			0.120			0.004

OUTLINE AND MECHANICAL DATA



Body: 12 x 12 x 1.7mm

LFBGA160
Low Profile **F**ine Pitch **B**all **G**rid **A**rray



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