

4Mb Ultra-Low Power Asynchronous CMOS SRAM w/ Dual Vcc and VccQ for Ultimate Power Reduction

256K×16 bit POWER SAVER TECHNOLOGY

Overview

The N04Q1618C2B are ultra-low power memory devices containing a 4 Mbit Static Random Access Memory organized as 262,144 words by 16 bits. The device is designed and fabricated using AMI Semiconductor's advanced CMOS technology to provide ultra-low active and standby power. The device operates with two chip enable ($\overline{CE1}$ and $CE2$) controls and output enable (\overline{OE}) to allow for easy memory expansion. Byte controls (\overline{UB} and LB) allow the upper and lower bytes to be accessed independently. The 4Mb SRAM is optimized for the ultimate in low power and is suited for various applications where ultra-low-power is critical such as medical applications, battery backup and power sensitive hand-held devices. The unique page mode operation saves active operating power and the dual power supply rails allow very low voltage operation while maintaining 3V I/O capability. The device can operate over a very wide temperature range of 0°C to +70°C for the lowest power and is also available in the industrial range of -40°C to +85°C. The devices are available in standard BGA and TSOP packages. The devices are also available as Known Good Die (KGD) for embedded package applications.

Product Options

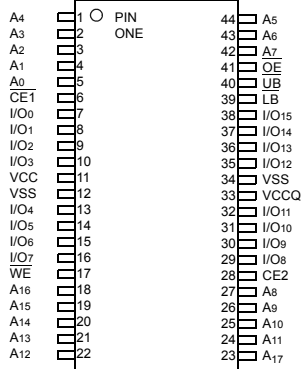
| Part Number | Typical Standby Current | Vcc (V) | VccQ (V) | Speed (nS) | Typical Operating Current | Operating Temperature |
|-------------------------------|-------------------------|---------|---------------|------------|---------------------------|-----------------------|
| N04Q1612C2Bx-15C ¹ | 50nA | 1.2 | 1.2, 1.8, 3.0 | 150ns | 0.4 mA @ 1MHz | 0°C to +70°C |
| N04Q1618C2Bx-15C ¹ | 50nA | 1.8 | 1.8, 3.0 | 150ns | 0.4 mA @ 1MHz | |
| N04Q1618C2Bx-70C | 200nA | | | 70ns | 0.6 mA @ 1MHz | |
| N04Q1618C2Bx-85C | 200nA | | | 85ns | 0.6 mA @ 1MHz | |

1. Part numbers are under development. Please contact your local sales representative for details.

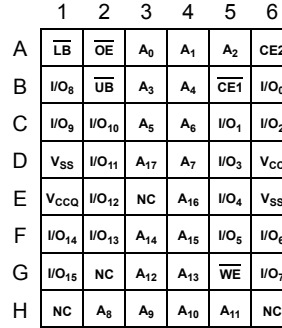
Features

- **Multiple Power Supply Ranges**
1.1V - 1.3V
1.65V - 1.95V
- **Dual Vcc / VccQ Power Supplies**
1.2V Vcc with 3V VccQ
1.8V Vcc with 3V VccQ
- **Very low standby current**
50nA typical for 1.2V operation
- **Very low operating current**
400µA typical for 1.2V operation at 1µs
- **Very low Page Mode operating current**
80µA typical for 1.2V operation at 1µs
- **Simple memory control**
Dual Chip Enables ($\overline{CE1}$ and $CE2$)
Byte control for independent byte operation
Output Enable (\overline{OE}) for memory expansion
- **Automatic power down to standby mode**
- **BGA, TSOP and KGD options**
- **RoHS Compliant**

Pin Configurations (4Mb)



TSOP II

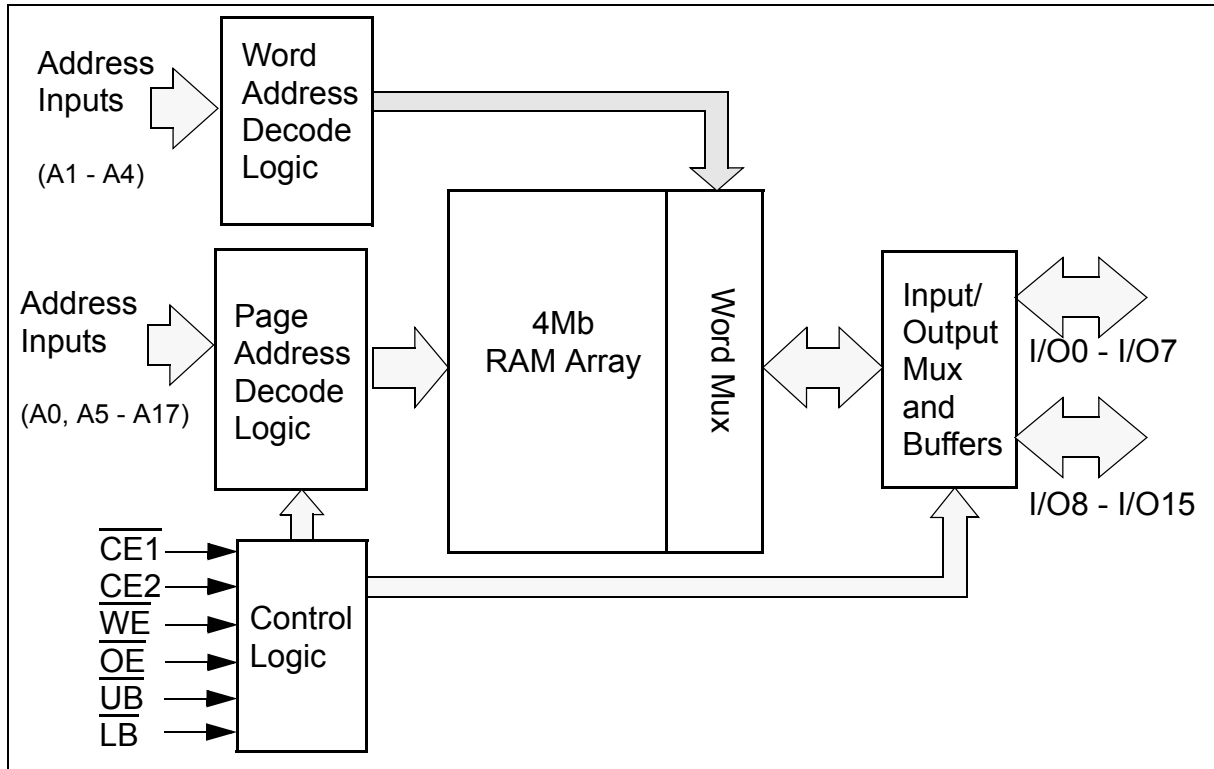


48 Pin BGA (top)

Pin Descriptions

| Pin Name | Pin Function |
|-------------------------------------|------------------------------|
| A ₀ -A ₁₇ | Address Inputs |
| \overline{WE} | Write Enable Input |
| $\overline{CE1}$ | Chip Enable 1 Input |
| $\overline{CE2}$ | Chip Enable 2 Input |
| \overline{OE} | Output Enable Input |
| \overline{LB} | Lower Byte Enable Input |
| \overline{UB} | Upper Byte Enable Input |
| I/O ₀ -I/O ₇ | Lower Byte Data Input/Output |
| I/O ₈ -I/O ₁₅ | Upper Byte Data Input/Output |
| V _{CC} | Core Power |
| V _{CCQ} | Power for I/O |
| V _{SS} | Core Ground |
| NC | Not Connected |

Functional Block Diagram



Functional Description

| $\overline{CE1}$ | $\overline{CE2}$ | \overline{WE} | \overline{OE} | \overline{UB}^1 | \overline{LB}^1 | $I/O_0 - I/O_{15}^1$ | MODE | POWER |
|------------------|------------------|-----------------|-----------------|-------------------|-------------------|----------------------|----------------------|---------|
| H | X | X | X | X | X | High Z | Standby ² | Standby |
| X | L | X | X | X | X | High Z | Standby ² | Standby |
| L | H | X | X | H | H | High Z | Standby | Standby |
| L | H | L | X ³ | L ¹ | L ¹ | Data In | Write ³ | Active |
| L | H | H | L | L ¹ | L ¹ | Data Out | Read | Active |
| L | H | H | H | L ¹ | L ¹ | High Z | Active | Active |

1. When \overline{UB} and \overline{LB} are in select mode (low), $I/O_0 - I/O_{15}$ are affected as shown. When \overline{LB} only is in the select mode only $I/O_0 - I/O_7$ are affected as shown. When \overline{UB} is in the select mode only $I/O_8 - I/O_{15}$ are affected as shown.

2. When the device is in standby mode, control inputs (\overline{WE} , \overline{OE} , \overline{UB} , and \overline{LB}), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.

3. When \overline{WE} is invoked, the \overline{OE} input is internally disabled and has no effect on the circuit.

Capacitance¹

| Item | Symbol | Test Condition | Min | Max | Unit |
|-------------------|-----------|--|-----|-----|------|
| Input Capacitance | C_{IN} | $V_{IN} = 0V, f = 1 \text{ MHz}, T_A = 25^\circ\text{C}$ | | 8 | pF |
| I/O Capacitance | $C_{I/O}$ | $V_{IN} = 0V, f = 1 \text{ MHz}, T_A = 25^\circ\text{C}$ | | 8 | pF |

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings¹

| Item | Symbol | Rating | Unit |
|---|--------------|----------------------|------|
| Voltage on any pin relative to V_{SS} | $V_{IN,OUT}$ | -0.3 to $V_{CC}+0.3$ | V |
| Voltage on V_{CC} Supply Relative to V_{SS} | V_{CC} | -0.3 to 4 | V |
| Power Dissipation | P_D | 500 | mW |
| Storage Temperature | T_{STG} | -40 to 125 | °C |
| Operating Temperature | T_A | -40 to +85 | °C |
| Soldering Temperature and Time | T_{SOLDER} | 260°C, 10sec | °C |

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range, 0° - 70° C)

| Item | Symbol | Device | Conditions | Min. | Typ | Max | Unit |
|------------------------|-----------|-------------|---|-----------------|-----|-----------------|---------|
| Core Supply Voltage | V_{CC} | N04Q1612... | 1.2V Core Device | 1.1 | 1.2 | 1.3 | V |
| | | N04Q1618... | 1.8V Core Device | 1.65 | 1.8 | 1.95 | |
| I/O Supply Voltage | V_{CCQ} | N04Q1612... | 1.2V Core Device | 1.1 | | 3.3 | V |
| | | N04Q1618... | 1.8V Core Device | 1.65 | | 3.3 | |
| Input High Voltage | V_{IH} | | | 0.8 x V_{CCQ} | | $V_{CC}+0.3$ | V |
| Input Low Voltage | V_{IL} | | | -0.3 | | 0.2 x V_{CCQ} | |
| Output High Voltage | V_{OH} | | $I_{OH} = -100\mu A$ | $V_{CC}-0.2$ | | | V |
| Output Low Voltage | V_{OL} | | $I_{OL} = 100\mu A$ | | | 0.2 | V |
| Input Leakage Current | I_{LI} | | $V_{IN} = 0$ to V_{CC} | | | 0.5 | μA |
| Output Leakage Current | I_{LO} | | $\overline{OE} = V_{IH}$ or Chip Disabled | | | 0.5 | μA |

Power Consumption ($T_A = 0^\circ\text{C} - 70^\circ\text{C}$)

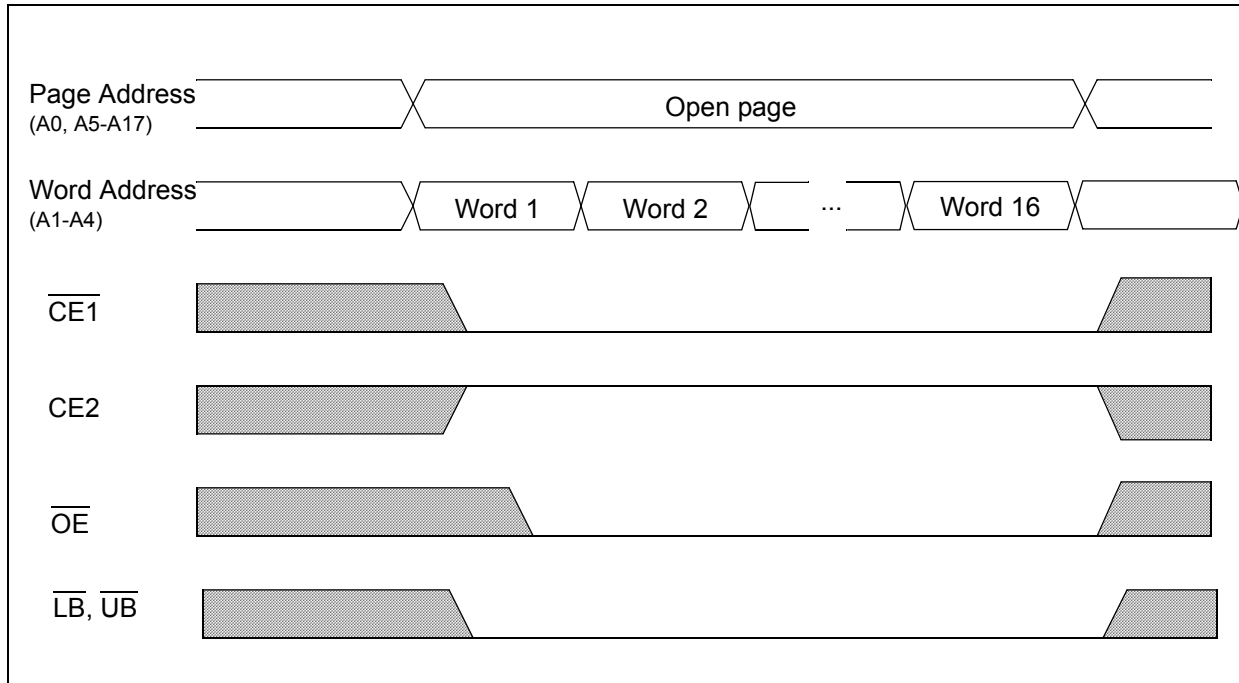
| Device PN | | | | Speed | Typ ¹ | Max | |
|----------------------|---------------------------------|------------------|--|--------------|------------------|-----|----|
| N04Q1612C2Bx-15C | Standby Current ² | I _{sb} | Chip Disabled V _{CC} = 1.3V, V _{IN} = V _{CC} or 0 | | 50 | 500 | nA |
| | | | | | | | |
| | Read/Write Current ³ | I _{cc} | Chip Enabled, I _{OUT} = 0 V _{CC} =1.3V, V _{IN} =V _{IH} or V _{IL} | 1us | 0.4 | 0.5 | mA |
| | | | | 150ns | 2 | 3 | |
| | Page Mode Current | I _{ccp} | Chip Enabled, I _{OUT} = 0 V _{CC} =1.3V, V _{IN} =V _{IH} or V _{IL} | 1us | 80 | 100 | μA |
| | | | | 150ns | 300 | 450 | |
| N04Q1618C2Bx-15C | Standby Current | I _{sb} | Chip Disabled V _{CC} = 1.9V, V _{IN} = V _{CC} or 0V | | 50 | 500 | nA |
| | | | | | | | |
| | Read/Write Current | I _{cc} | Chip Enabled, I _{OUT} = 0 V _{CC} =1.9V, V _{IN} =V _{IH} or V _{IL} | 1us | 0.4 | 0.5 | mA |
| | | | | 150ns | 2 | 3 | |
| | Page Mode Current | I _{ccp} | Chip Enabled, I _{OUT} = 0 V _{CC} =1.9V, V _{IN} =V _{IH} or V _{IL} | 1us | 80 | 100 | μA |
| | | | | 150ns | 400 | 500 | |
| N04Q1618C2Bx-70C/85C | Standby Current | I _{sb} | Chip Disabled V _{CC} = 1.9V, V _{IN} = V _{CC} or 0 | | 0.2 | 1.5 | μA |
| | | | | | | | |
| | Read/Write Current | I _{cc} | Chip Enabled, I _{OUT} = 0 V _{CC} =1.9V, V _{IN} =V _{IH} or V _{IL} | 1us | 0.6 | 0.9 | mA |
| | | | | 70ns 85ns | 6 | 7 | |
| | Page Mode Current | I _{ccp} | Chip Enabled, I _{OUT} = 0 V _{CC} =1.9V, V _{IN} =V _{IH} or V _{IL} | 1us | 0.1 | 0.2 | mA |
| | | | | 70ns 85ns | 0.8 | 1 | |

1. Typical values are measured at V_{cc}=V_{cc} Typ., T_A=25°C and not 100% tested.

2. This device assumes a standby mode if the chip is disabled ($\overline{\text{CE}}1$ high or CE2 low). In order to achieve low standby current all inputs must be within 0.2 volts of either V_{CC} or V_{SS}. This applies to all I_{SB} values.

3. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system. This applies to all I_{CC} and I_{CCP} values.

Power Savings with Page Mode Operation ($\overline{WE} = V_{IH}$)



Note: Page mode operation is a method of addressing the SRAM to save operating current. The internal organization of the SRAM is optimized to allow this unique operating mode to be used as a valuable power saving feature.

The only thing that needs to be done is to address the SRAM in a manner that the internal page is left open and 16-bit words of data are read from the open page. By treating addresses A1 - A4 as the least significant bits and addressing the 16 words within the open page, power is reduced to the page mode value which is considerably lower than standard operating currents for low power SRAMs.

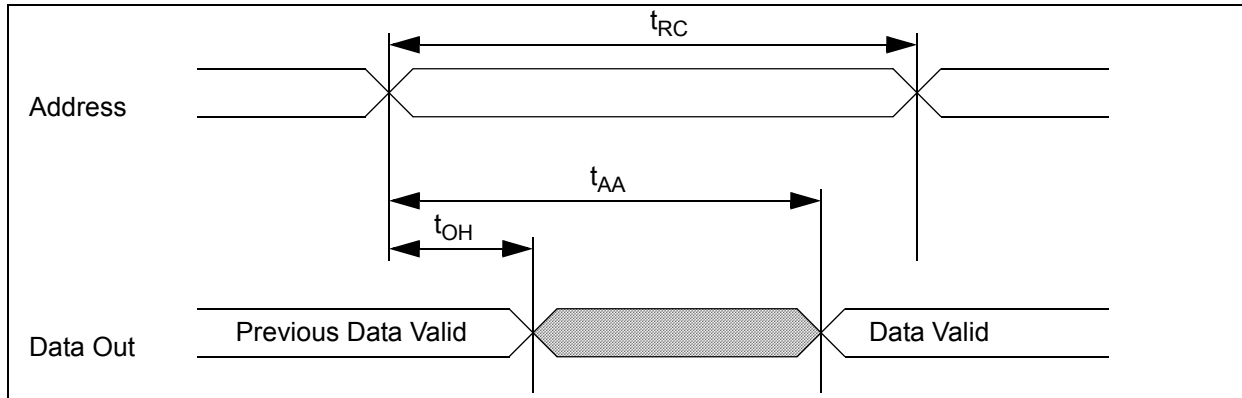
Timing Test Conditions

| Item | |
|--|---|
| Input Pulse Level | 0.1V _{CC} to 0.9 V _{CC} |
| Input Rise and Fall Time | 5ns |
| Input and Output Timing Reference Levels | 0.5 V _{CC} |
| Output Load | CL = 30pF |
| Operating Temperature | 0 to +70°C |

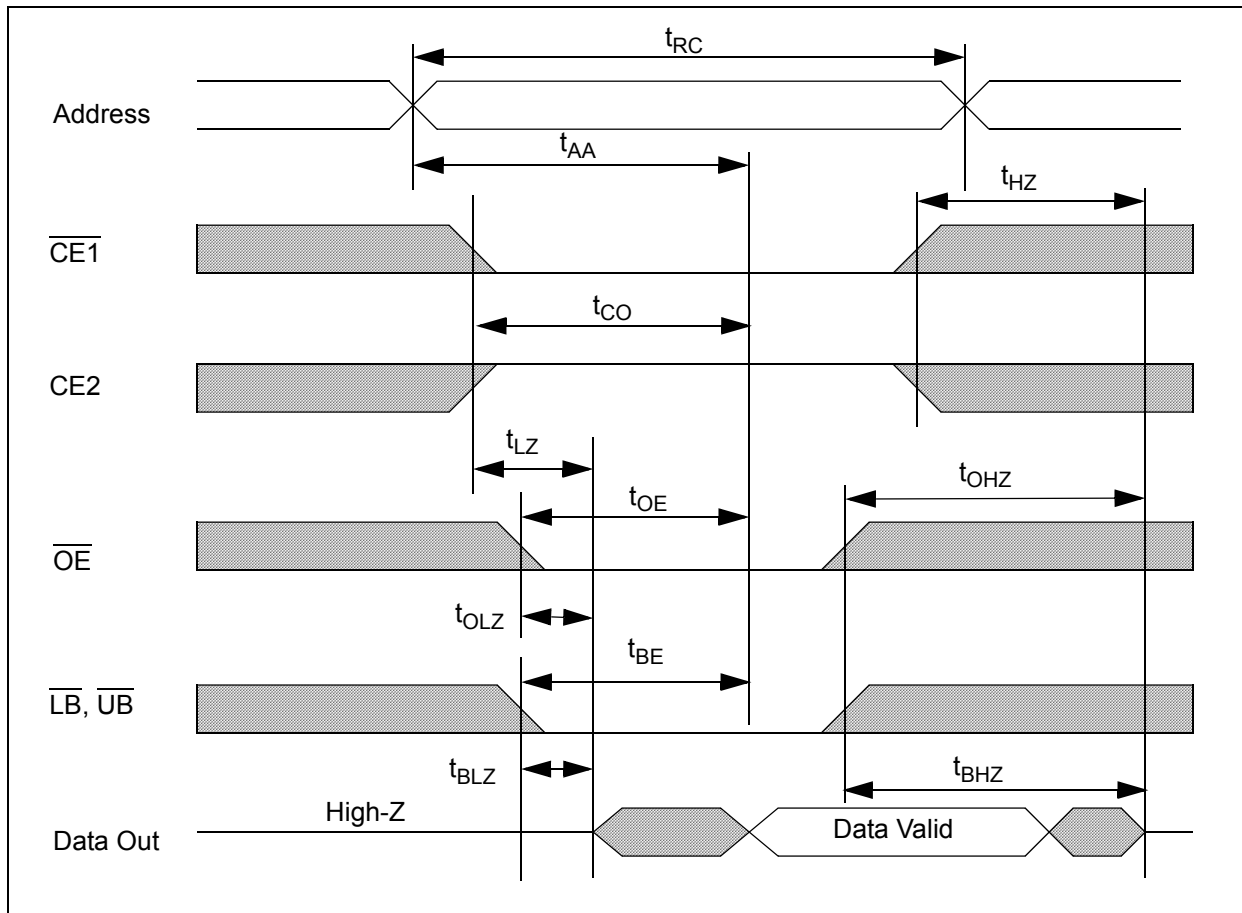
Timing

| Item | Symbol | -70 | | -85 | | -150 | | Units |
|--------------------------------------|------------------|------|------|------|------|------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle Time | t _{RC} | 70 | | 85 | | 150 | | ns |
| Address Access Time | t _{AA} | | 70 | | 85 | | 150 | ns |
| Page Mode Address Access Time | t _{AAP} | | 70 | | 85 | | 150 | ns |
| Chip Enable to Valid Output | t _{CO} | | 70 | | 85 | | 150 | ns |
| Output Enable to Valid Output | t _{OE} | | 35 | | 45 | | 75 | ns |
| Byte Select to Valid Output | t _{BE} | | 70 | | 85 | | 150 | ns |
| Chip Enable to Low-Z output | t _{LZ} | 10 | | 10 | | 10 | | ns |
| Output Enable to Low-Z Output | t _{OLZ} | 5 | | 5 | | 5 | | ns |
| Byte Select to Low-Z Output | t _{BZ} | 10 | | 10 | | 10 | | ns |
| Chip Disable to High-Z Output | t _{HZ} | 0 | 20 | 0 | 20 | 0 | 20 | ns |
| Output Disable to High-Z Output | t _{OZH} | 0 | 20 | 0 | 20 | 0 | 20 | ns |
| Byte Select Disable to High-Z Output | t _{BHZ} | 0 | 20 | 0 | 20 | 0 | 20 | ns |
| Output Hold from Address Change | t _{OH} | 10 | | 10 | | 10 | | ns |
| Write Cycle Time | t _{WC} | 70 | | 85 | | 150 | | ns |
| Chip Enable to End of Write | t _{CW} | 50 | | 60 | | 120 | | ns |
| Address Valid to End of Write | t _{AW} | 50 | | 60 | | 120 | | ns |
| Byte Select to End of Write | t _{BW} | 50 | | 60 | | 120 | | ns |
| Write Pulse Width | t _{WP} | 40 | | 50 | | 100 | | ns |
| Address Setup Time | t _{AS} | 0 | | 0 | | 0 | | ns |
| Write Recovery Time | t _{WR} | 0 | | 0 | | 0 | | ns |
| Write to High-Z Output | t _{WHZ} | | 20 | | 20 | | 20 | ns |
| Data to Write Time Overlap | t _{DW} | 40 | | 50 | | 100 | | ns |
| Data Hold from Write Time | t _{DH} | 0 | | 0 | | 0 | | ns |
| End Write to Low-Z Output | t _{OW} | 5 | | 5 | | 5 | | ns |

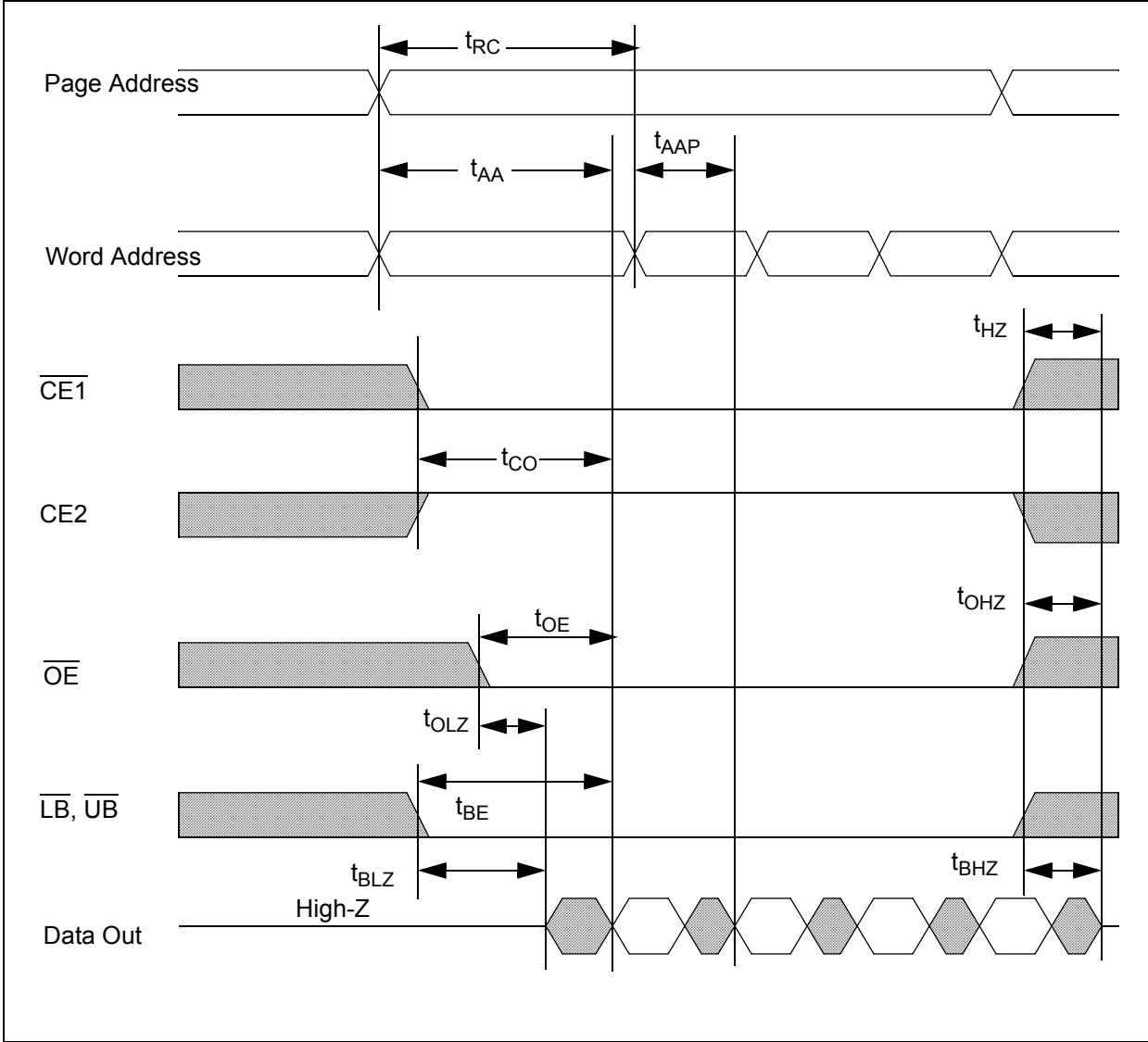
Timing of Read Cycle ($\overline{CE1} = \overline{OE} = V_{IL}, \overline{WE} = CE2 = V_{IH}$)



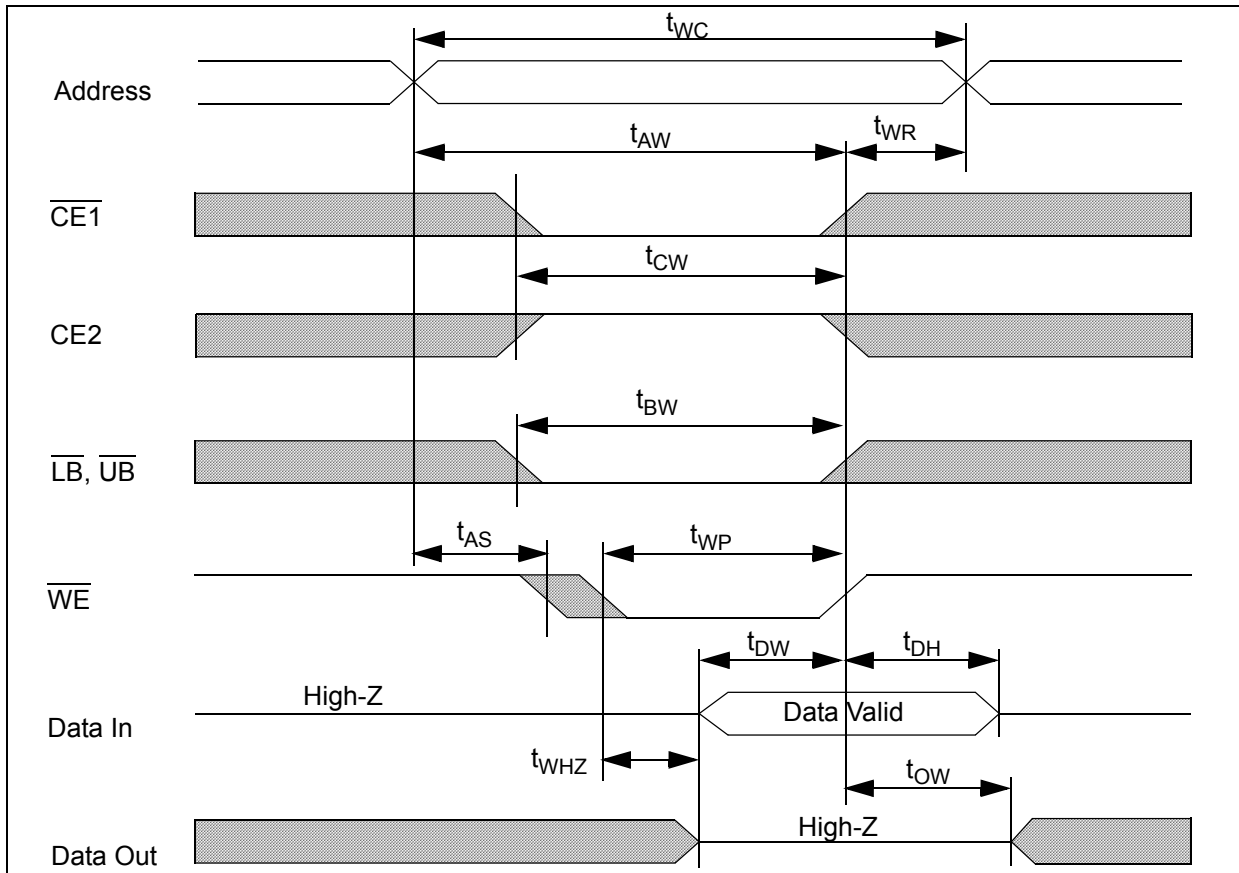
Timing Waveform of Read Cycle ($\overline{WE} = V_{IH}$)



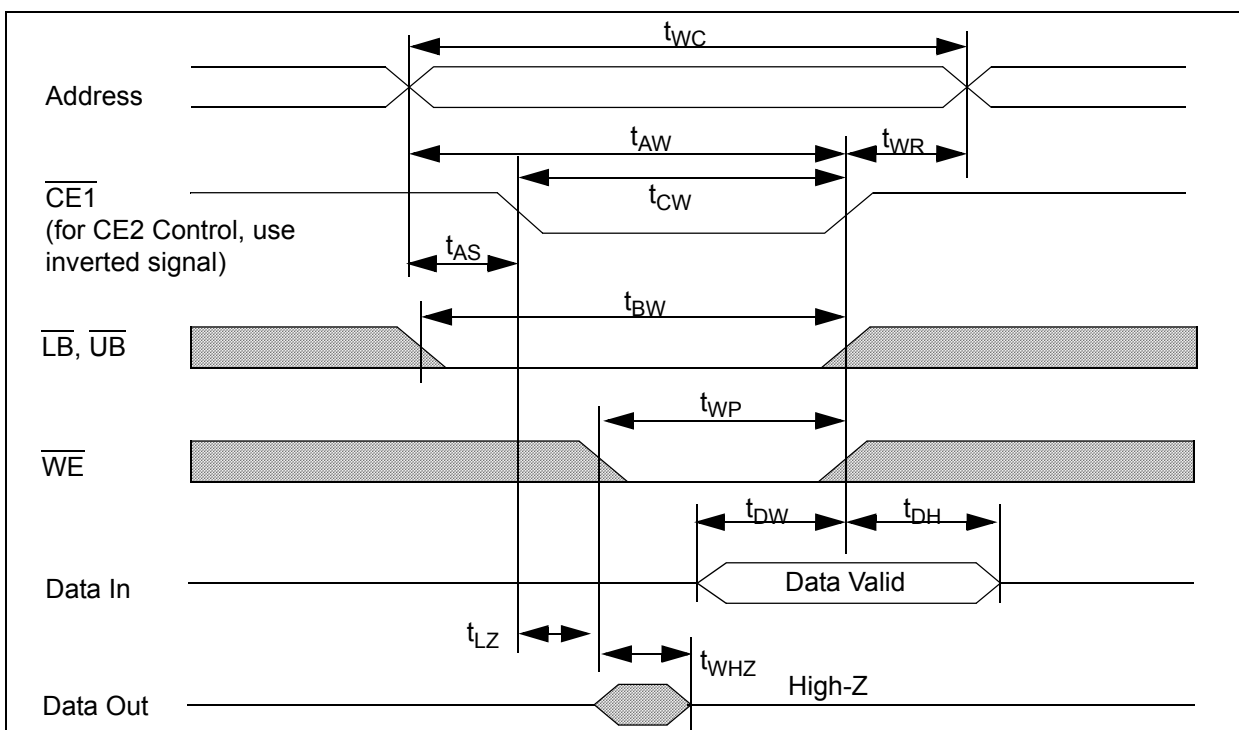
Timing Waveform of Page Mode Read Cycle ($\overline{WE} = V_{IH}$)



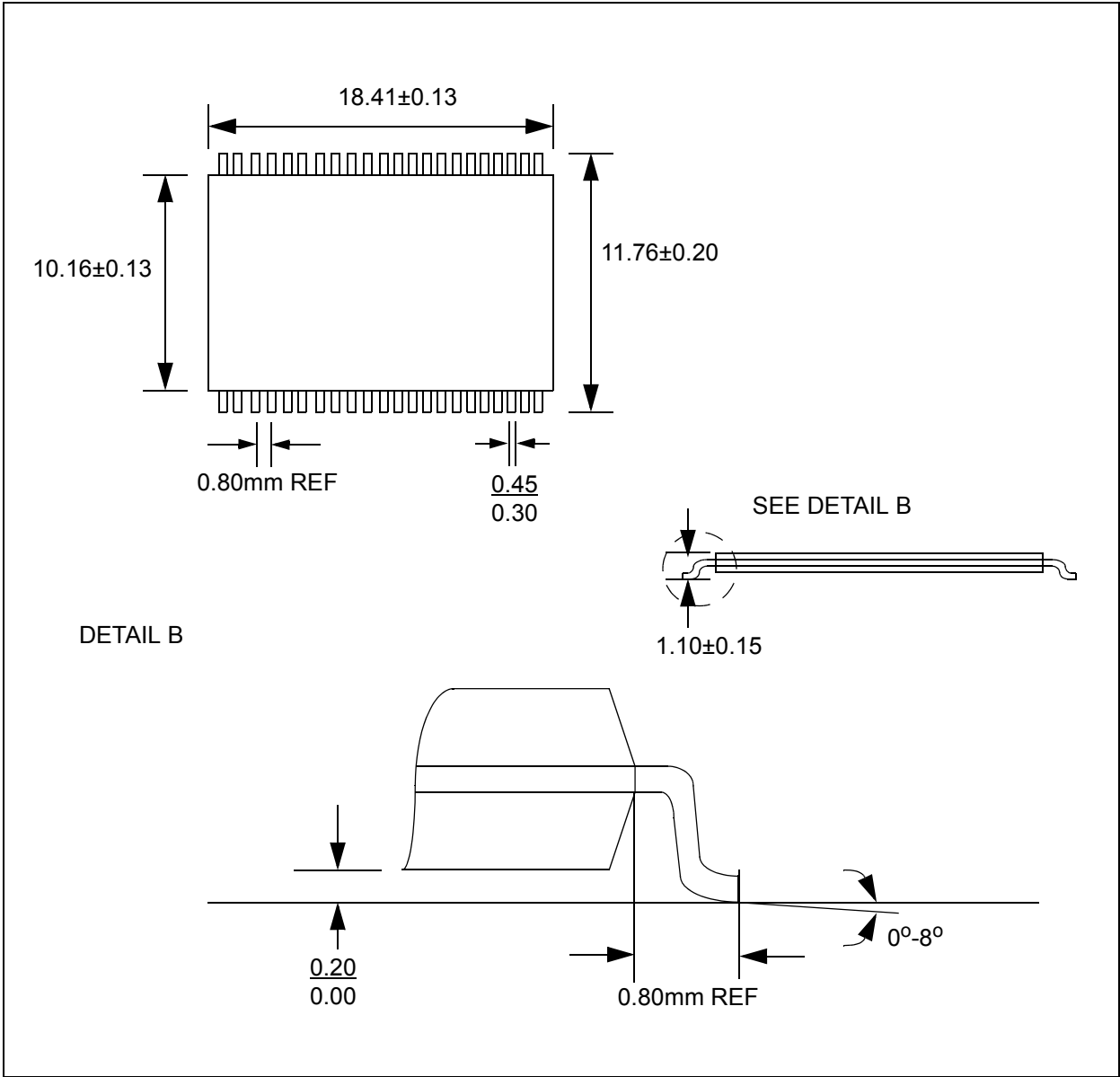
Timing Waveform of Write Cycle (\overline{WE} control)



Timing Waveform of Write Cycle ($\overline{CE1}$ Control)

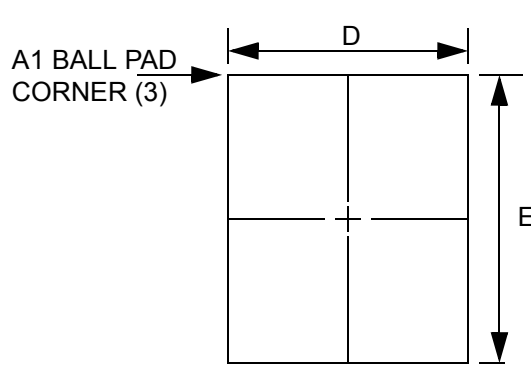


44-Lead TSOP II Package (T44)

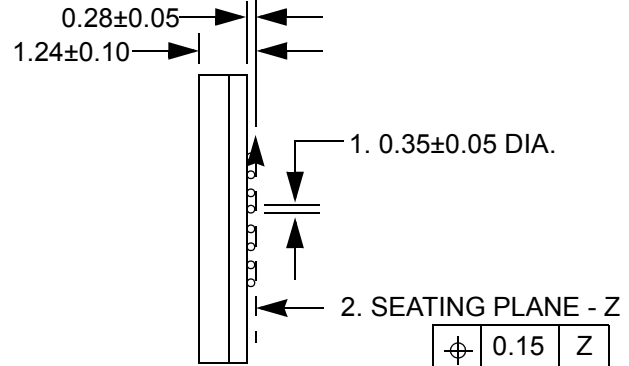


- Note:
1. All dimensions in inches (Millimeters)
 2. Package dimensions exclude molding flash

Ball Grid Array Package

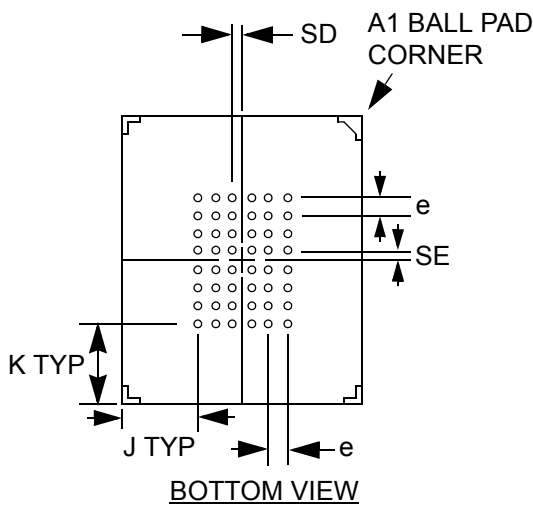


TOP VIEW



SIDE VIEW

| | | |
|---|------|---|
| ∅ | 0.15 | Z |
| ∅ | 0.05 | Z |



BOTTOM VIEW

1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

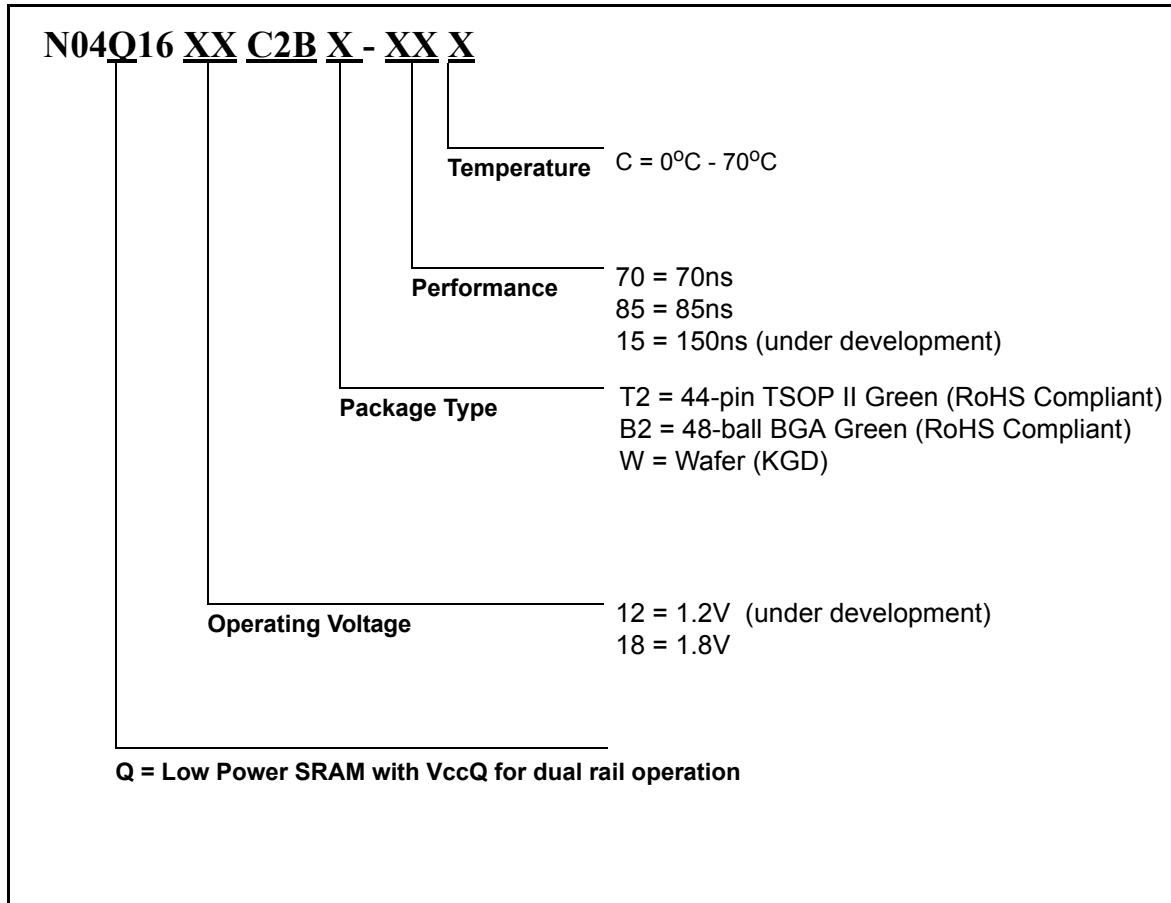
2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

Dimensions (mm)

| D | E | e = 0.75 | | | | BALL MATRIX TYPE |
|--------|--------|----------|-------|-------|-------|------------------|
| | | SD | SE | J | K | |
| 6±0.10 | 8±0.10 | 0.375 | 0.375 | 1.125 | 1.375 | FULL |

Ordering Information



Revision History

| Revision | Date | Change Description |
|----------|----------------|--|
| A | October 2005 | Initial Advanced Release |
| B | February 2006 | Raised maximum Vcc to 3.6V for 3V device Added green packages Changed dual rail to 'Q' part designator |
| C | July 2006 | Separated 1.8V dual rail and 3V single rail Updated VccQ for TSOP |
| D | September 2006 | Converted to AMI Semiconductor |

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