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8Mb Ultra-Low Power Asynchronous CMOS SRAM

1024K × 8 bit

Overview

The N08L083WC2C is an integrated memory device containing a 8 Mbit Static Random Access Memory organized as 1,048,576 words by 8 bits. The device is designed and fabricated using NanoAmp's advanced CMOS technology to provide both high-speed performance and ultra-low power. The device operates with two chip enable ($\overline{CE1}$ and CE2) controls and output enable ($\overline{OE}$) to allow for easy memory expansion. The N08L083WC2C is optimal for various applications where low-power is critical such as battery backup and hand-held devices. The device can operate over a very wide temperature range of -40^{o}C to +85^{o}C and is available in JEDEC standard packages compatible with other standard 512Kb x 16 SRAMs

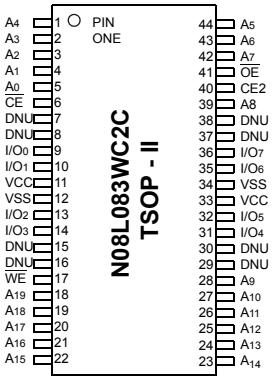
Features

- **Single Wide Power Supply Range**
  2.2 to 3.6 Volts
- **Very low standby current**
  2.0µA at 3.0V (Typical)
- **Very low operating current**
  1.5mA at 3.0V and 1µs(Typical)
- **Simple memory control**
  Dual Chip Enables ($\overline{CE1}$ and CE2)
  Byte control for independent byte operation
  Output Enable ($\overline{OE}$) for memory expansion
- **Low voltage data retention**
  Vcc = 1.5V
- **Very fast output enable access time**
  25ns $\overline{OE}$ access time
- **Automatic power down to standby mode**
- **TTL compatible three-state output driver**
- **Ultra Low Power Sort Available**

Product Family

Part Number	Package Type	Operating Temperature	Power Supply (Vcc)	Speed	Standby Current (I_{SB}), Typical	Operating Current (Icc), Typical
N08L083WC2CT1	44 TSOP II Pb Free	-40^{o}C to +85^{o}C	2.2V - 3.6V	55ns	2 µA	1.5 mA @ 1MHz

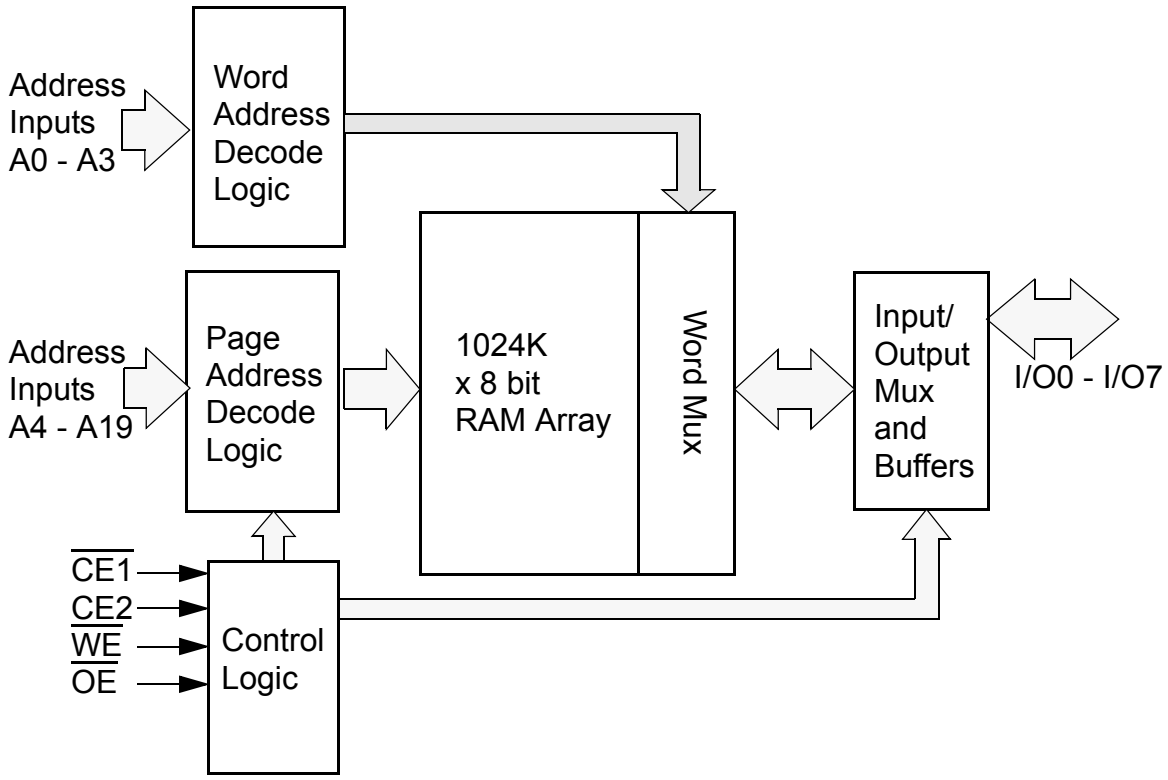
Pin Configuration



Pin Descriptions

Pin Name	Pin Function
A_0-A_{19}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE1}$, CE2	Chip Enable Input
$\overline{OE}$	Output Enable Input
I/O_0-I/O_7	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground
NC	Not Connected

Functional Block Diagram



Functional Description

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	I/O_0 - I/O_7	MODE	POWER
H	X	X	X	High Z	Standby	Standby
X	L	X	X	High Z	Standby	Standby
L	H	L	X[1]	Data In	Write[3]	Active
L	H	H	L	Data Out	Read	Active
L	H	H	H	High Z	Active	Active

1. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.

Capacitance[1]

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		10	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		10	pF

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–65 to 150	°C
Operating Temperature	T_A	-40 to +85	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10sec	°C

Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

Item	Symbol	Test Conditions		Min.	Typ[1]	Max	Unit
Supply Voltage	V_{CC}			2.2	3.0	3.6	V
Data Retention Voltage	V_{DR}	Chip Disabled		1.5			V
Input High Voltage	V_{IH}	Vcc = 2.2V to 2.7V		1.8		V_{CC}+0.3	V
		Vcc = 2.7V to 3.6V		2.2		V_{CC}+0.3	
Input Low Voltage	V_{IL}	Vcc = 2.2V to 2.7V		-0.3		0.6	V
		Vcc = 2.7V to 3.6V		-0.3		0.8	
Output High Voltage	V_{OH}	I_{OH} = -0.1mA, Vcc = 2.2V		2.0			V
		I_{OH} = -1.0mA, Vcc = 2.7V		2.4			
Output Low Voltage	V_{OL}	I_{OL} = 0.1mA, Vcc = 2.2V				0.4	V
		I_{OL} = 2.1mA, Vcc = 2.7V				0.4	
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}		-1		1	µA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to V_{CC} Output Disabled		-1		1	µA
Read/Write Operating Supply Current @ 1 µs Cycle Time[2]	I_{CC1}	V_{CC}=3.6 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0			1.5	3.0	mA
			-L		1.5	3.0	
Read/Write Operating Supply Current @ fmax	I_{CC2}	V_{CC}=3.6 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0			12.0	20.0	mA
			-L		12.0	15.0	
Maximum Standby Current	I_{SB1}	V_{IN} = V_{CC} or 0V Chip Disabled t_A= 85°C, V_{CC} = 3.6 V			2.0	20	µA
			-L		2.0	8	
Maximum Data Retention Current	I_{DR}	Vcc = 1.5V, CE ≥ Vcc - 0.2V, VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V				10	µA
			-L			4	

1. Typical values are measured at Vcc=Vcc Typ., T_A=25°C and not 100% tested.

2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to 0.9 V_{CC}
Input Rise and Fall Time	1V/ns
Input and Output Timing Reference Levels	0.5 V_{CC}
Output Load	CL = 30pF/50pF
Operating Temperature	-40 to +85 ^{O}C

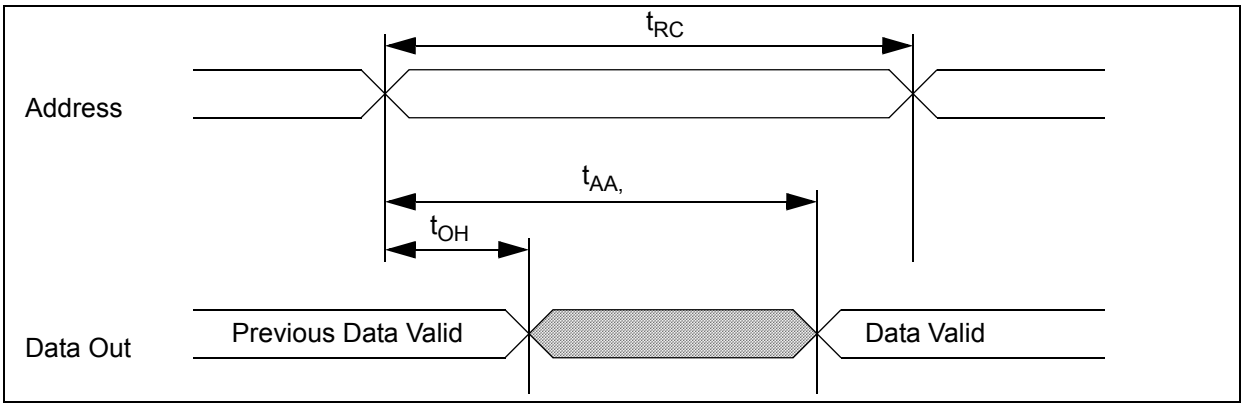
Timing

Item	Symbol	55		Units
		Min	Max	
Read Cycle Time	t_{RC}	55		ns
Address Access Time (Random Access)	t_{AA}		55	ns
Chip Enable to Valid Output	t_{CO}		55	ns
Output Enable to Valid Output	t_{OE}		25	ns
Chip Enable to Low-Z output	t_{LZ}	10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		ns
Chip Disable to High-Z Output	t_{HZ}		20	ns
Output Disable to High-Z Output	t_{OHZ}		20	ns
Output Hold from Address Change	t_{OH}	10		ns
Write Cycle Time	t_{WC}	55		ns
Chip Enable to End of Write	t_{CW}	40		ns
Address Valid to End of Write	t_{AW}	40		ns
Write Pulse Width	t_{WP}	40		ns
Address Setup Time	t_{AS}	0		ns
Write Recovery Time	t_{WR}	0		ns
Write to High-Z Output	t_{WHZ}		20	ns
Data to Write Time Overlap	t_{DW}	25		ns
Data Hold from Write Time	t_{DH}	0		ns
End Write to Low-Z Output	t_{OW}	10		ns

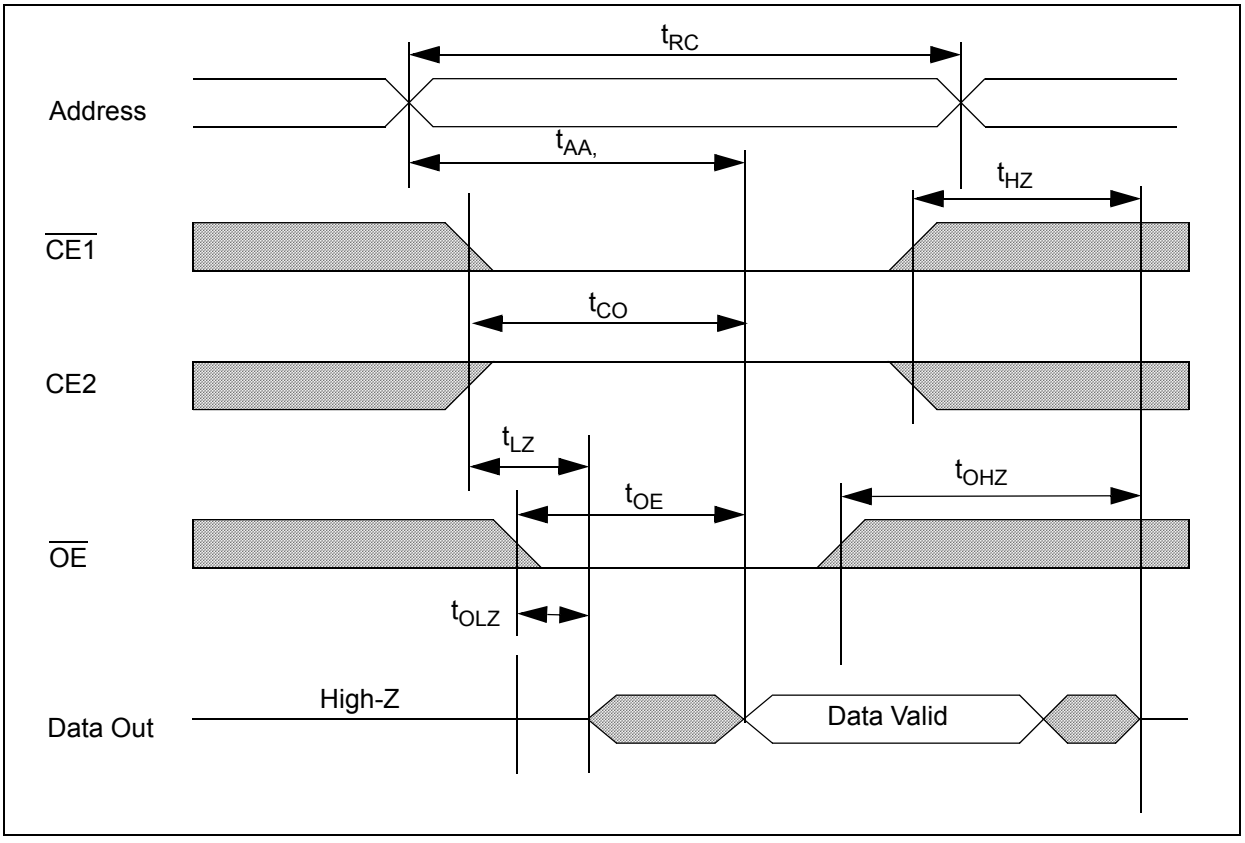
Note:

1. Full device AC operation assumes a 100us ramp time from 0 to Vcc(min) and 200µs wait time after Vcc stablization.
2. Full device operation requires linear Vcc ramp from V_{DR} to Vcc(min) ≥ 100us or stable at Vcc(min) ≥ 100µs.

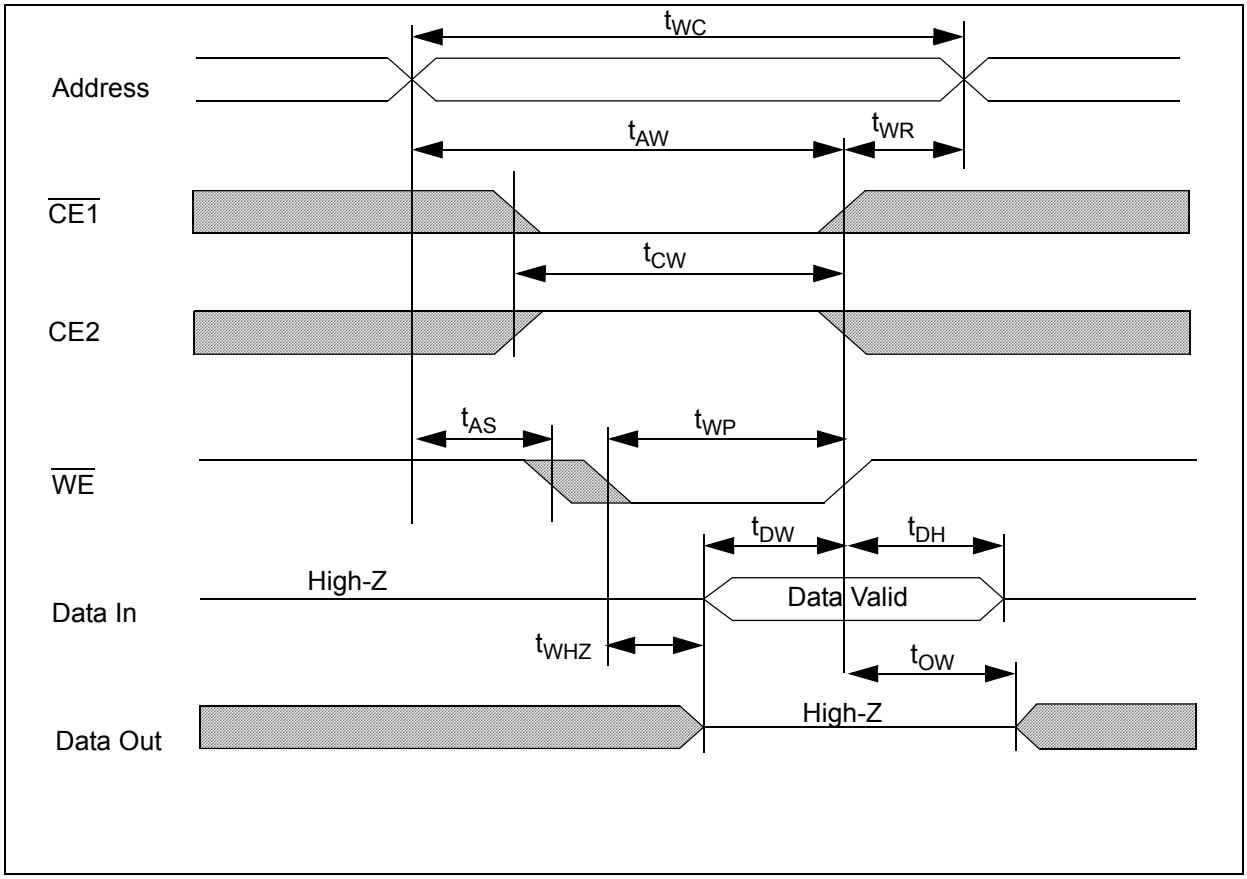
Timing of Read Cycle ($\overline{CE1}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = CE2 = V_{IH})



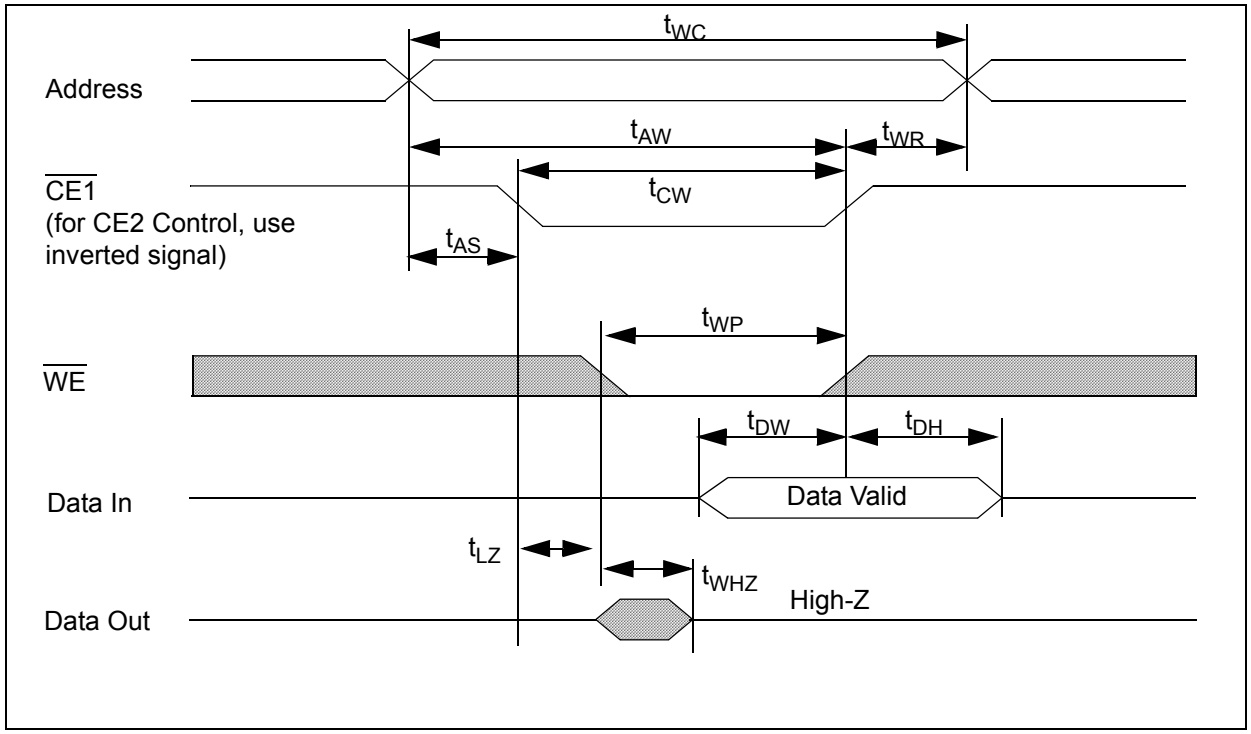
Timing Waveform of Read Cycle ($\overline{WE}$=V_{IH})



Timing Waveform of Write Cycle ($\overline{WE}$ control)



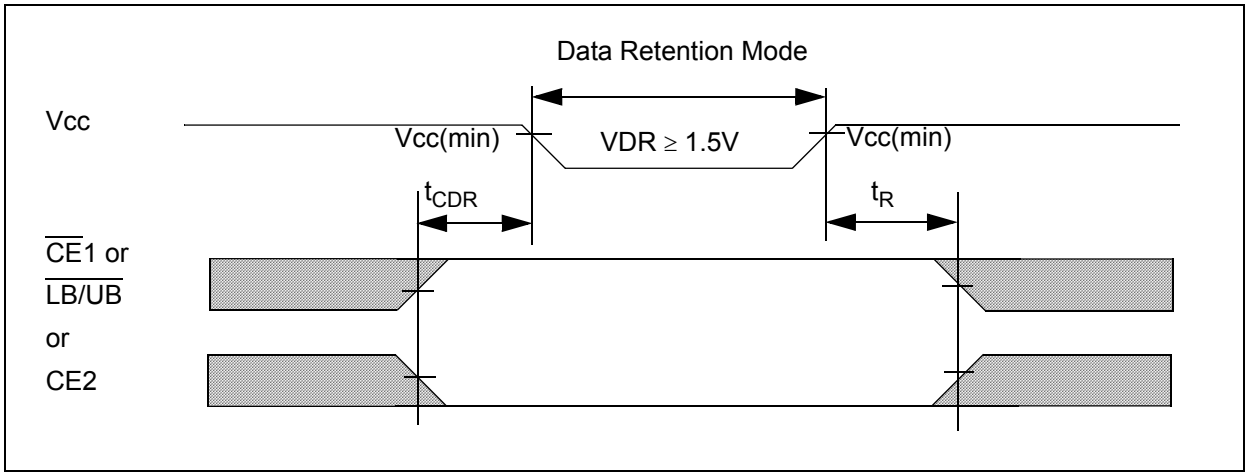
Timing Waveform of Write Cycle ($\overline{CE1}$ Control)



Data Retention Characteristics

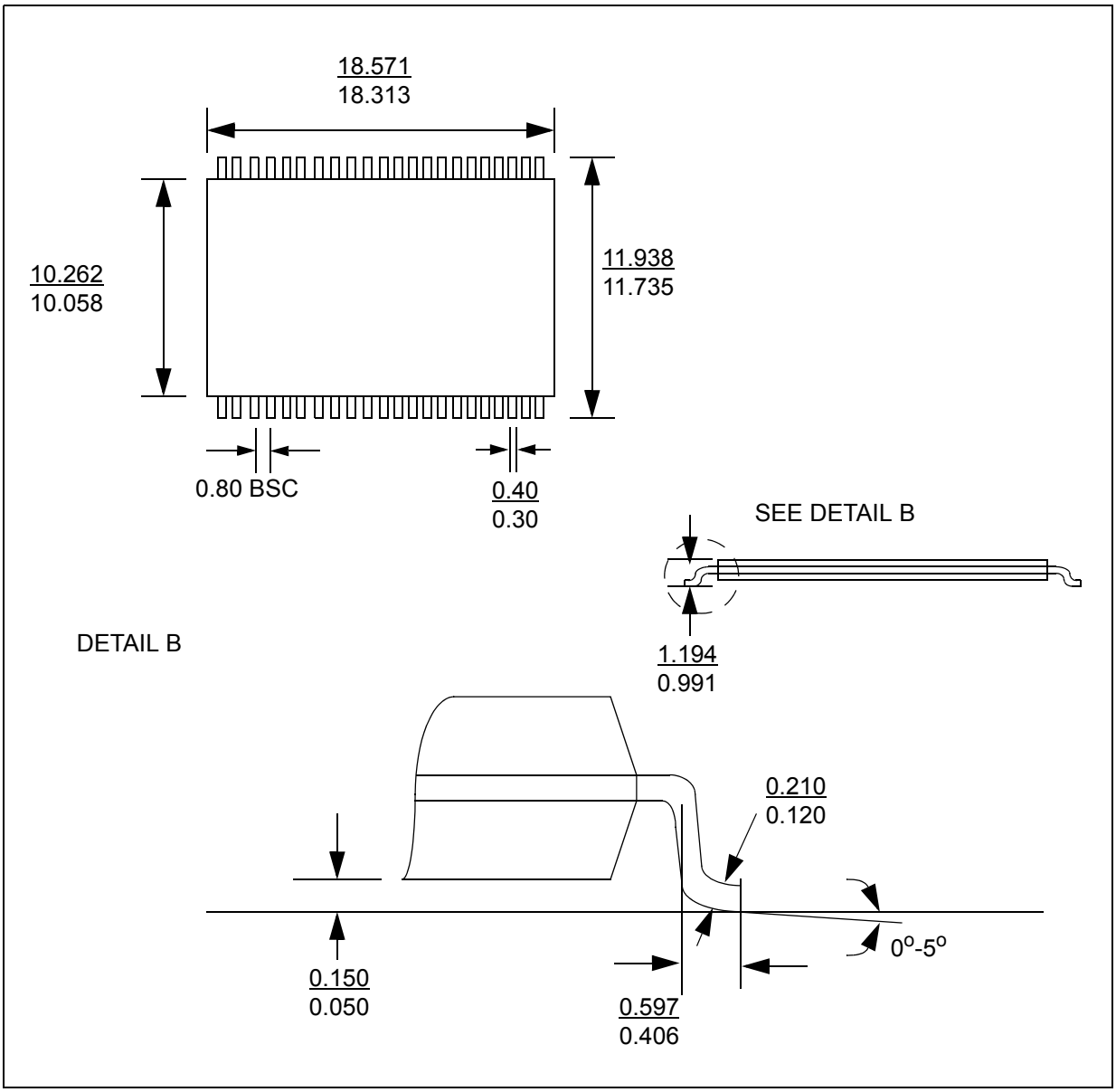
Parameter	Description	Condition		Min	Typ	Max	Unit
V_{DR}	Vcc for Data Retention			1.5			V
I_{CCDR}	Data Retention Current	Vcc = 1.5V, CE ≥ Vcc - 0.2V, VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V				10	µA
			-L			4	
t_{CDR}	Chip Deselect to Data Retention Time			0			ns
t_R	Operation Recovery Time			t_{RC}			ns

Data Retention Waveform

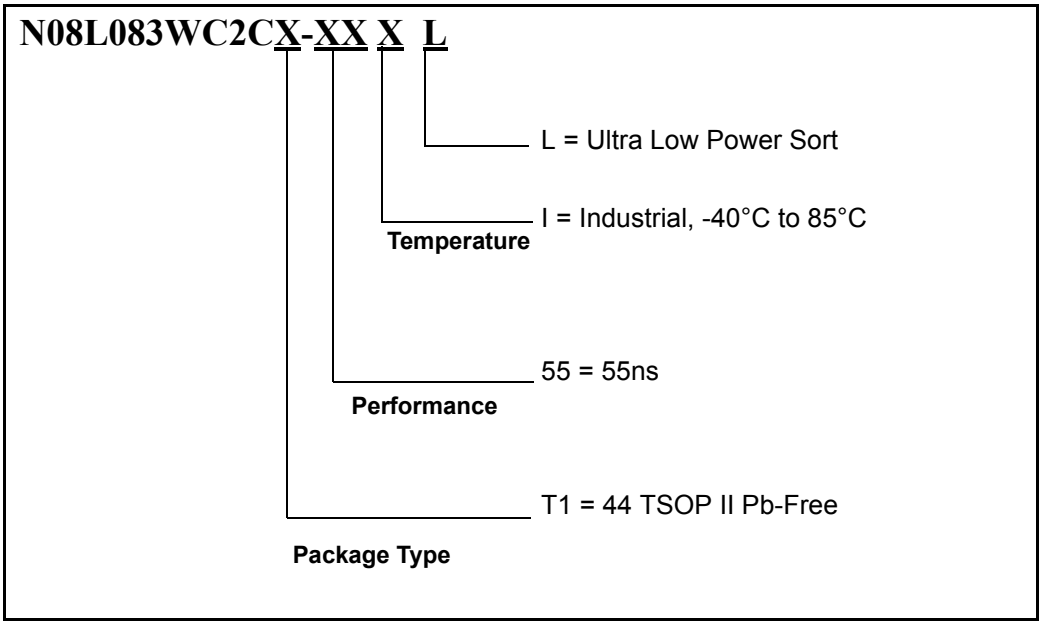


Note: Full device operation requires linear Vcc ramp from VDR to Vcc(min) > 100 µs

44 TSOP II Package (Z44)



Ordering Information



Revision History

Revision	Date	Change Description
A	Jan 14. 2005	Initial Release