April 2002
Revised December 2005

NC7SBU3157 • FSAU3157

Low Voltage SPDT Analog Switch with −2V Undershoot Protection

General Description

The NC7SBU3157 or FSAU3157 is a high performance, single-pole/double-throw (SPDT) Analog Switch or 2:1 Multiplexer/ Demultiplexer Bus Switch. The device is fabricated with advanced sub-micron CMOS technology to achieve high speed enable and disable times and low On Resistance. The break before make select circuitry prevents disruption of signals on the B Port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5V V_{CC} operating range. The control input tolerates voltages up to 5.5V independent of the V_{CC} operating range.

Fairchild's integrated Undershoot Hardened Circuit (UHC™) senses undershoot at the I/Os, and responds by preventing voltage differentials from developing and turning the switch on.

Features

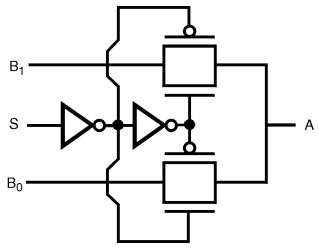
- Useful in both analog and digital applications
- Space saving SC70 6-lead surface mount package
- Low On Resistance: $< 10\Omega$ on typ @ 3.3V V_{CC}
- Broad V_{CC} operating range: 1.65V to 5.5V
- Rail-to-Rail signal handling
- Power down high impedance control input
- Overvoltage tolerance of control input to 7.0V
- Break before make enable circuitry
- 250 MHz - 3dB bandwidth
- Available in Lead (Pb) Free packaging

Ordering Code:

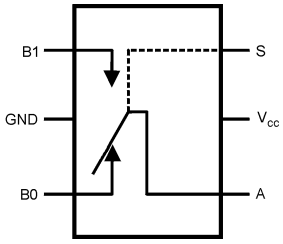
Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SBU3157P6X	MAA06A	U7A	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SBU3157P6X_NL	MAA06A	U7A	Pb-Free 6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
FSAU3157P6X	MAA06A	U7A	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel

Pb-Free package per JEDEC J-STD-020B.

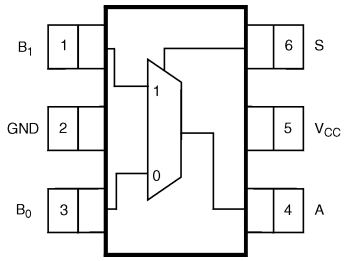
Logic Symbol



Analog Symbol

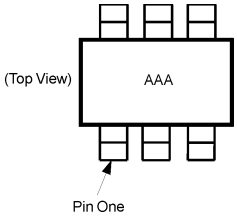


Connection Diagrams



(Top View)

Pin One Orientation Diagram



AAA = Product Code Top Mark - see ordering code.

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level
L = LOW Logic Level

Pin Descriptions

Pin Names	Description
A, B_0, B_1	Data Ports
S	Control Input

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S) (Note 2)	−0.5V to V_{CC} +0.5V
DC Input Voltage (V_{IN}) (Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
@ (I_{IK}) V_{IN} < 0V	−50 mA
DC Output Current (I_{OUT})	128 mA
DC V_{CC} or Ground Current (I_{CC}/I_{GND})	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @ +85°C	180 mW

Recommended Operating Conditions (Note 3)

Supply Voltage Operating (V_{CC})	1.65V to 5.5V
Control Input Voltage (V_{IN})	0V to V_{CC}
Switch Input Voltage (V_{IN})	0V to V_{CC}
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
Control Input V_{CC} = 2.3V - 3.6V	0 ns/V to 10 ns/V
Control Input V_{CC} = 4.5V - 5.5V	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	350°C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Control input must be held HIGH or LOW, it must not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
V_{IH}	HIGH Level Input Voltage	1.65 – 1.95	0.75 V_{CC}			0.75 V_{CC}		V	
		2.3 – 5.5	0.7 V_{CC}			0.7 V_{CC}			
V_{IL}	LOW Level Input Voltage	1.65 – 1.95			0.25 V_{CC}		0.25 V_{CC}	V	
		2.3 – 5.5			0.3 V_{CC}		0.3 V_{CC}		
I_{IN}	Input Leakage Current	0 – 5.5		±0.05	±0.1		±1	μA	0 ≤ V_{IN} ≤ 5.5V
I_{OZ}	OFF State Leakage Current	1.65 – 5.5		±0.05	±0.1		±1	μA	0 ≤ A, B ≤ V_{CC}
R_{ON}	Switch On Resistance (Note 4)	4.5		3.0	15.0		15.0	Ω	V_{IN} = 0V, I_O = 30 mA
				5.0	15.0		15.0	Ω	V_{IN} = 2.4V, I_O = −30 mA
				7.0	15.0		15.0	Ω	V_{IN} = 4.5V, I_O = −30 mA
		3.0		4.0	20.0		20.0	Ω	V_{IN} = 0V, I_O = 24 mA
				10.0	20.0		20.0	Ω	V_{IN} = 3V, I_O = −24 mA
		2.3		5.0	30.0		30.0	Ω	V_{IN} = 0V, I_O = 8 mA
				13.0	30.0		30.0	Ω	V_{IN} = 2.3V, I_O = −8 mA
		1.65		6.5	50.0		50.0	Ω	V_{IN} = 0V, I_O = 4 mA
				17.0	50.0		50.0	Ω	V_{IN} = 1.65V, I_O = −4 mA
I_{CC}	Quiescent Supply Current All Channels ON or OFF	5.5			1.0		10.0	μA	V_{IN} = V_{CC} or GND I_{OUT} = 0
	Analog Signal Range	V_{CC}	0		V_{CC}	0	V_{CC}	V	
R_{RANGE}	On Resistance Over Signal Range (Note 4)(Note 8)	4.5					25.0	Ω	I_A = −30 mA, 0 ≤ V_{Bn} ≤ V_{CC}
		3.0					50.0		I_A = −24 mA, 0 ≤ V_{Bn} ≤ V_{CC}
		2.3					100		I_A = −8 mA, 0 ≤ V_{Bn} ≤ V_{CC}
		1.65					300		I_A = −4 mA, 0 ≤ V_{Bn} ≤ V_{CC}
ΔR_{ON}	On Resistance Match Between Channels (Note 4)(Note 5)(Note 6)	4.5		0.15				Ω	I_A = −30 mA, V_{Bn} = 3.15
		3.0		0.2					I_A = −24 mA, V_{Bn} 2.1
		2.3		0.5					I_A = −8 mA, V_{Bn} = 1.6
		1.65		0.5					I_A = −4 mA, V_{Bn} = 1.15
V_{IKU}	Voltage Undershoot	5.5					−2.0	V	0.0 mA ≥ I_{IN} ≥ −50 mA, $\overline{OE}$ 5.5V
R_{flat}	On Resistance Flatness (Note 4)(Note 5)(Note 7)	5.0		6.0				Ω	I_A = −30 mA, 0 ≤ V_{Bn} ≤ V_{CC}
		3.3		12.0					I_A = −24 mA, 0 ≤ V_{Bn} ≤ V_{CC}
		2.5		28.0					I_A = −8 mA, 0 ≤ V_{Bn} ≤ V_{CC}
		1.8		125					I_A = −4 mA, 0 ≤ V_{Bn} ≤ V_{CC}

Note 4: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

Note 5: Parameter is characterized but not tested in production.

Note 6: ΔR_{ON} = R_{ON} max − R_{ON} min measured at identical V_{CC}, temperature and voltage levels.

DC Electrical Characteristics (Continued)

Note 7: Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

Note 8: Guaranteed by Design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus (Note 10)	1.65 – 1.95						ns	V_I = OPEN	Figures 2, 3
		2.3 – 2.7			1.2		1.2			
		3.0 – 3.6			0.8		0.8			
		4.5 – 5.5			0.3		0.3			
t_{PZL} t_{PZH}	Output Enable Time Turn on Time (A to B_n)	1.65 – 1.95	7.0		23.0	7.0	24.0	ns	V_I = 2 x V_{CC} for t_{PZL} V_I = 0V for t_{PZH}	Figures 2, 3
		2.3 – 2.7	3.5		13.0	3.5	14.0			
		3.0 – 3.6	2.5		6.9	2.5	7.6			
		4.5 – 5.5	1.7		5.2	1.7	5.7			
t_{PLZ} t_{PHZ}	Output Disable Time Turn Off Time (A Port to B Port)	1.65 – 1.95	3.0		12.5	3.0	13.0	ns	V_I = 2 x V_{CC} for t_{PLZ} V_I = 0V for t_{PHZ}	Figures 2, 3
		2.3 – 2.7	2.0		7.0	2.0	7.5			
		3.0 – 3.6	1.5		5.0	1.5	5.3			
		4.5 – 5.5	0.8		3.5	0.8	3.8			
t_{B-M}	Break Before Make Time (Note 9)	1.65 – 1.95	0.5			0.5		ns		Figure 4
		2.3 – 2.7	0.5			0.5				
		3.0 – 3.6	0.5			0.5				
		4.5 – 5.5	0.5			0.5				
Q	Charge Injection (Note 9)	5.0		7.0				pC	C_L = 0.1 nF, V_{GEN} = 0V R_{GEN} = 0Ω	Figure 5
		3.3		3.0						
OIRR	Off Isolation (Note 11)	1.65 – 5.5		−57.0				dB	R_L = 50Ω f = 10MHz	Figure 6
Xtalk	Crosstalk	1.65 – 5.5		−54.0				dB	R_L = 50Ω f = 10MHz	Figure 7
BW	−3dB Bandwidth	1.65 – 5.5		250				MHz	R_L = 50Ω	Figure 10
THD	Total Harmonic Distortion (Note 9)	5		0.011				%	R_L = 600 Ω 0.5 V_{P-P} f = 20 Hz to 20 KHz	

Note 9: Guaranteed by Design.

Note 10: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Note 11: Off Isolation = $20 \log_{10} [V_A / V_{Bn}]$

Capacitance (Note 12)

Symbol	Parameter	Typ	Max	Units	Conditions	Figure Number
C_{IN}	Control Pin Input Capacitance	2.3		pF	V_{CC} = 0V	
C_{IO-B}	B Port Off Capacitance	6.5		pF	V_{CC} = 5.0V	Figure 8
C_{IOA-ON}	A Port Capacitance When Switch Is Enabled	18.5		pF	V_{CC} = 5.0V	Figure 9

Note 12: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested in production.

Undershoot Characteristic (Note 13)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OUTU}	Output Voltage During Undershoot	2.5	V_{OH} - 0.3		V	Figure 1

Note 13: This test is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

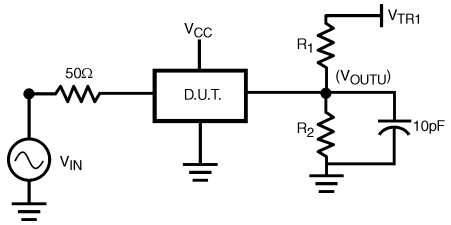
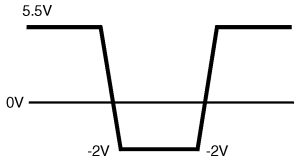


FIGURE 1.

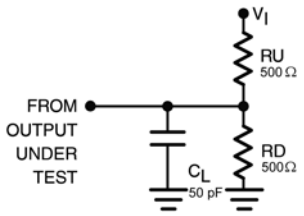
Device Test Conditions

Parameter	Value	Units
V_{IN}	see Waveform	V
$R_1 = R_2$	100K	Ω
V_{TRI}	7.0	V
V_{CC}	5.5	V

Transient Input Voltage (V_{IN}) Waveform



AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz; t_W = 500 ns

FIGURE 2. AC Test Circuit

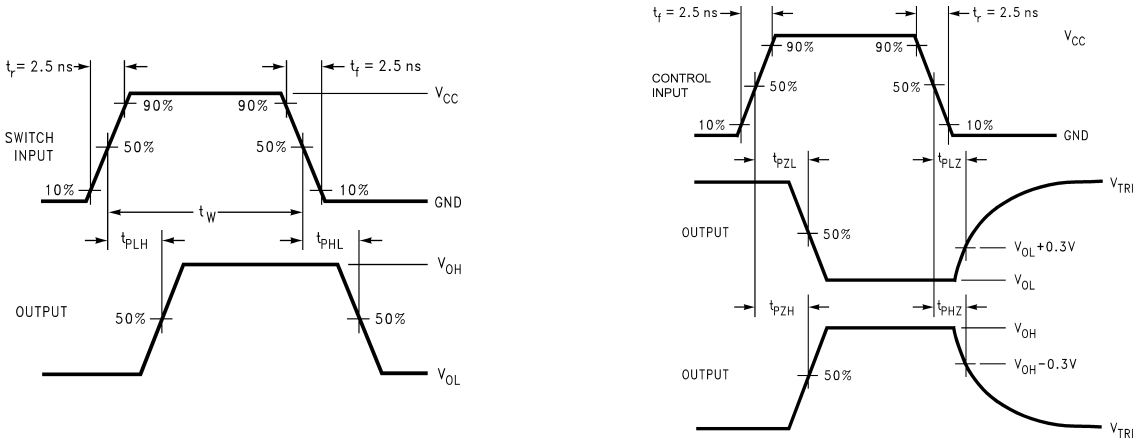


FIGURE 3. AC Waveforms

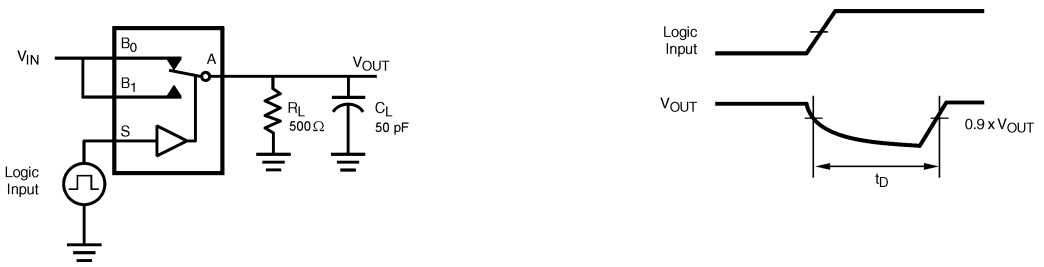
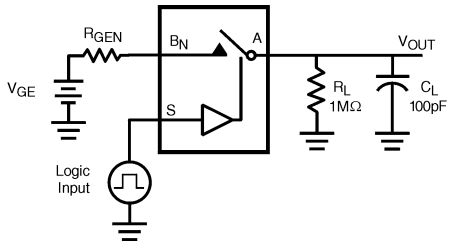


FIGURE 4. Break Before Make Interval Timing



AC Loading and Waveforms (Continued)

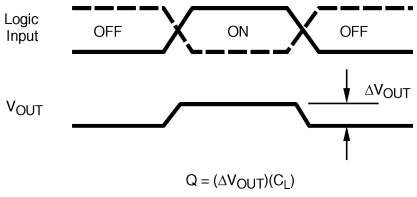


FIGURE 5. Charge Injection Test

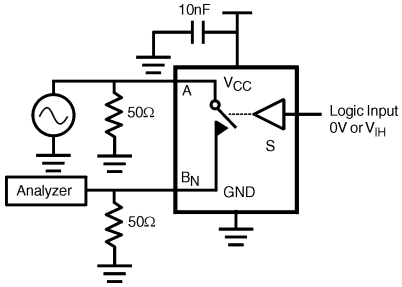


FIGURE 6. Off Isolation

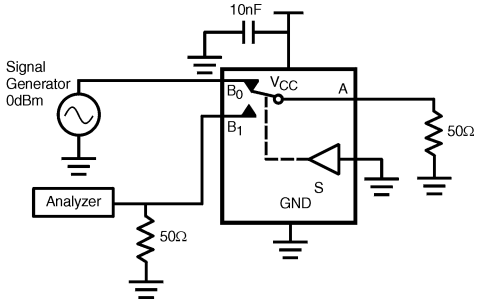


FIGURE 7. Crosstalk

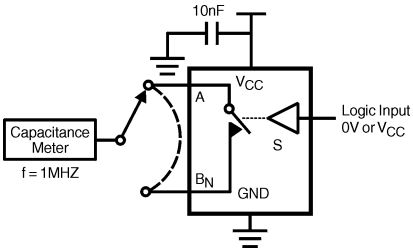


FIGURE 8. Channel Off Capacitance

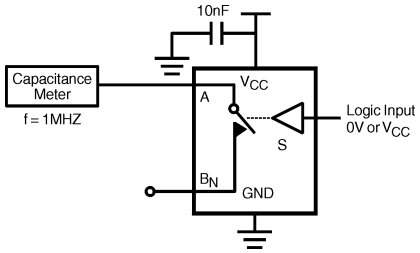


FIGURE 9. Channel On Capacitance

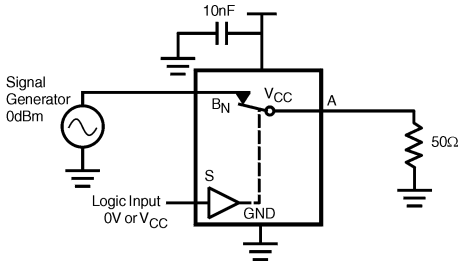


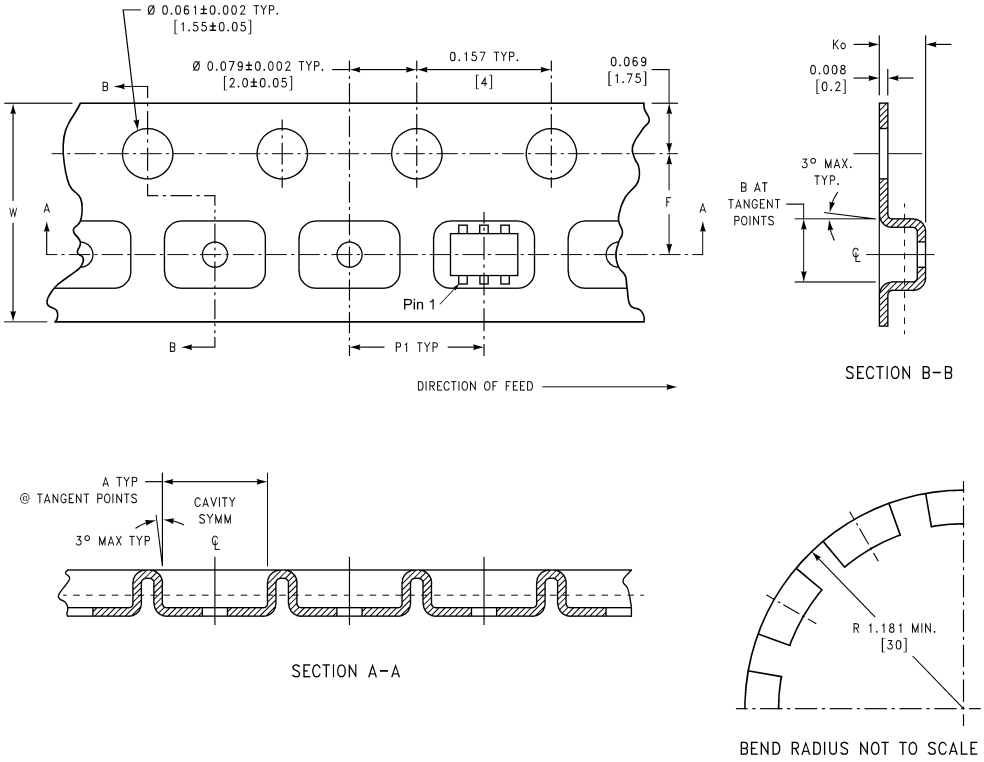
FIGURE 10. Bandwidth

Tape and Reel Specification

TAPE FORMAT

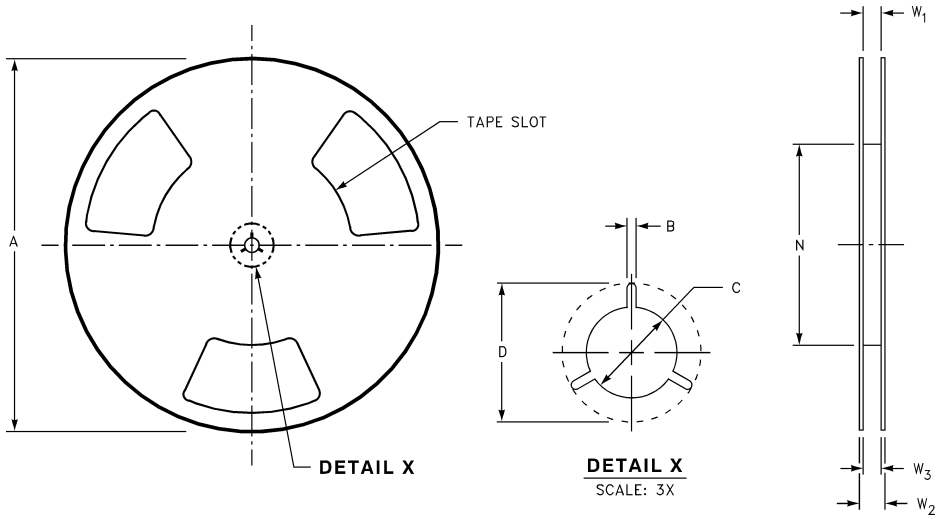
Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



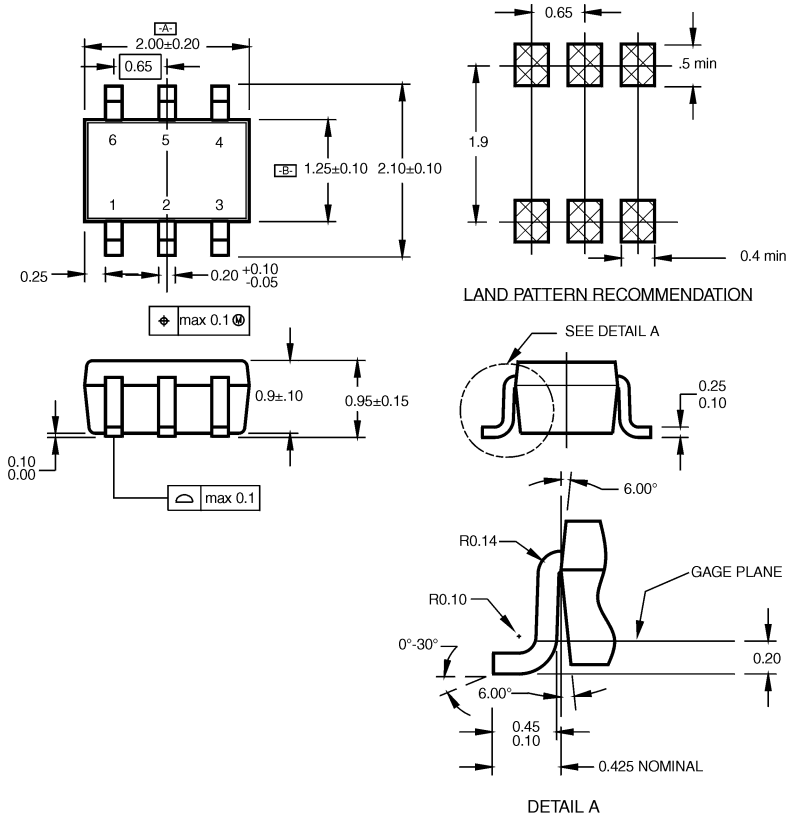
Package	Tape Size	DIM A	DIM B	DIM F	DIM K_o	DIM P1	DIM W
SC70-6	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)

REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
C. DIMENSIONS ARE IN MILLIMETERS.

MAA06ARevC

6-Lead SC70, EIAJ SC88, 1.25mm Wide
Package Number MAA06A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.