NetMos Technology

Nm9820

Single PCI UART

Features

- Single 5-V Operation
- Low Power
- PCI compatible single UART
- Pin-to-Pin compatible to Nm9835
- 16 byte transmit-receive FIFO (UART)
- Selectable receive trigger levels
- Programmable baud rate generator
- Modem control signals
- 5, 6, 7, 8 Bit characters selection
- Even, Odd, No parity, or Force parity generations
- Status report capability
- Compatible with 16C550
- On chip oscillator
- Re-map function for legacy ports
- Microsoft Compatible
- 128-pin VQFP package

Applications

- Embedded applications
- High speed modems
- Monitoring equipment
- Add on I/O cards
- Serial networking

General Description

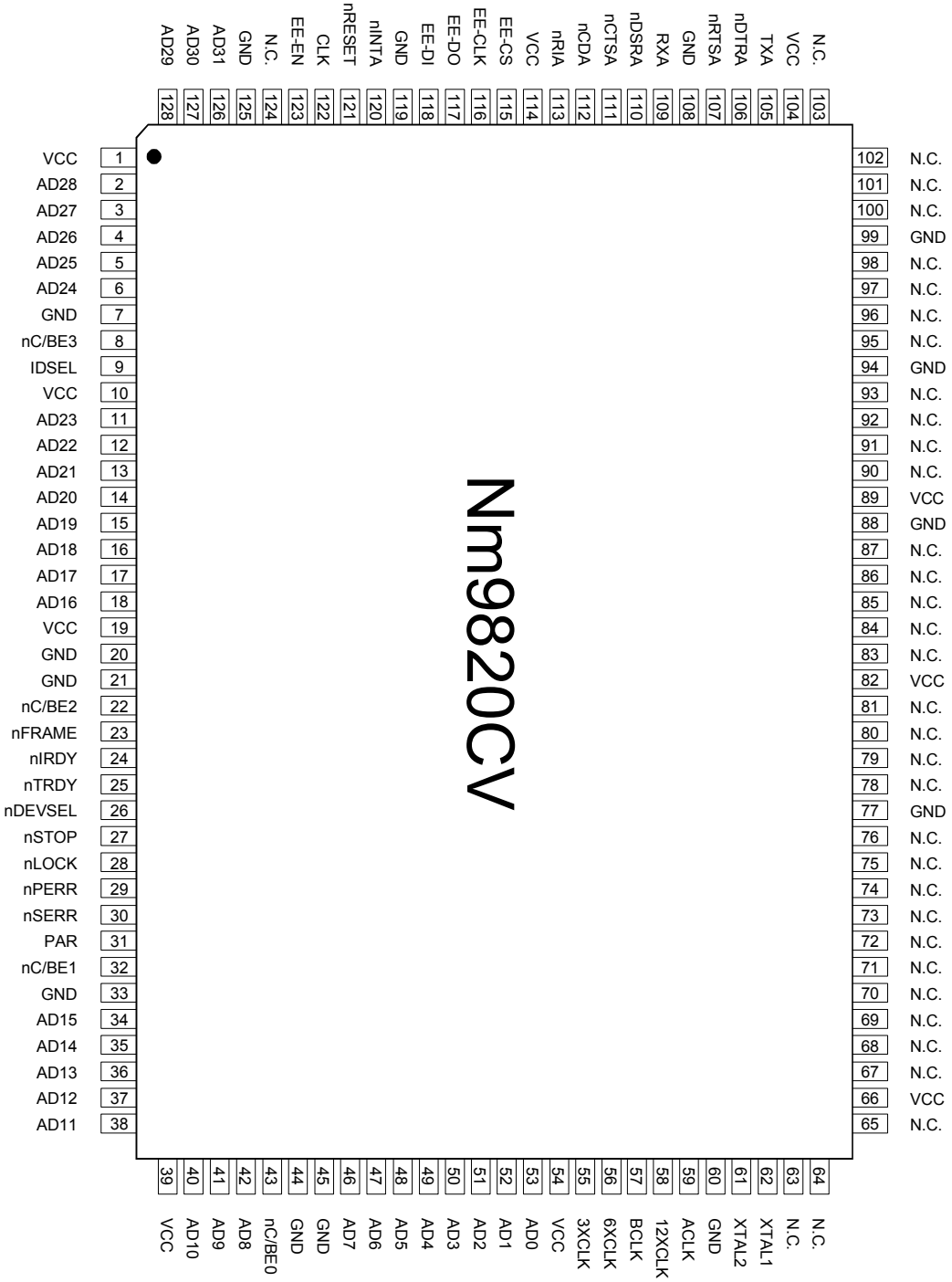
The Nm9820 is a PCI based single-channel high performance UART. The Nm9820 offers 16 byte transmit and receive FIFO compatible with standard 16C550. The Nm9820 perform serial-to-parallel conversions on data received from a peripheral device, and parallel-to-serial conversion on data received from its CPU.

The Nm9820 is ideally suited for PC applications, such as high-speed COM ports. The Nm9820 is available in 128-Pin QFP package, it is fabricated in an advanced in submicron CMOS process to achieve low drain power and high-speed requirements.

Ordering Information

Commercial Grade		
Nm9820CV	128-VQFP	0° C to +70° C
Industrial Grade		
Nm9820EV	128-VQFP	-40° C to +85° C

128-Pin VQFP Package



Pin Name	128	Type	Description
CLK	122	I	33 MHz PCI system clock input.
nRESET	121	I	PCI System reset (avtice low). Resets all internal register, sequencers, and signals to a consistent state. During reset condition AD31-0, nSER are three-stated.
AD31-29	126-128	I/O	Multiplexed PCI address / data bus. A bus transaction consists of an address phase followed by one or more data phase. During the address phase AD31-0 contain a physical address. Write data is stable and valid when nIRDY and nTRDY are asserted (active).
AD28-24	2-6	I/O	See AD31-29 description.
AD23-16	11-18	I/O	See AD31-29 description.
AD15-11	34-38	I/O	See AD31-29 description.
AD10-8	40-42	I/O	See AD31-29 description.
AD7-0	46-53	I/O	See AD31-29 description.
nFRAME	23	I	Frame is driven by the current master to indicate the beginning and duration of an access. nFRAME is asserted to indicate a bus transaction is beginning. While nFRAME is active, data transfer continues.
nIRDY	24	I	Initiator Ready. During a write, nIRDY asserted indicates that the initiator is driving valid data onto the data bus. During a read, nIRDY asserted indicates that the initiator is ready to accept data from the Nm9820.
nTRDY	25	O	Target Ready (three-state). It is asserted when Nm9820 is ready to complete the current data phase.
nSTOP	27	O	Nm9820 asserts nSTOP to indicate that it wishes the initiator to stop the transaction in process on the current data phase.
nLOCK	28	I	Lock indicates an atomic operation that my require multiple transactions to complete.
IDSEL	9	I	Initialization Device Select. It is used as a chip select during configuration read and writes transactions.
nDEVSEL	26	O	Device Select (three-state). Nm9820 asserts nDEVSEL when the Nm9820 has decoded its address.

Pin Name	128	Type	Description
nPERR	29	O	Parity Error (three-state). Is used to report parity errors during all PCI transactions except a Special Cycle. The minimum duration of nPERR is one clock cycle.
nSERR	30	O	System Error (open drain). This pin goes low when address parity errors are detected.
PAR	31	I/O	Even Parity. Parity is even parity across AD31-0 and nC/BE3-0. PAR is stable and valid one clock after the address phase. For data phase PAR is stable and valid one clock after either nIRDY is asserted on a write transaction or nTRDY is asserted on a read transaction.
nC/BE3	8	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During data phase nC/BE3-0 are used as Byte Enables.nC/BE3 applies to byte “3”.
nC/BE2	22	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During data phase nC/BE3-0 are used as Byte Enables. nC/BE2 applies to byte “2”.
nC/BE1	32	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During data phase nC/BE3-0 are used as Byte Enables. nC/BE1 applies to byte “1”.
nC/BE0	43	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During data phase nC/BE3-0 are used as Byte Enables. nC/BE0 applies to byte “0”.
nINTA	120	O	PCI active low interrupt output (open-drain). This signal goes low (active) when an interrupt condition occurs.
EE-CS	115	O	External EE-Prom chip select (active high). After power on reset, Nm9820 reads the EE-Prom and loads the read-only configuration registers sequentially from the first 64 bytes in the EE-Prom.
EE-CLK	116	O	External EE-Prom clock.
EE-DI	118	I	External EE-Prom data input.
EE-DO	117	O	External EE-Prom data output.
EE-EN	123	I	Enable/Disable external EEprom (active high, internal pull-up). External EEprom can be disabled when this pin is tied to GND or pulled low. When external EEprom is disabled, the default values for Nm9820 will be loaded into PCI configuration register.

Pin Name	128	Type	Description
XTAL1	62	I	Crystal oscillator input or External clock input pin (22.1184 MHz). This signal input is used in conjunction with XTAL2 to form a feedback circuit for the internal timing. Two external capacitors (10pF) connected from each side of the XTAL1 and XTAL2 to GND is required to form a crystal oscillator circuit.
XTAL2	61	O	Crystal oscillator output. See XTAL1 description.
12XCLK	58	O	External clock or crystal oscillator clock divide by 12 output (1.8432 MHz standard PC UART clock for 115.2k data rate).
6XCLK	56	O	External clock or crystal oscillator clock divide by 6 output (3.6864 MHz PC UART clock for 230.4k data rate).
3XCLK	55	O	External clock or crystal oscillator clock divide by 3 output (7.3728 MHz UART clock for 460.8k data rate).
ACLK	59	I	UART-A clock input. ACLK should be connected to external clock source or one of the 12XCLK, 6XCLK, 3XCLK output pins of the Nm9820.
BCLK	57	I	UART-B clock input. BCLK should be connected to external clock source or one of the 12XCLK, 6XCLK, 3XCLK output pins of the Nm9820.
TXA	105	O	UART-A Serial data output.
nRTSA	107	O	Active low, UART-A request-to-send signal. It is set to high (in active) after a hardware reset or during internal loop-back mode. When low, this indicates that Modem or data set is ready to establish a communication link. nRTSA has no effect on the transmitter or receiver.
nDTRA	106	O	Active low, UART-A data-terminal-ready signal. It is set to high (in active) after a hardware reset or during internal loop-back mode. When low, this output indicates to the Modem or data set that the UART-A is ready to establish a communication link. nDTRA has no effect on the transmitter or receiver.
RXA	109	I	UART-A, Serial data input.
nCTSA	111	I	Active low, UART-A clear-to-send signal. When low this indicates that Modem or data set is ready to exchange data. nCTSA has no effect on the transmitter.
nDSRA	110	I	Active low, UART-A data-set-ready signal.
nCDA	112	I	Active low, UART-A Carrier-detect signal. When low this indicates that Modem or data set has detected the data carrier. nCDA has no effect on the transmitter.
nRIA	113	I	Active low, UART-A ring-detect signal.

Pin Name	128	Type	Description
GND	7,20,21, 33,44,45, 60,77,88, 94,99,108 119,125	Pwr	Power and signal ground.
VCC	1,10,19, 39,54,66, 82,89,104, 114	Pwr	5-V Supply.

PCI bus operation:
The execution of PCI bus transaction takes place in broadly five stages, address phase, transaction Claiming, data phase(s), final data transfer and transaction completion.

Address phase:
Every PCI transaction starts off with an address phase, one PCI clock period in duration. During address phase the initiator (Also known as current bus master) identifies the target device (via the address) and type of transaction. (via the Command).The initiator drives the 32 bit address on to 32 bit Address/Data bus and 4bit command on to 4bit Command / Byte enable bus. The initiator also asserts the nFRAME signal during the same clock cycle to indicate the presence of valid address and transaction type on those buses. The initiator supplies start address (and the target, Nm9820, generates the subsequent sequential addresses for burst transfers) and command type for one PCI clock cycle. The Address/Data bus becomes Data bus and Command/Byte enable bus becomes Byte enable bus for the remainder of the clock cycles of that transaction. The target (Nm9820) latches the address and command type on the next rising edge of PCI clock (and so do all the devices on that PCI bus). The target (Nm9820) decodes the address and determines whether it is being addressed, and decodes the command to determine the type of transaction.

Claiming the transaction:
When Nm9820 determines that it is the target of a transaction, it claims the transaction by asserting nDEVSEL.

Data phase(s):
The data phase of a transaction is the period during which a data object is transferred between the initiator and the target (Nm9820). The number of data bytes to be transferred during a data phase is determined by the number of Command/Byte enable signals that are asserted by the initiator during the data phase. Each data phase is at least one PCI clock period in duration. Both initiator and target must indicate that they are ready to complete a data phase. If not, the data phase is extended by a wait state of one clock period in duration. The initiator and the target indicate this by asserting nIRDY and nTRDY respectively and the data transfer is completed at the rising edge of the next PCI clock.

Transaction duration:
The initiator, as stated earlier, gives only start address during address phase but does not tell the number of data transfers in a burst transfer transaction. However the initiator indicates the completion of data transfer of a transaction by asserting nIRDY and de-asserting nFRAME during the last data transfer phase. The transaction however, does not complete until the target has also asserted the nTRDY signal and the last data transfer takes place. At this point the nTRDY and nDEVSEL are de-asserted by the target.

Transaction completion:
When all of nIRDY, nTRDY, nDEVSEL, and nFRAME are in inactive state (high state), the bus is in idle state. The bus is ready to be claimed by another bus master.

Internal address select configuration

I/O Address	Function
XX00-XX07	UART (E1)

Nm9820 Configuration space register map

AD 31-23	AD 22-16	AD 15-8	AD 7-0	Addr
Device ID (9820)		Vendor ID (9710)		00H
Status		Command		04H
Class Code (070002)			Revision ID (01)	08H
BIST	Header Type	Latency Timer	Cache Size (08)	0CH
I/O (E1)Base Address				10H
I/O (E2)Base Address				14H
I/O (E3)Base Address				18H
I/O (E4)Base Address				1CH
Reserved				20H
Reserved				24H
Reserved				28H
Subsystem ID		Subsystem Vendor ID		2CH
Reserved				30H
Reserved				34H
Reserved				38H
Max Latency (00)	Min Grant (00)	Interrupt Pin (01)	Interrupt Line	3CH

UART Registers Table

Ex A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
Ex 0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Ex 0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Ex 0 0 1	IER	0	0	Power Down	Sleep Mode	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
Ex 0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
Ex 0 1 0	IIR	0/ FIFO enabled	0/ FIFO enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
Ex 0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
Ex 1 0 0	MCR	0	0	Flow Control	loop back	INT enable (nOP2)	(nOP1)	nRTS	nDTR
Ex 1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
Ex 1 1 0	MSR	nCD	nRI	nDSR	nCTS	delta nCD	delta nRI	delta nDSR	delta nCTS
Ex 1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Ex **0 0 0**	**DLL**	**bit-7**	**bit-6**	**bit-5**	**bit-4**	**bit-3**	**bit-2**	**bit-1**	**bit-0**
Ex **0 0 1**	**DLM**	**bit-15**	**bit-14**	**bit-13**	**bit-12**	**bit-11**	**bit-10**	**bit-9**	**bit-8**

DLL and DLM are accessible only when LCR Bit-7=1.
E1: Internal UART-A chip select
E2: Internal UART-B chip select

UART Registers Description

Transmitter Holding Register (THR)
The transmitter section of the Nm9820 consists of a transmitter holding register (THR) and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Transmitter section control is a function of the Nm9820 line control register. The Nm9820 THR receives data off the internal data bus and when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at TX. In the 16C450 mode, if the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled (IER-1=1), an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

Receive Holding Register (RHR)
The receiver section of the Nm9820 consists of a receiver shift register (RSR) and a receiver Holding register (RHR). The RHR is actually a 16-byte FIFO. Timing to receive holding register is supplied by the 16x-receiver clock. Receiver section control is a function of the Nm9820 line control register.
The Nm9820 RHR receives serial data from RX. The RSR then concatenates the data and moves it into the RHR FIFO. In the 16C450 mode, when a character is placed in the receiver holding register and the received data available interrupt is enabled (IER-0=1), an interrupt is generated. This interrupt is cleared when the data is read out of the receiver holding register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

Interrupt Enable Register (IER)
The interrupt enables register enables each of the five types of interrupts and INT pin response to an interrupt generation. The interrupt enable register can also be used to disable the interrupt system by setting bits 0-3 to logic 0. The contents of this register are described below.

IER Bit-0:
0 = Disable the received data available interrupt.
1 = Enables the received data available interrupt.

IER Bit-1:
0 = Disable the transmitter holding register empty interrupt.
1 = Enable the transmitter holding register empty interrupt.

IER Bit-2:
0 = Disables the receiver line status interrupt.
1 = Enables the receiver line status interrupt.

IER Bit-3:
0 = Disables the modem status interrupt.
1 = Enables the modem status interrupt.

IER Bit 4:
0 = Standard 16C450/550 mode. Sleep mode is disabled.
1 = Enables Sleep mode. The Nm9820 is always awake when there is a byte in the transmitter, activity on the RX, or either Delta CTS, Delta DSR, Delta CD, Delta RI is/are set to logic “1”, or when the device is in the loop-back mode.

IER Bit 5:
0 = Standard 16C450/550 mode. Power down mode is disabled.
1 = Enables the power down mode. Power down mode functions similar to Sleep mode, except oscillator section.

IER Bits 6-7:
These bits are not used (always set to 0).

Interrupt Identification Register (IIR)
The Nm9820 has an on chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors.

IIR Bit-0:
0 = An interrupt is pending. Used either in a hardware prioritized or polled interrupt system.
1 = No interrupt is pending.

IIR Bits 1-2:
The Nm9820 provides four prioritized levels of interrupts:

Priority 1 - Receiver line status (highest priority)
Priority 2 - Receiver data ready
Priority 2 - Receiver character time-out
Priority 3 - Transmitter holding register empty
Priority 4 - Modem status (lowest priority)

When an interrupt is generated, the interrupt identification register indicates that an interrupt is pending and encodes the type of interrupt in its three least significant bits (bits 0, 1, and 2).

Interrupt Priority decode

Bit-3	Bit-2	Bit-1	Bit-0	Interrupt source
0	1	1	0	Receive data Error
0	1	0	0	Receive data ready
1	1	0	0	Receive time-out
0	0	1	0	Transmit holding empty
0	0	0	0	Modem status change

The bits are used to identify the highest priority interrupt pending.

IIR Bit-0 will clear to “1” when no interrupt is pending. To clear the interrupts following reads from registers are required.

Receive Data Error:
Reading LSR register will clear this interrupt. User should save LSR value after reading the register to maintain the error condition.

Receive Data Ready:
Reading RHR register till FIFO becomes empty.

Receive Timeout:
Reading entire characters from RHR.

Transmit Holding empty:
Writing a character into THR register or reading IIR register (if source of interrupt).

Modem Status Change:
Reading MSR register will clear this interrupt.

IIR Bit-3:
0 = In the 16C450 mode. In FIFO mode, this bit is set along with bit-2 to indicate that a time-out interrupt is pending.

IIR Bit 4:
This bit is not used (always reset at 0).

IIR Bit 5:
0 = 16C450/550 mode, 16 byte FIFO mode.
1 = Enhance FIFO mode. 64 byte FIFO mode enabled.

IIR Bits 6-7:
0 = In the 16C450 mode.
1 = When FCR-0 is equal to 1.

FIFO control register (FCR)
The FIFO control register (FCR) is a write only register. The (FCR) enables and clears the FIFO sets receive FIFO trigger level, and selects the type of DMA signaling.

FCR Bit-0:
0 = 16C450 mode, disables the transmitter and receiver FIFO.
1 = Enables the transmitter and receiver FIFO. This bit must be set to 1 when other (FCR) bits are written to or they are not programmed. Changing this bit clears the FIFO.

FCR Bit-1:
0 = Normal operation
1 = Clears all bytes in the receiver FIFO and resets its counter logic to 0. The shift register is not cleared. The one that is written to this bit position is self-clearing.

FCR Bit-2:
0 = Normal operation
1 = Clears all bytes in the transmit FIFO and resets its counter logic to 0. The shift register is not cleared. The one that is written to this bit position is self-clearing.

FCR Bit-3:
0 = Mode [0]:
Supports single transfer DMA (16C450 mode) in which a transfer is made between CPU bus cycle.
1 = Mode [1]:
Supports multi transfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied.

FCR Bit 5-4:
This bit is not used.

FCR Bits 6-7:
These bits are used to set the trigger level for receive FIFO interrupt.

Receive trigger levels (BYTES)

Bit-7	Bit-6	RX FIFO trigger level
0	0	1
0	1	4
1	0	8
1	1	14

Line Control Register (LCR)
The system programmer controls the format of the asynchronous data communication exchange through the line control register. In addition, the programmer is able to retrieve, inspect, and modify the contents of the line control register; this eliminates the need for separate storage of the line characteristics in system memory.

LCR Bits 0-1:
These two bits specify the number of bits in each transmitted or received serial character.

Word Length

Bit-1	Bit-0	Word length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

LCR Bit-2:
This bit specifies, 1, 1-1/2, or 2 stop bits in each transmitted character. When bit-2 is reset to 0, one stop bit is generated in the data. When bit-2 is set to 1, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks only the first stop bit regardless of the number of stop bits selected. The number of stop bits generated in relation to word length and bit-2.

Stop Bits

Bit-2	Word length	Stop bit(s)
0	X	1
1	5 bits	1-1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

LCR Bit-3:
0 = Parity is disabled. No parity is generated or checked.
1 = Parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, parity is checked.

LCR Bit-4:
0 = ODD parity select bit. When parity is enabled by bit-3, a 1 in bit-4 produces odd parity (an odd number of 1's in the data and parity bits.
1 = Even parity select bit. When parity is enabled by bit-3, a 1 in bit-4 produces even parity (an even number of 1's in the data and parity bits).

LCR Bit-5:
0 = Stick parity is disabled.
1 = Stick parity bit. When bits 3-5 are set to 1 the parity bit is transmitted and checked as a 0. When bits-3 and 5 are 1's and bit-4 is a 0, the parity bit is transmitted and checked as 1.

Parity selection

Bit-5	Bit-4	Bit-3	Parity type
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Forced parity “1”
1	1	1	Forced parity “0”

LCR Bit-6:
0 = Normal operation. Break condition is disabled and has no effect on the transmitter logic.
1 = Force a break condition. A condition where TX is forced to the space (low) state.

LCR Bit-7:
0 = Normal operation.
1 = Divisor latch enable. Must be set to 1 to access the divisor latches of the baud generator during a read or write. Bit-7 must be reset to 0 during a read or write to the receiver holding, the transmitter holding register, or the interrupt enable register.

Modem Control Register (MCR)
The modem control register is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem.

MCR Bit-0:
0 = Sets the nDTR output pin to high.
1 = Sets the nDTR output pin to low.

MCR Bit-1:
0 = Sets the nRTS output pin to high.
1 = Sets the nRTS output pin to low.

MCR Bit-2:
0 = Sets the nOP1 to high during loop-back mode.
1 = Sets the nOP1 to low during loop-back mode.

MCR Bit-3:
0 = Disables UART interrupt. Sets the nOP2 to high during loop-back mode.
1 = Enables UART interrupt. This bit is gated with IER Bits 0-3. Sets the nOP2 to low during loop-back mode.

MCR Bit-4:
0 = Normal operation.
1 = Internal loop back mode. Provides a local loop-back feature for diagnostic testing of the Nm9820. When LOOP is set to 1, the following occurs:
The transmitter TX pin is set to high.
The receiver RX pin is disconnected.
The output of the transmitter shift register is looped back into the receiver shift register input.
The four modem inputs (nCTS, nDSR nCD and nRI) pins are disconnected. The four modem outputs (nDTR, nRTS, nOP1, and nOP2) pins are internally connected to the four modem inputs. The four modem outputs are forced to the high levels.

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify transmit and receive data paths to the Nm9820. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the modem control interrupt sources are now the lower four bits of the modem control register instead of the four modem control inputs. All interrupts are still controlled by the interrupt enable register.

MCR Bit-5:
0 = 16C450/550 mode. Hardware flow control is disabled.
1 = Enable hardware flow control (nRTS/nCTS).

MCR Bit-5	MCR Bit-1	Flow Control
1	1	Auto RTS/CTS
1	0	Auto CTS only
0	X	Disabled

nRTS becomes active (low) when the receiver is empty or the threshold has not been reached. When receiver FIFO level reaches a trigger level of 1, 4, 8, and 14, nRTS is de-asserted (high). nRTS is automatically re-asserted once the receiver FIFO is empty by reading receive holding register.

The transmitter circuitry checks nCTS before sending the next data byte. When nCTS is active (low), the transmitter sends the next byte. To stop the transmitter

from sending the next byte, nCTS must be released before the middle of the last stop bit that is currently being sent.

MCR bits 6-7:
These bits are not used.

Line Status Register (LSR)
The line status register provides information to the CPU concerning the status of data transfers. The line status register is intended for read operations only; writing to this register is not recommended. Bits 1-4 are the error conditions that produce a receiver line status interrupt.

LSR Bit-0:
0 = No data in receive holding or FIFO.
1 = Data ready indicator for the receiver. This bit is set to 1 whenever a complete incoming character has been received and transferred into the receiver holding register or the FIFO. It is reset to 0 by reading all of the data in the receiver holding register or the FIFO.

LSR Bit-1:
0 = Normal operation. No overrun error.
1 = It indicates that before the character in the receiver holding register was read, it was over written by the next character transferred into the register. OE is reset every time the CPU reads the contents of the line status register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR Bit-2:
0 = Normal operation (No parity error).
1 = It indicates that the parity of the received data character does not match the parity selected in the line control register. PE is reset every time the CPU reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.

LSR Bit-3:
0 = Normal operation (No framing error).
1 = It indicates that the received character did not have a valid stop bit. FE is reset every time the CPU reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The Nm9820 tries to re-synchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit.

LSR Bit-4:
0 = Normal operation.
1 = It indicates that the received data input was held in the logic low state for longer than a full word transmission time. A full word transmission time is defined as the total time to transmit the start, data, parity, and stop bits. BI is reset every time the CPU reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO.

LSR Bit-5:
0 = At least one byte is written to the transmit FIFO or transmit holding register.
1 = Transmitter holding register is empty, indicating that the Nm9820 is ready to accept a new character. If the THRE interrupt is enabled when THRE is set to 1, an interrupt is generated. THRE is set to 1 when the contents of the transmitter holding register are transferred to the transmitter shift register.

LSR Bit-6:
0 = When either the transmitter holding register or the transmitter shift register contains a data character.
1 = Transmitter holding register and the transmitter shift register are both empty.

LSR Bit-7:
0 = In the 16C450, this bit is always reset to 0.
1 = In the FIFO mode, at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

Modem Status Register (MSR)
The modem status register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provide change information, when input from the modem Changes State, the appropriate bit is set to 1. All four bits are reset to 0 when the CPU reads the modem status register.

MSR Bit-0:
0 = No change to nCTS input.
1 = Indicates that the nCTS input has changed state since the last time it was read by the CPU. When interrupt is enabled, a modem status interrupt is generated.

MSR Bit-1:
0 = No change to nDSR input.
1 = Indicates that the nDSR input has changed state since the last time it was read by the CPU. When interrupt is enabled, a modem status interrupt is generated.

MSR Bit-2:
0 = No change to nRI input.
1 = Indicates that the nRI input has changed from a low to a high level. When nRI is set to 1 and the modem status interrupt is enabled, a modem status interrupt is generated.

MSR Bit-3:
0 = No change to nCD input.
1 = Indicates that the nCD input has changed state since the last time it was read by the CPU. When interrupt is enabled, a modem status interrupt is generated.

MSR Bit-4:
Complement of the clear to send (nCTS) input. When the Nm9820 is in the diagnostic test mode, this bit is equal to nRTS.

MSR Bit-5:
Complement of the data set ready (nDSR) input. When the Nm9820 is in the diagnostic test mode, this bit is equal to nDTR.

MSR Bit-6:
Complement of the ring indicator (nRI) input. When the Nm9820 is in the diagnostic test mode, this bit is equal to nOP1.

MSR Bit-7:
Complement of the data carrier detects (nCD) input. When the Nm9820 is in the diagnostic test mode, this bit is equal to nOP2.

Scratch Pad Register (SPR)
The scratch pad register is an 8-bit register that is intended for programmer use as a scratch pad in the sense that it temporarily holds the programmer data without affecting any other Nm9820 operation.

Programmable Baud-Rate Generator
The Nm9820 contains a programmable baud generator that takes a clock input of 1.8432 MHz and divides it by a divisor in the range between 1 and (2_{16}-1) The output frequency of the baud generator is 16 times the baud rate. Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the Nm9820 in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Baud rate generator programming table for 1.8432 MHz clock (12XCLK).

Baud out	DLM (hex)	DLL (hex)
115.2k	00	01
57.6k	00	02
38.4k	00	03
19.2	00	06
9600	00	0C
2400	00	30
1200	00	60
600	00	C0
300	01	80
150	03	00
50	09	00

FIFO interrupt mode operation
When the receiver FIFO and receiver interrupts are enabled (FCR-0=1, IER-0=1, IER-2=1), a receiver interrupt occurs as follows:

The received data available interrupt issued to the microprocessor when the FIFO has reached its programmed trigger level. It is cleared when the FIFO drops below its programmed trigger level. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.

The receiver line status interrupt has higher priority than the received data available interrupt. The data ready bit (LSR-0) is set when a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

When the receiver FIFO and receiver interrupts are enabled, FIFO time-out interrupt occurs when the following conditions exist:

At least one character is in the FIFO. The most recent serial character was received more than four continuous character times ago (if two stop bits are programmed, the second one is included in this time delay). The most recent microprocessor read of the FIFO occurred more than five continuous character times ago. When a time-out interrupt has occurred, it is cleared and the timer is reset when the microprocessor reads one character from the receiver FIFO.
When a time-out interrupt has not occurred, the time-out timer is reset after a new character is received or after the microprocessor reads the receiver FIFO.
When the transmitter FIFO and THRE interrupt are enabled (FCR-0=1, IER-1=1), transmit interrupts occur as follows:

The occurrence of transmitter holding register empty interrupt is delayed one character time minus the last stop bit time when there have not been at least two bytes in the transmitter FIFO at the same time since the last time the transmitter FIFO was empty. It is cleared as soon as the transmitter holding register is written to (1 to 64 characters may be written to transmit FIFO while servicing this interrupt) or the IIR is read.

The first transmitter interrupt after changing FCR is immediate if it is enabled.

The transmitter empty indicator is delayed one character time when there has not been at least two bytes in the transmitter FIFO at the same time since the last time that TEMT=1. TEMT is set after the stop bit has been completely shifted out.

The transmitter FIFO empty indicator works the normal way in this mode and is not delayed. Character time-out and receiver FIFO trigger-level interrupts have the same priority as the current
Received data available interrupt.

Absolute Maximum Ratings

Supply Range	7 Volts
Voltage at any pin	GND – 0.3 to VCC +0.3
Operating Temperature	-45° C to 90° C
Storage Temperature	-65° C to 150° C
Package Dissipation	500 mW
ESD	± 2000 Volts
Latch up	220 mA

DC Electrical Specification

T = 0° C to 70° C (-40° C to +85° C for industrial “E” grade parts), VCC = 5V ± 10% unless otherwise specified.

Symbol	Parameter	5-V Min	5-V Max	Unit	Condition
Vil	Input Low voltage	-0.3	0.8	V	
Vih	Input High voltage	2.0		V	
Vt-	Schmitt trigger negative going threshold voltage	1.10		V	
Vt+	Schmitt trigger positive going threshold voltage	1.87		V	
Vol	Output low voltage		0.4	V	Iol=4 mA
Voh	Output high voltage	3.5		C	Ioh=4 mA
Iil	Input low current		±1	µA	
Iih	Input high current		±1	µA	
Ioz	Three state leakage current		±10	µA	
Cin	Input capacitance	3	5	pF	
Cout	Output capacitance	3	5	pF	
Icc	Operating current		60	mA	No load

Revision	Notes	Date
1.0	Corrections	10/01