# DATA SHEET

NEC

# MOS FIELD EFFECT TRANSISTOR
# NP100P06PDG

## SWITCHING
## P-CHANNEL POWER MOSFET

### DESCRIPTION

The NP100P06PDG is P-channel MOS Field Effect Transistor designed for high current switching applications.

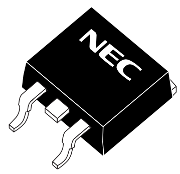
<R> **ORDERING INFORMATION**

| PART NUMBER | LEAD PLATING | PACKING | PACKAGE |
|---|---|---|---|
| NP100P06PDG-E1-AY [Note] | Pure Sn (Tin) | Tape 800 p/reel | TO-263 (MP-25ZP) |
| NP100P06PDG-E2-AY [Note] | | | |

**Note** Pb-free (This product does not contain Pb in external electrode.)

### FEATURES

(TO-263)




- Super low on-state resistance

  $R_{DS(on)1}$ = 6.0 mΩ MAX. ($V_{GS}$ = –10 V, $I_D$ = –50 A)

  $R_{DS(on)2}$ = 7.8 mΩ MAX. ($V_{GS}$ = –4.5 V, $I_D$ = –50 A)

- High current rating: $I_{D(DC)}$ = ∓100 A

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C)

| | | | |
|---|---|---|---|
| Drain to Source Voltage ($V_{GS}$ = 0 V) | $V_{DSS}$ | –60 | V |
| Gate to Source Voltage ($V_{DS}$ = 0 V) | $V_{GSS}$ | ∓20 | V |
| Drain Current (DC) ($T_C$ = 25°C) | $I_{D(DC)}$ | ∓100 | A |
| Drain Current (pulse) [Note1] | $I_{D(pulse)}$ | ∓300 | A |
| Total Power Dissipation ($T_C$ = 25°C) | $P_{T1}$ | 200 | W |
| Total Power Dissipation ($T_A$ = 25°C) | $P_{T2}$ | 1.8 | W |
| Channel Temperature | $T_{ch}$ | 175 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +175 | °C |
| Single Avalanche Current [Note2] | $I_{AS}$ | 64 | A |
| Single Avalanche Energy [Note2] | $E_{AS}$ | 420 | mJ |

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

**2.** Starting $T_{ch}$ = 25°C, $V_{DD}$ = –30 V, $R_G$ = 25 Ω, $V_{GS}$ = –20 → 0 V

### THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| Channel to Case Thermal Resistance | $R_{th(ch-C)}$ | 0.75 | °C/W |
| Channel to Ambient Thermal Resistance | $R_{th(ch-A)}$ | 83.3 | °C/W |




Document No. D18693EJ3V0DS00 (3rd edition)
Date Published May 2007 NS CP(K)
Printed in Japan



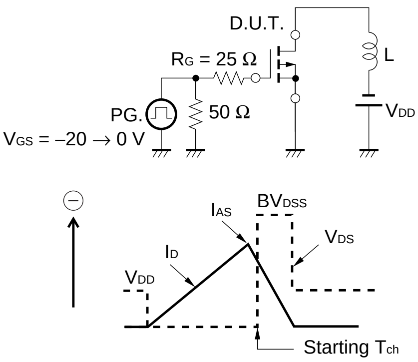

**The mark <R> shows major revised points.**
**The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.**

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C)

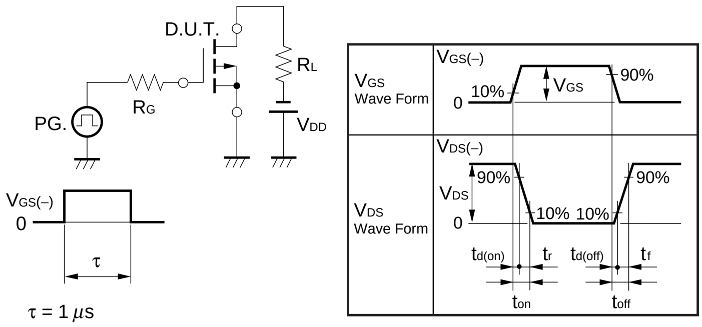
| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = –60 V, $V_{GS}$ = 0 V | | | –10 | μA |
| Gate Leakage Current | $I_{GSS}$ | $V_{GS}$ = ∓20 V, $V_{DS}$ = 0 V | | | ∓100 | nA |
| Gate to Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = –10 V, $I_D$ = –1 mA | –1.0 | –1.6 | –2.5 | V |
| Forward Transfer Admittance Note | $\| y_{fs} \|$ | $V_{DS}$ = –10 V, $I_D$ = –50 A | 43 | 86 | | S |
| Drain to Source On-state Resistance Note | $R_{DS(on)1}$ | $V_{GS}$ = –10 V, $I_D$ = –50 A | | 4.4 | 6.0 | mΩ |
| | $R_{DS(on)2}$ | $V_{GS}$ = –4.5 V, $I_D$ = –50 A | | 5.0 | 7.8 | mΩ |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = –10 V, | | 15000 | | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V, | | 1810 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 840 | | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$ = –30 V, $I_D$ = –45 A, | | 28 | | ns |
| Rise Time | $t_r$ | $V_{GS}$ = –10 V, | | 35 | | ns |
| Turn-off Delay Time | $t_{d(off)}$ | $R_G$ = 0 Ω | | 275 | | ns |
| Fall Time | $t_f$ | | | 100 | | ns |
| Total Gate Charge | $Q_G$ | $V_{DD}$ = –48 V, | | 300 | | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{GS}$ = –10 V, | | 35 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | $I_D$ = –100 A | | 85 | | nC |
| Body Diode Forward Voltage Note | $V_{F(S-D)}$ | $I_F$ = –100 A, $V_{GS}$ = 0 V | | 0.92 | 1.5 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = –100 A, $V_{GS}$ = 0 V, | | 67 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = –100 A/μs | | 135 | | nC |

**Note** Pulsed test PW ≤ 350 μs, Duty Cycle ≤ 2%

### TEST CIRCUIT 1 AVALANCHE CAPABILITY

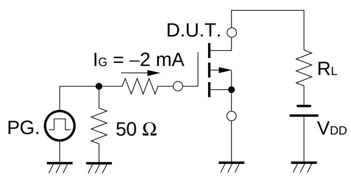



### TEST CIRCUIT 2 SWITCHING TIME



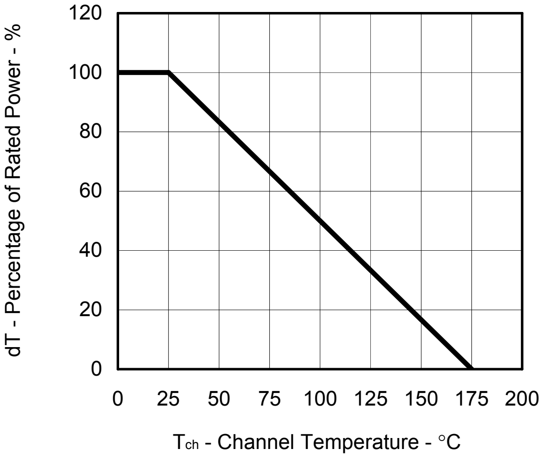

τ = 1 μs
Duty Cycle ≤ 1%

### TEST CIRCUIT 3 GATE CHARGE

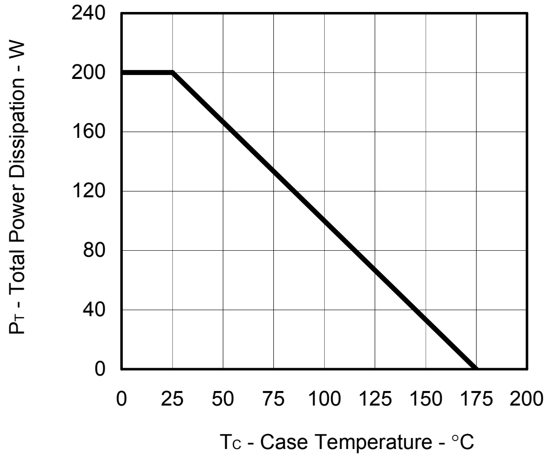


## TYPICAL CHARACTERISTICS ($T_A$ = 25°C)

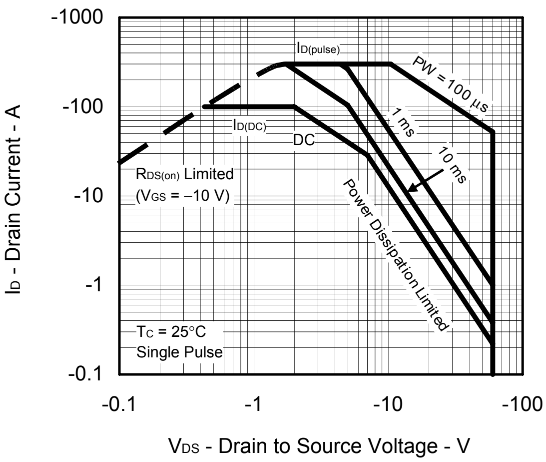
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



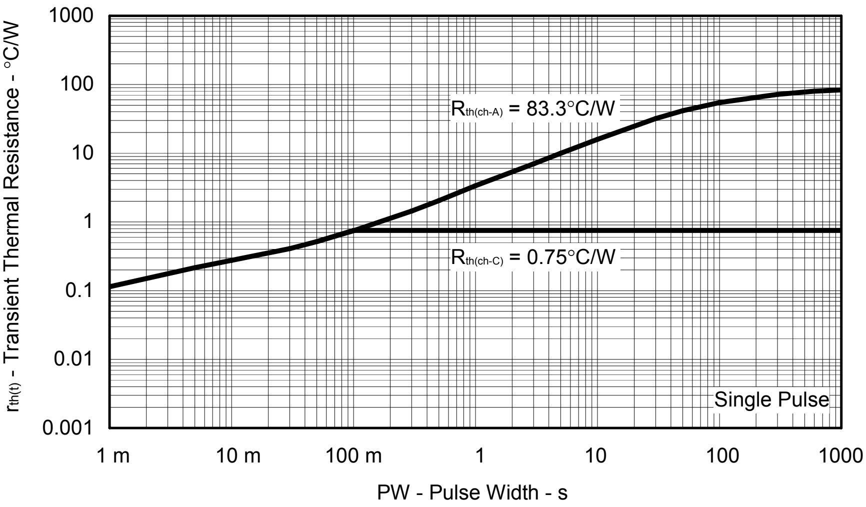

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



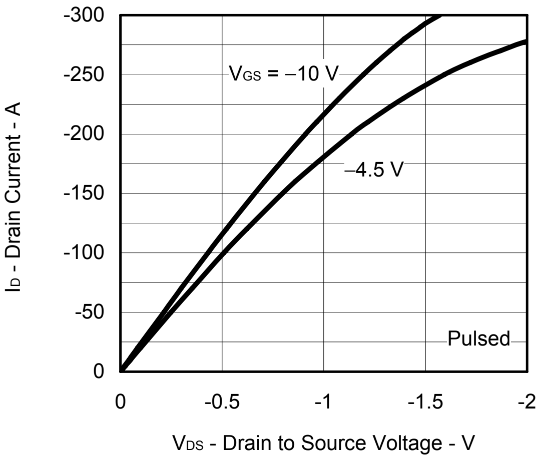

FORWARD BIAS SAFE OPERATING AREA



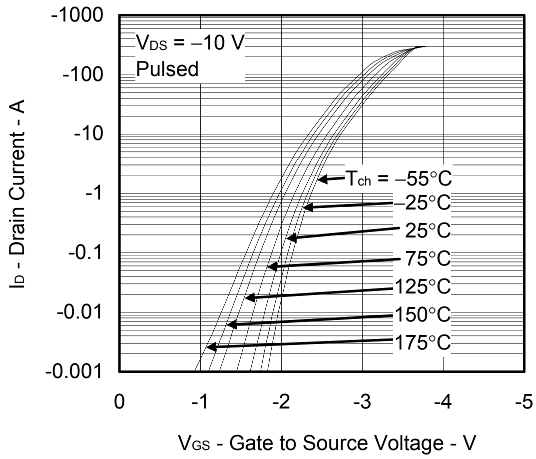

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



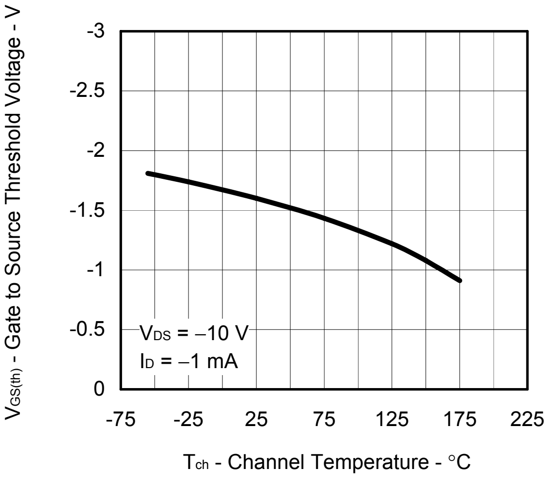
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



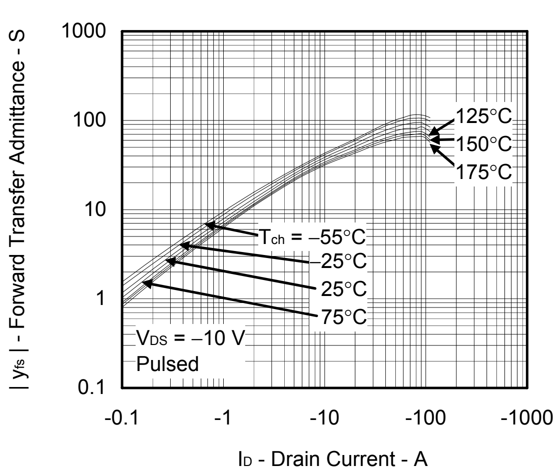

FORWARD TRANSFER CHARACTERISTICS



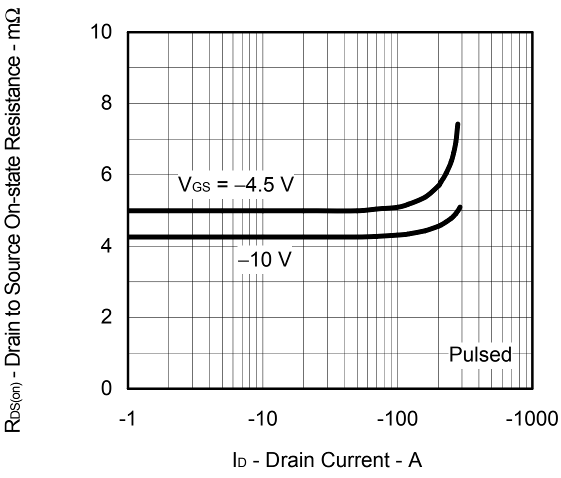

GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



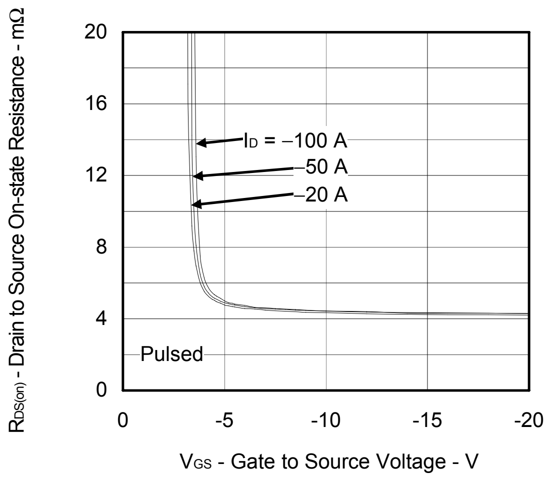

FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



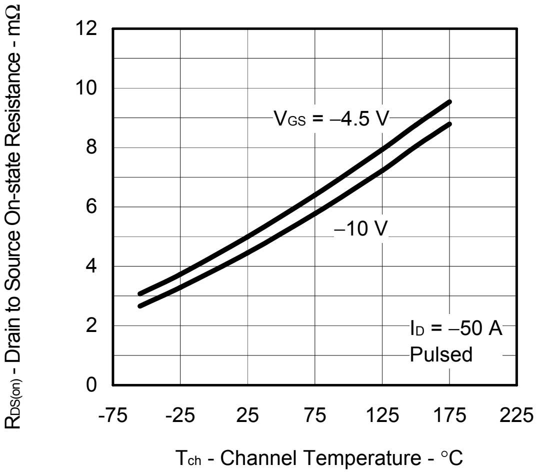

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



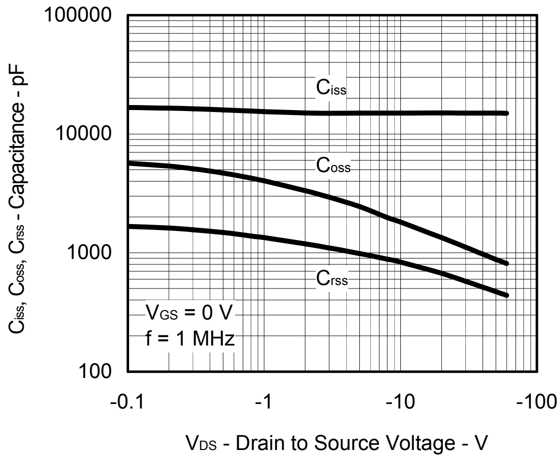

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



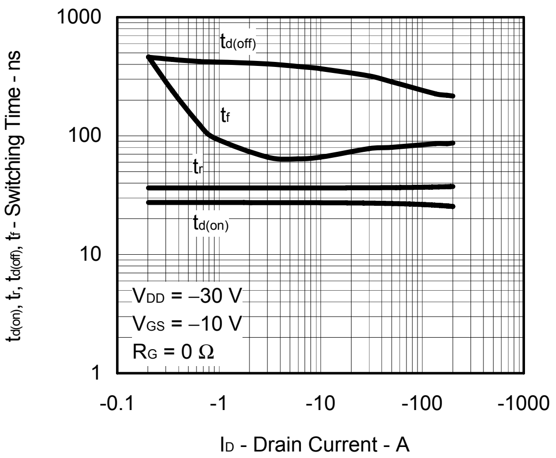
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



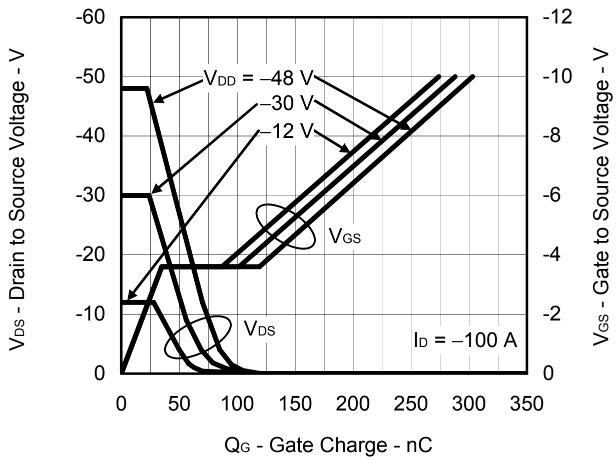

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



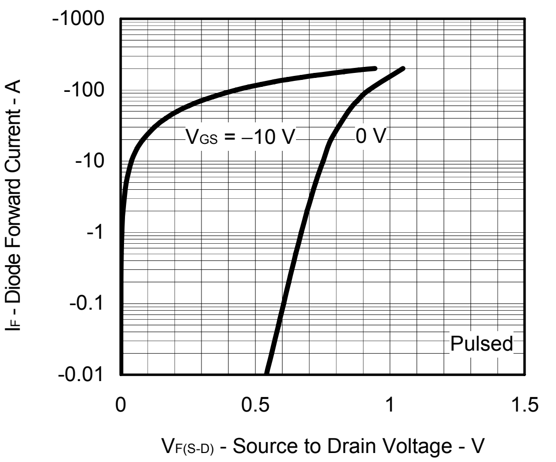

SWITCHING CHARACTERISTICS



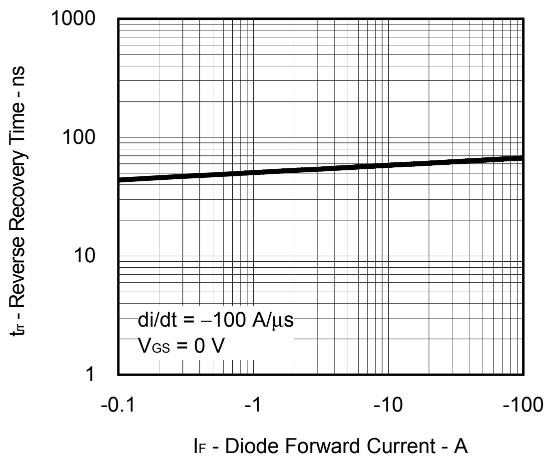

DYNAMIC INPUT/OUTPUT CHARACTERISTICS




SOURCE TO DRAIN DIODE FORWARD VOLTAGE

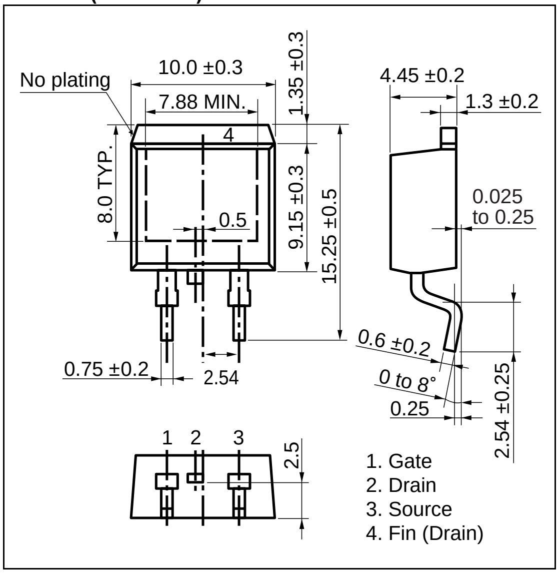



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

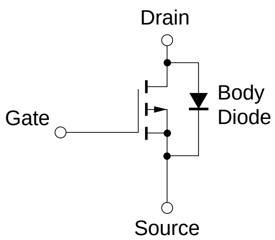


**PACKAGE DRAWING (Unit: mm)**

**TO-263 (MP-25ZP)**




**EQUIVALENT CIRCUIT**




**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.