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NTE7069
Integrated Circuit
2 Modulus High Speed Divider W/ECL Output
for Phase–Lock Loop (PLL) Synthesized TV Tuner

Description:

The NTE7069 is an integrated circuit consisting of a 1/128, 1/136 prescaler, high speed frequency divider using an ECL (emitter–coupled logic) circuit configuration in an 8–Lead SIP type package. When the clocks are applied to the pulse swallow control input terminal, M, the dividing ratio is 1/136, and when M is stable (“H” or “L”), the ratio is 1/128. This device operates in the frequency range of 80MHz to 1000MHz. Typical applications for the NTE7069 include prescalers for PLL (Phase Lock Loop) TV tuners and general use in consumer and industrial digital equipment.

Features:

- High–Speed Operation: f_{max} = 1GHz
- Operates at Low Input Amplitudes: –20dB Min
- ECL Level Output: 1.30$V_{P–P}$ Typ

Absolute Maximum Ratings: (T_A = –20° to +75°C unless otherwise specified)

Supply Voltage, V_{CC} . . . . . –0.3 to +7V
Input Voltage (T, $\overline{T}_{(REF)}$), V_I . . . . . 0 to V_{CC}
Power Dissipation (T_A = +25°C), P_D 1.15W
Operating Temperature Range, T_{opr} . . . . . –20° to +75°C
Storage Temperature Range, T_{stg} . . . . . –55° to +125°C

Recommended Operating Conditions: (T_A = –20° to +75°C unless otherwise specified)

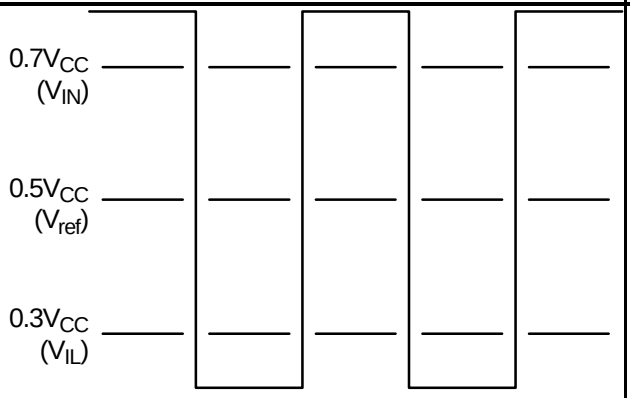
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5	5.0	6.6	V
Input Amplitude	V_{IN}	f_{IN} = 80 to 1000MHz	–20	–	4	dBm

Electrical Characteristics: (V_{CC} = 5V ±10%, T_A = –20° to +75°C unless otherwise specified)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Current		I_{CC}	V_{CC} = 5.5V, T_A = +25°C		–	33	50	mA
Input Sensitivity		V_{IN}	f_{IN} = 80 to 1000MHz		–20	–	4	dBm
Output Amplitude		V_O	V_{CC} = 4.5V, f_{IN} = 80 to 1000MHz		0.9	1.3	1.7	V_{P-P}
High Level Input Voltage	When the dividing ratio is 1/136	V_{IH}	M Terminal, Note 2		$0.7V_{CC}$	–	–	V
Low Level Input Voltage		V_{IL}			–	–	$0.3V_{CC}$	V
High Level Input Current		I_{IH}		V_{CC} = –5V, V_{IH} = 3.5V	–	–	50	µA
Low Level Input Current		I_{IL}		V_{CC} = –5V, V_{IL} = 1.5V	–	–	–160	µA

Note 1. Typical values are at V_{CC} = 5V, T_A = +25°C.

Note 2. Input conditions of pulse swallow control input terminal M:

Dividing Ratio	Input Conditions	Description
1/136		When the clocks are applied to M terminal as shown in the left figure, the dividing raito changes from 1/128 to 1/136
1/128	V_{IL} = 0V, V_{IN} = V_{CC} or V_{IN} = OPEN	M terminal is stable at GND or V_{CC}, or opened

Pin Connection Diagram
(Front View)