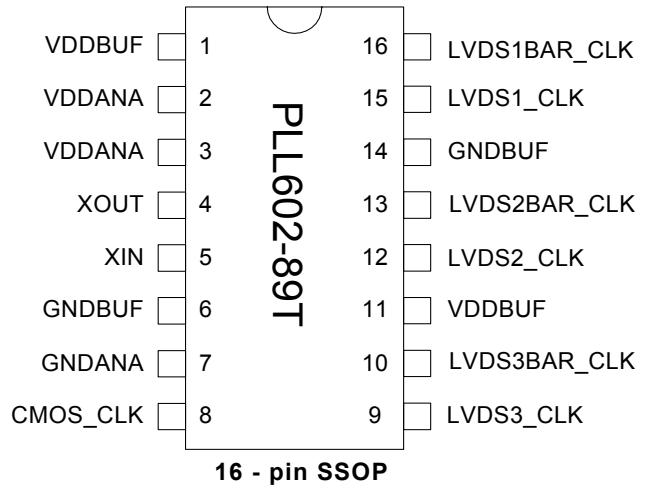


**12-27 MHz XO IC with 3 Pairs of LVDS and 1 CMOS Outputs**

**FEATURES**

- Low jitter XO for the 12MHz to 27MHz range.
- Integrated crystal load capacitor: no external load capacitor required.
- 3 pairs of LVDS outputs and 1 CMOS output.
- 12-27 MHz fundamental crystal input.
- Low jitter (RMS): 2.5 ps period jitter (1 sigma).
- 2.5V to 3.3V operation.
- Available in 16-Pin SSOP package.

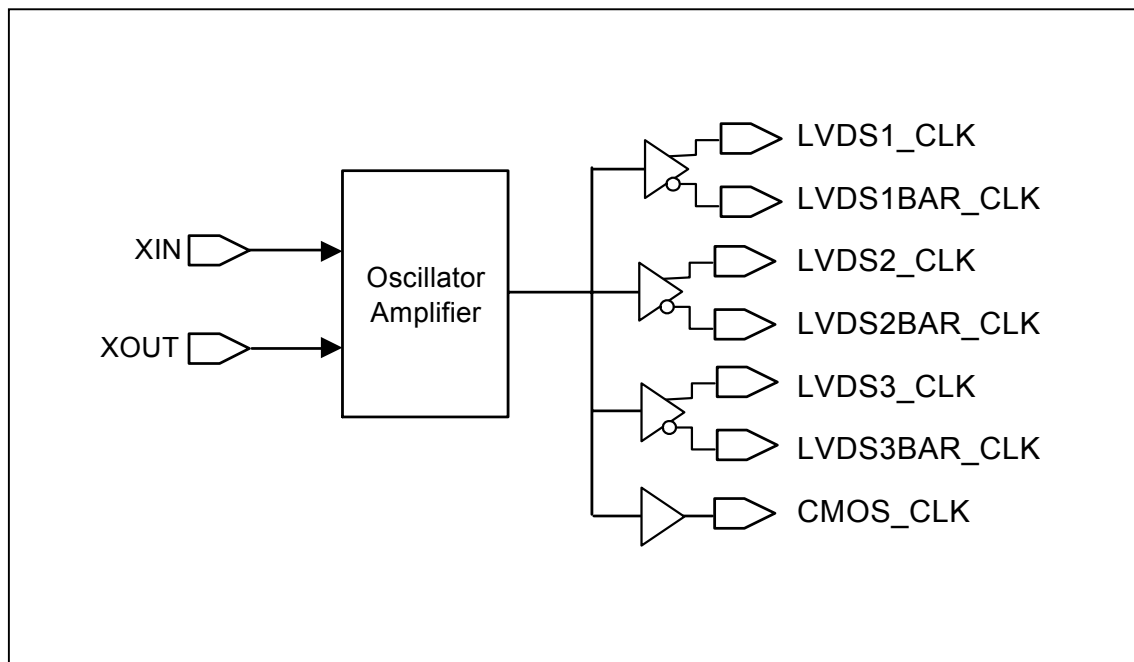
**PIN CONFIGURATION**  
(Top View)



**DESCRIPTION**

The PLL602-89T is a high performance multiple output XO IC chip. It provides 3 pairs of LVDS and 1 CMOS outputs. The chip combines a crystal oscillator (XO) with a multiple-output buffer. It accepts a low cost fundamental parallel resonant mode crystal from 12MHz to 27MHz, which is reproduced at the outputs. The very low jitter (2.5 ps RMS period jitter) makes this chip ideal for data and telecommunication applications.

**BLOCK DIAGRAM**



**12-27 MHz XO IC with 3 Pairs of LVDS and 1 CMOS Outputs**
**PIN DESCRIPTION**

Name	Pin Number	Type	Description
VDD	1,2,3,11	P	+3.3V VDD connection. VDDANA and VDDBUF should be decoupled separately.
XOUT	4	I	Crystal out connector. This is the output of the crystal oscillator circuitry. The crystal should be mounted as close to the IC as possible, with minimum parasitic capacitance.
XIN	5	I	Crystal in connector. This is the input of the crystal oscillator circuitry. The crystal should be mounted as close to the IC as possible, with minimum parasitic capacitance.
GND	6,7,14	P	Ground connection.
CMOS_CLK	8	O	CMOS output signal.
LVDS3_CLK	9	O	LVDS output.
LVDS3BAR_CLK	10	O	LVDS complementary output.
LVDS2_CLK	12	O	LVDS output.
LVDS2BAR_CLK	13	O	LVDS complementary output.
LVDS1_CLK	15	O	LVDS output.
LVDS1BAR_CLK	16	O	LVDS complementary output.

**ELECTRICAL SPECIFICATIONS**
**1. Absolute Maximum Ratings**

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		4.6	V
Input Voltage, dc	$V_I$	-0.5	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	-0.5	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature*	$T_A$	-40	85	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

\* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

**2. Crystal Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	$F_{XIN}$	Parallel Fundamental Mode	12		27	MHz
Crystal Loading Rating	$C_L$ (xtal)			21.5		pF
Recommended ESR	$R_E$				30	$\Omega$

**12-27 MHz XO IC with 3 Pairs of LVDS and 1 CMOS Outputs**
**3. General Electrical Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Operating Voltage	$V_{DD}$		2.25		3.63	V	
Supply Current, Dynamic (with Loaded Outputs)	$I_{DD}$	CMOS outputs loaded with 15pF, LVDS outputs loaded with 100 $\Omega$	$F_{out} = 12$ MHz		15	20	mA
			$F_{out} = 25$ MHz		20	25	
Short Circuit Current				$\pm 50$		mA	

**4. AC Electrical Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency			12		27	MHz
Output Clock Rise Time	$t_r$	0.8V ~ 2.0V with 10 pF load			1.5	ns
	$t_r$	0.3V ~ 3.0V with 15 pF load		2	5	
Output Clock Fall Time	$t_f$	2.0V ~ 0.8V with 10 pF load			1.5	
	$t_f$	3.0V ~ 0.3V with 15pF load		2	5	
Output Clock Duty Cycle		Measured @ 1.25 V (LVDS)	45	50	55	%
		Measured @ 50% $V_{DD}$ (CMOS)	45	50	55	

**5. Jitter Specifications**

PARAMETERS	CONDITIONS	FREQUENCY	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	With capacitive decoupling between VDD and GND.	25MHz		2.5	4	ps
Peak to Peak jitter	With capacitive decoupling between VDD and GND. Over 10,000 cycles.	25MHz		18	30	ps

**6. CMOS Output Electrical Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output High Voltage	$V_{OH}$	$I_{OH} = -12$ mA	2.4			V
Output Low Voltage	$V_{OL}$	$I_{OL} = 12$ mA			0.4	V
Output High Voltage at CMOS level	$V_{OHC}$	$I_{OH} = -4$ mA	$V_{DD} - 0.4$			V
Output drive current		At TTL level	10			mA

**7. CMOS Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Clock Rise/Fall Time (Standard Drive)		0.8V ~ 2.0V with 10 pF load		1.15		ns
		0.3V ~ 3.0V with 15 pF load		2.4		

**12-27 MHz XO IC with 3 Pairs of LVDS and 1 CMOS Outputs**

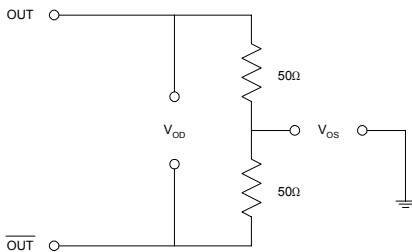
**8. LVDS Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	$V_{OD}$	$R_L = 100 \Omega$ (see figure)	247	355	454	mV
$V_{DD}$ Magnitude Change	$\Delta V_{OD}$		-50		50	mV
Output High Voltage	$V_{OH}$			1.4	1.6	V
Output Low Voltage	$V_{OL}$		0.9	1.1		V
Offset Voltage	$V_{OS}$		1.125	1.2	1.375	V
Offset Magnitude Change	$\Delta V_{OS}$		0	3	25	mV
Power-off Leakage	$I_{OXD}$	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		$\pm 1$	$\pm 10$	$\mu A$
Output Short Circuit Current	$I_{OSD}$			-5.7	-8	mA

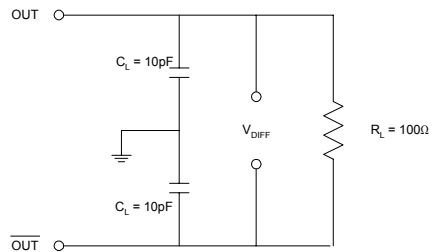
**9. LVDS Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	$t_r$	$R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	$t_f$		0.2	0.7	1.0	ns

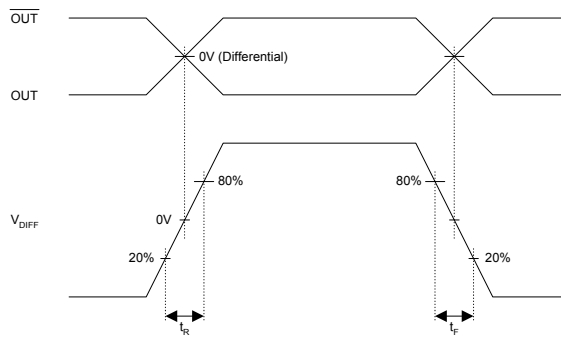
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform



**12-27 MHz XO IC with 3 Pairs of LVDS and 1 CMOS Outputs**

**PACKAGE INFORMATION**

16 PIN SSOP ( inch )			
	SSOP		
Symbol	Min.	Nom.	Max.
A	.053	.064	.069
A1	.004	.006	.010
B	.008	-	.012
C	.007	-	.010
D	.189	.193	.197
E	.150	.154	.157
H	.228	.236	.244
L	.016	.025	.050
e	.025 BASIC		

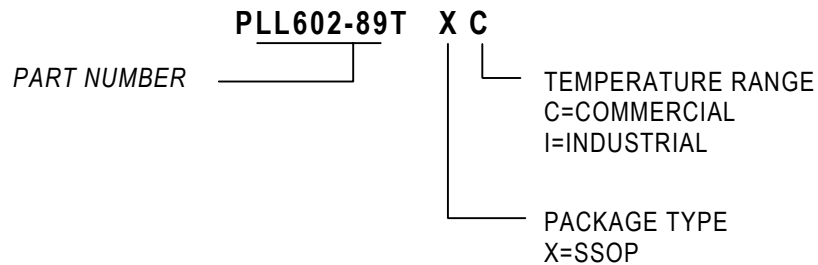
**ORDERING INFORMATION**

**For part ordering, please contact our Sales Department:**

47745 Fremont Blvd., Fremont, CA 94538, USA  
Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:  
Device number, Package type and Operating temperature range



<b>Order Number</b>	<b>Marking</b>	<b>Package Option</b>
PLL602-89TXC-R	P602-89T XC	SSOP - Tape and Reel
PLL602-89TXC	P602-89T XC	SSOP - Tube

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