PA17

PRELIMINARY

FEATURES

- **HIGH INTERNAL DISSIPATION — 850 WATTS**
- **HIGH VOLTAGE, HIGH CURRENT — 200V 50A CONTINUOUS, 100A PULSE**
- **HIGH SLEW RATE — 50V/μS**
- **4 WIRE CURRENT LIMIT SENSING**
- **EXTERNAL SHUT DOWN CONTROL**
- **OPTIONAL BOOST VOLTAGE INPUTS**

APPLICATIONS

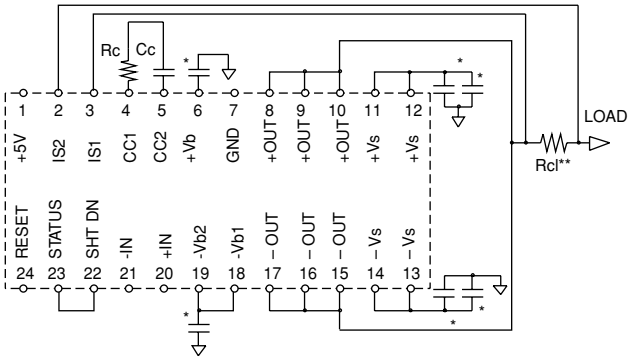
- **SEMI CONDUCTOR TESTING**
- **SONAR TRANSDUCER DRIVER**
- **LINEAR AND ROTARY MOTOR DRIVES**
- **YOKE/MAGNETIC FIELD EXCITATION**

DESCRIPTION

The PA17 is a high voltage MOSFET power operational amplifier that extends the performance limits of power amplifiers in slew rate and power bandwidth, while maintaining high current and power dissipation ratings.

The PA17 is a highly flexible amplifier. The shutdown feature allows ultra-low quiescent current for standby operation or load protection by disabling the entire amplifier. Boost voltage inputs allow the small signal portion of the amplifier to operate at a higher voltage than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high currents for extra efficient operation. External compensation tailors performance to user needs. A four wire sense technique allows current limiting without the need to consider internal or external milliohm parasitic resistance in the output line.

EXTERNAL CONNECTIONS

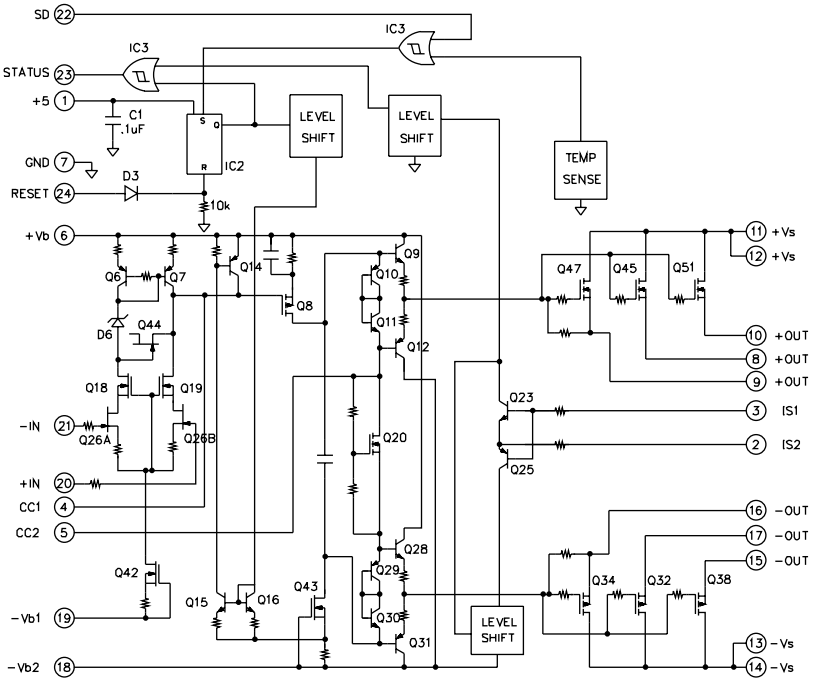


PHASE COMPENSATION

GAIN	Rc	Cc
1	100	470pF
>3	SHORT	220pF
>10	SHORT	100pF
100	SHORT	10pF

PIN SIDE VIEW
* BYPASSING OF SUPPLIES IS REQUIRED
** SEE TEXT FOR OTHER CURRENT LIMIT CONNECTIONS

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V
BOOST VOLTAGE	$\pm V_S$±20V
OUTPUT CURRENT, within SOA	100A
POWER DISSIPATION, internal	850W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_B$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–25 to +85°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			5	10	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		30	50	µV/°C
OFFSET VOLTAGE, vs. supply			15		µV/V
BIAS CURRENT, initial			10	50	pA
BIAS CURRENT, vs. supply			.01		pA/V
OFFSET CURRENT, initial			10	50	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE	Full temperature range	$\pm V_B \mp 10$			V
COMMON MODE REJECTION, DC	Full temp. range, V_{CM} = ±20V	86	98		dB
INPUT NOISE	100kHz BW, R_S = 1KΩ		10		µVrms
GAIN					
OPEN LOOP, @ 15Hz	Full temperature range, C_C = 100pF	94	102		dB
GAIN BANDWIDTH PRODUCT	I_O = 10A		2		MHz
POWER BANDWIDTH	R_L = 4.5Ω, V_O = 180V p-p		90		kHz
PHASE MARGIN	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING[5]	I_O = 50A	$\pm V_S \mp 8.8$	$\pm V_S \mp 7.5$		V
VOLTAGE SWING[5]	$\pm V_B = \pm V_S \pm 10V$, I_O = 50A	$\pm V_S \mp 6.8$	$\pm V_S \mp 5.5$		V
CURRENT, peak[5]		100			A
SETTLING TIME to .1%			2.5		µs
SLEW RATE	C_C= 100pF	40	50		V/µs
CAPACITIVE LOAD	A_V = +1	10			nF
POWER SUPPLY					
VOLTAGE	Full temperature range	±15	±75	±100	V
CURRENT, quiescent, boost supply				30	mA
CURRENT, quiescent, total				120	mA
CURRENT, quiescent, total, shutdown	Full temperature range			22	mA
THERMAL					
RESISTANCE, AC, junction to case[3]	Full temperature range, F>60Hz			.1	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F<60Hz			.15	°C/W
RESISTANCE[4], junction to air	Full temperature range		10		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25		85	°C

NOTES
1. Unless otherwise noted: T_C = 25°C. DC input specifications are ± value given. Power supply voltage is typical rating. ±VB= $\pm V_S$, Cc = 470pF, Rc=100Ω.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
4. The PA17 must be used with a heatsink or the quiescent power may drive the unit to junction temperatures higher than 150°C.
5. Parameter guaranteed but not tested.

CAUTION The PA17 is constructed from MOSFET transistors. ESD handling procedures must be observed.

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

The positive and negative outputs of the PA17 must be connected together by the user. However, the fact that multiple pins share the output current allows for some unusual current limit schemes not found in amplifiers with a single output pin.

Three pins each in the positive and negative outputs share the output current of the PA17. Pins 8 and 10 of the positive output and pins 15 and 17 of the negative output each carry approximately 25% of the output current. Pin 9 of the positive output and pin 16 of the negative output carry the remaining 50% of the output current .

For the current limit to operate correctly pin 3 (IS1) must be connected to the amplifier output side and pin 2 (IS2) connected to the load side of the current limit resistor Rcl, as shown in Figure 1. But Rcl may be connected to sample only a fraction of the output current. With this method the current limit resistor consumes less power and only slightly lowers the overall accuracy of the current limit set point. Figure 1, shows a circuit that samples only 25% of the output current. Only those pins necessary to illustrate the current limit function are shown in Figure 1.

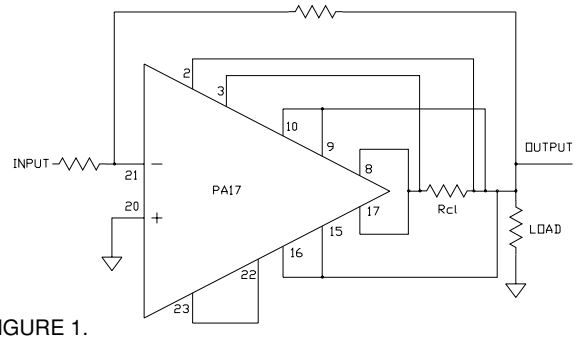


FIGURE 1.

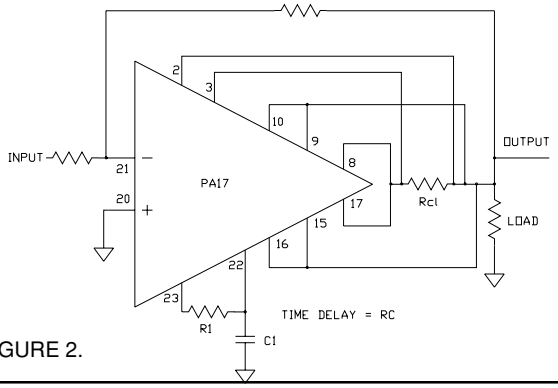


FIGURE 2.

In addition, the current limit of the PA17 operates differently than other Apex linear power amplifiers in that the output current is not clamped at the current limit set point. Instead, when an over-current condition is detected the PA17 sets STATUS (pin 23) high. This flag can alert external circuitry to do a variety of things to deal with this fault condition. For example, when STATUS is connected directly to SD (pin 22) the output stage of the PA17 is disabled until RESET (pin 24) is toggled high (Figure 1). Another possibility would be to connect STATUS to the SD pin via a RC circuit to delay the shutdown of the output stage (Figure 2). This technique would be useful if a short-term overload is normally expected that does not exceed the safe operating area of the PA17. In still another variation STATUS could trigger an external timer that would periodically reset the PA17 until the fault is cleared.

STATUS, SHUTDOWN AND RESET FUNCTIONS

The 5V logic section of the PA17 provides control and monitoring functions. The PA17 is protected from thermal overloads by directly measuring the temperature of the output transistors. When a thermal overload is detected the output stage is latched off and the STATUS output goes high, indicating an alarm condition. A high on the RESET pin resets the output stage. A high on the SHUTDOWN pin will also latch the output stage off and forces the STATUS pin high. The SHUTDOWN pin can be used to put the PA17 in a standby mode to lower the quiescent current and standby power dissipation. A thermal overload immediately latches off the output stage and cannot be delayed by external circuitry.

BOOST OPERATION

With the V_{BOOST} feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_{BOOST}$ (pin 6) and $-V_{BOOST}$ (pins 18, 19) are connected to the small signal circuitry of the amplifier. $+V_S$ (pins 11,12) and $-V_S$ (pins 13, 14) are connected to the high current output stage. An additional 10V on the V_{BOOST} pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swings to the supply rails is not required the $+V_{BOOST}$ and $+V_S$ pins must be strapped together as well as the $-V_{BOOST}$ and $-V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

COMPENSATION

The external compensation components C_C and R_C are connected to pins 4 and 5. Unity gain stability can be achieved at any compensation capacitance greater than 330 pF with at least 60 degrees of phase margin. At higher gains more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C and R_C for the application.

