## Applications

- Bluetooth[tm] Class 1
- USB Dongles
- Laptops
- Access Points
- Cordless Piconets
- Flip chip and chip-on-board applications

## Features

- +22.5 dBm at 47% Power Added Efficiency
- Low current 80 mA typical @ Pout=+20 dBm
- Temperature stability better than 1dB
- Power-control and Power-down modes
- -40C to +85C temperature range
- Gold bump bare die (0.63mm x 0.96mm)

## Ordering Information

| Part | Package | Shipping Method |
|---|---|---|
| PA2423G | Gold bump bare die | Diced wafer<br>Waffle pack |
| PA2423G-EV | Evaluation kit | |

## Product Description

A monolithic, high-efficiency, silicon-germanium power amplifier IC, the PA2423G is designed for Class 1 Bluetooth[tm] 2.4 GHz radio applications. It delivers +22.5 dBm output power with 47% power-added efficiency – making it capable of overcoming insertion losses of up to 2.5 dB between amplifier output and antenna input in Class 1 Bluetooth[tm] applications.

The amplifier features:

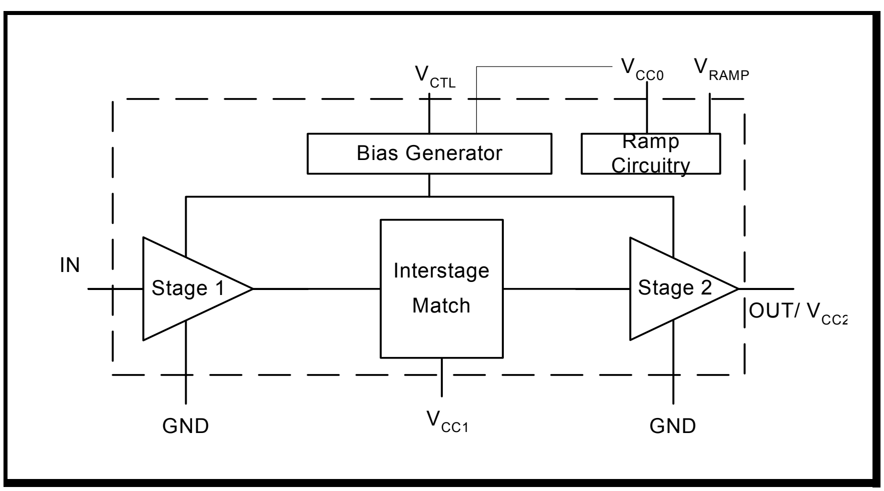
- an analog control input for improving PAE at reduced output power levels;
- a digital control input for controlling power up and power down modes of operation.

An on-chip ramping circuit corrects the turn-on/off switching of amplifier output with less than 3 dB overshoot, meeting the Bluetooth[tm] specification 1.1.

The PA2423G operates at 3.3V DC. At typical output power level (+22.5 dBm), its current consumption is 120 mA.

The silicon/silicon-germanium structure of the PA2423G provides high thermal conductivity and a subsequently low junction temperature. This device is capable of operating at a duty cycle of 100 percent.

## Functional Block Diagram



## Pad Description

For reference of pad numbers to the package drawings, see pages 4 and 5.

| Number | Name | Description | Pad Coordinate, Center of Pad (lower left corner is (0.0)) |
|---|---|---|---|
| 1 | IN | PA input | X = 192µm ± 10µm, Y = 315µm ± 10µm |
| 2 | VRAMP | PA enable/disable control input | X = 192µm ± 10µm, Y = 515µm ± 10µm |
| 3 | GND1 | Ground | X = 352µm ± 10µm, Y = 515µm ± 10µm |
| 4 | VCTL | Output power level control | X = 512µm ± 10µm, Y = 515µm ± 10µm |
| 5 | GND2 | Ground | X = 672µm ± 10µm, Y = 515µm ± 10µm |
| 6 | GND3 | Ground | X = 832µm ± 10µm, Y = 515µm ± 10µm |
| 7 | OUT/VCC2 | PA output and stage2 collector supply voltage | X = 752µm ± 10µm, Y = 315µm ± 10µm |
| 8 | GND4 | Ground | X = 832µm ± 10µm, Y = 115µm ± 10µm |
| 9 | GND5 | Ground | X = 672µm ± 10µm, Y = 115µm ± 10µm |
| 10 | VCC1 | Stage1 collector supply voltage | X = 512µm ± 10µm, Y = 115µm ± 10µm |
| 11 | GND6 | Ground | X = 352µm ± 10µm, Y = 115µm ± 10µm |
| 12 | VCC0 | Ramp supply voltage | X = 192µm ± 10µm, Y = 115µm ± 10µm |

## Absolute Maximum Ratings

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| VCC | Supply Voltage | -0.3 | +3.6 | V |
| VCTL | Control Voltage | -0.3 | $V_{CC}$ | V |
| VRAMP | Ramping Voltage | -0.3 | $V_{CC}$ | V |
| IN | RF Input Power | | +8 | dBm |
| TA | Operating Temperature Range | -40 | +85 | °C |
| TSTG | Storage Temperature Range | -40 | +150 | °C |
| Tj | Maximum Junction Temperature | | +150 | °C |

Operation in excess of any one of the above Absolute Maximum Ratings may result in permanent damage. This device is a high performance RF integrated circuit with EST rating < 600V and is ESD sensitive. Handling and assembly of this device should be at ESD protected workstations.

## DC Electrical Characteristics

Conditions: $V_{CC0} = V_{CC1} = V_{CC2} = V_{RAMP}$ = 3.3V, $V_{CTL}$ = 3.3V, $P_{IN}$ = +2dBm, $T_A$ = 25°C, f = 2.45GHz,
Input and Output externally matched to 50Ω ,unless otherwise noted.

| Symbol | Note | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| $I_{CC}$ | 1 | Supply Current ($I_{CC} = I_{VCC0} + I_{VCC1} + I_{VCC2}$ ) | | 120 | 150 | mA |
| $\Delta ICC_{temp}$ | 3 | Supply Current variation over temperature, (-40°C < $T_A$ <+85°C) | | 25 | | % |
| $V_{CTL}$ | | PA Output Power Control Voltage Range | 0 | | $V_{CC}$ | V |
| $I_{CTL}$ | 1 | Current sourced by $V_{CTL}$ Pin | | 200 | 250 | µA |
| $V_{RAMP}$ | 3 | Logic High Voltage | 2.0 | | | V |
| | 3 | Logic Low Voltage | | | 0.8 | V |
| $I_{stby}$ | 1 | Leakage Current when $V_{RAMP}$ = 0V | | 0.5 | 10 | µA |

## AC Electrical Characteristics

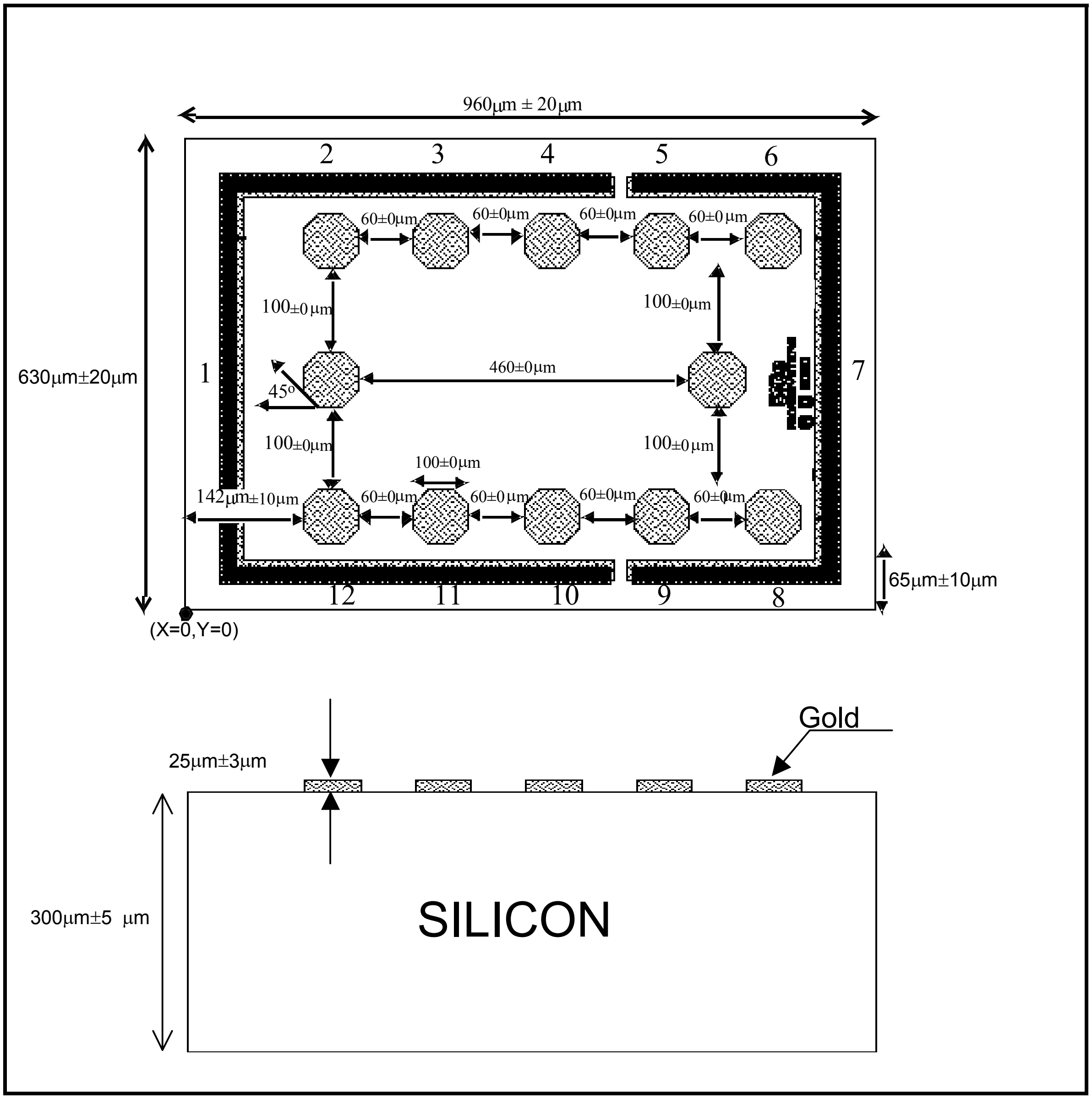
Conditions: $V_{CC0} = V_{CC1} = V_{CC2} = V_{RAMP}$ =3.3V, $V_{CTL}$ =3.3V, $P_{IN}$ =+2 dBm, $T_A$ =25°C, f = 2.45GHz,
Input and Output externally matched to 50Ω, unless otherwise noted

| Symbol | Note | Parameter | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{L-U}$ | 3 | Frequency Range | 2400 | | 2500 | MHz |
| $P_{OUT}$ | 1 | Output Power @ $P_{IN}$ =+2 dBm, $V_{CTL}$ = 3.3V | 20.0 | 22.5 | 23.5 | dBm |
| | 1 | Output Power @ $P_{IN}$ =+2 dBm, $V_{CTL}$ =0.4V | | -8 | 0 | dBm |
| $\Delta P_{TEMP}$ | 3 | $P_{OUT}$ variation over temperature (-40°C < $T_A$ <+85°C), $V_{CTL}$ =3.3V | | 1 | 2 | dB |
| $dP_{OUT}/dV_{CTL}$ | 3 | Control Voltage Sensitivity | | 60 | 120 | dBm/V |
| PAE | | Power Added Efficiency at +22.5 dBm Output Power | | 47 | | % |
| $G_{VAR}$ | 3 | Gain Variation over band (2400-2500 MHz) | | 0.7 | 1 | dB |
| 2f, 3f, 4f, 5f | 3,4 | Harmonics | | -35 | -30 | dBc |
| $\lvert S_{21}\rvert_{OFF}$ | 2 | Isolation in "OFF" State, $P_{IN}$ =+2dBm, $V_{RAMP}$ =0V | 20 | 25 | | dB |
| $\lvert S_{12}\rvert$ | 2 | Reverse Isolation | 32 | 42 | | dB |
| STAB | 2 | Stability ($P_{IN}$ = +2dBm, Load VSWR = 6:1) | All non-harmonically related outputs less than -50 dBc | | | |

**Notes:** (1) Guaranteed by production test at $T_A$ =25°C.
(2) Guaranteed by design only.
(3) Guaranteed by design and characterization.
(4) Harmonic levels are greatly affected by topology of external matching networks.
(5) RF characteristics specified above are for direct die attach (Flip-chip) on SiGe Applications Board. For wire bonded applications there may be some degradation in performance due to effects of bond wires and interconnect.

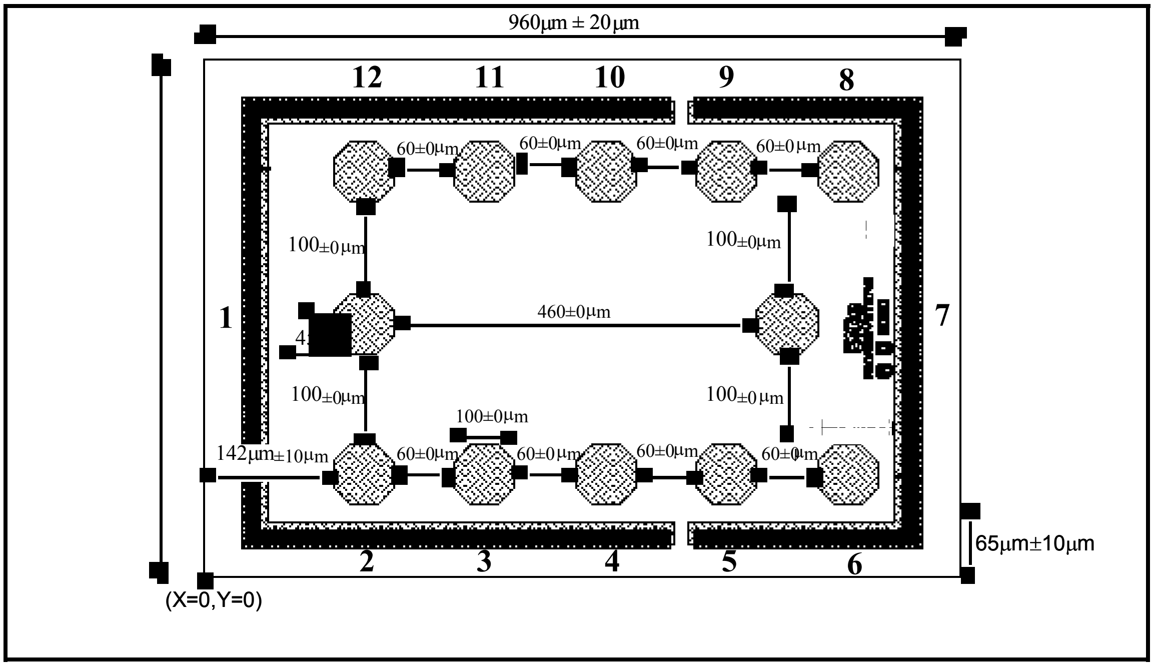
## Gold Bump Bare Die - Top and Side Views

The first drawing provides the top view of the gold bump bare die (gold bumps on top surface). This view should be used for the chip-on-board mounting. The second drawing illustrates the side view of the die.



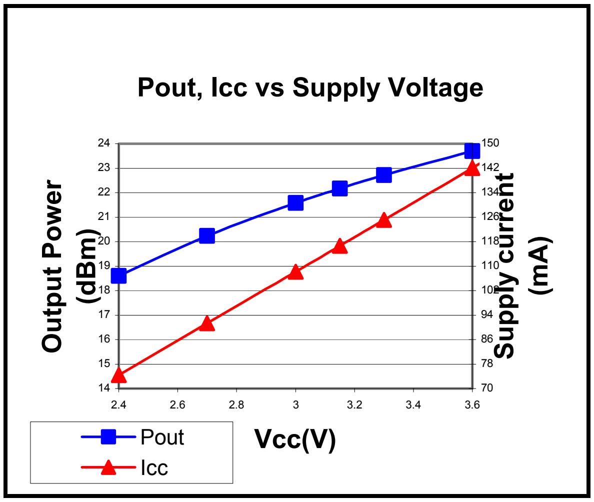
## Gold Bump Bare Die – Bottom View

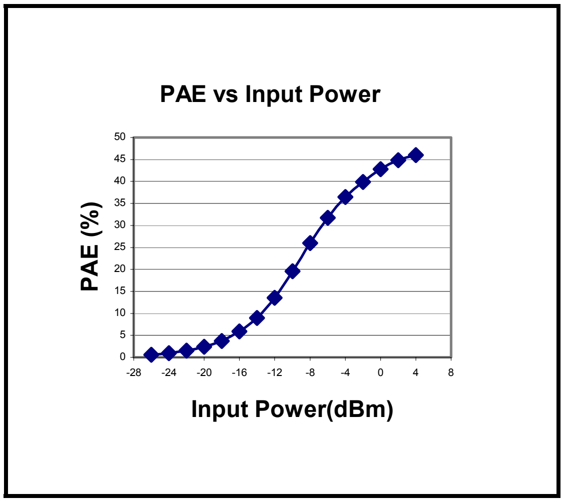
This drawing shows the gold bump bare die when viewed from the bottom of the die (without gold bumps). This view and pintout orientation should be used for flip chip mounting – top surface of die (with gold bumps) is inverted to make contact with PCB.

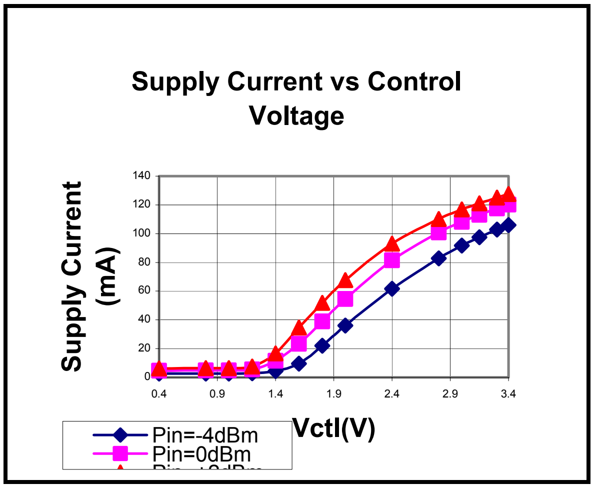


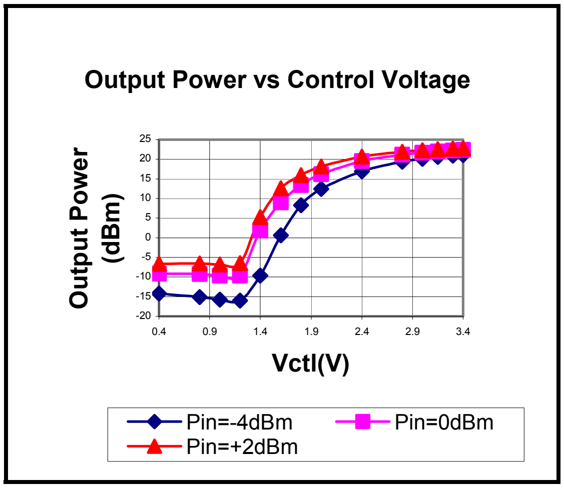
## Typical Performance Characteristics

SiGe PA2423G-EV evaluation board, $V_{CC0}$=$V_{CC1}$=$V_{CC2}$=$V_{RAMP}$=3.3V, $V_{CTL}$ = 3.3V, $P_{IN}$ = +2 dBm, $T_A$ = 25°C, f = 2.45GHz, Input and Output externally matched to 50Ω, unless otherwise noted)

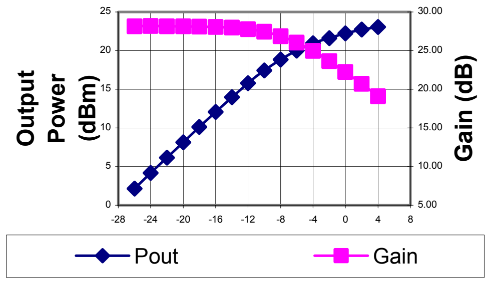


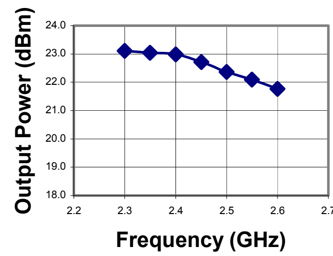



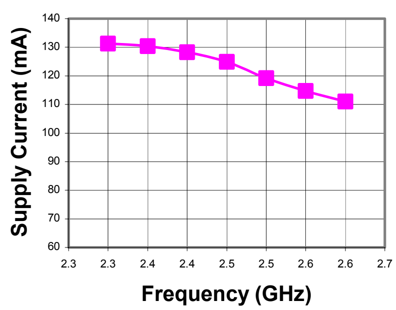
**Output Power, Gain vs Input Power**



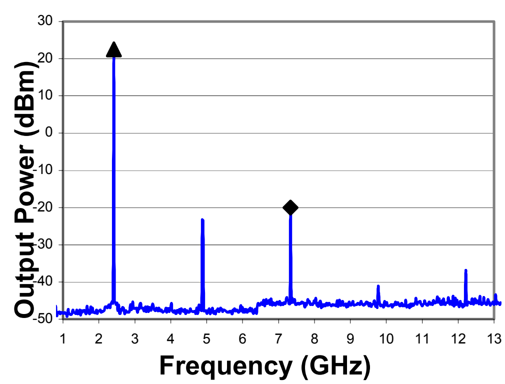

**Pout vs Frequency**



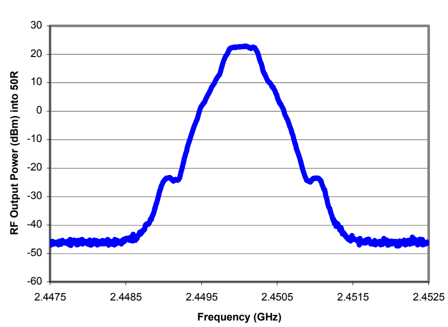

**Icc vs Frequency**




**Harmonic Output Spectrum**




**PA output spectrum with BT modulated signal**



## Applications Information

For test and design purposes, SiGe Semiconductor offers an evaluation board for the PA2423G. The order part number is PA2423G-EV. The evaluation board is intended to simplify the testing with respect to RF performance of this power amplifier.

The application note, 05AN007 provides the supporting information for using the evaluation board. It contains information on the schematic, bill of materials and recommended layout for the power amplifier and the input and output matching networks. To assist in the design process, this layout is available, upon request, in gerber file format.

**Using $V_{RAMP}$**

$V_{RAMP}$ is a digital pin used to power-up and power-down the PA2423G in Time Duplex systems such as Bluetooth$^{tm}$ 1.1. During receive mode, $V_{RAMP}$ voltage is pulled down, PA2423G acts as a 25 dB isolation block between the radio and the antenna while consuming a modest 1uA. In transmit mode, $V_{RAMP}$ voltage is pulled to VCC and PA2423G offers 19 dB to 21dB of large signal gain. The rise and fall time are in the order of 1-2usec.

**Using $V_{CTL}$**

$V_{CTL}$ is an analog pin that is designed to control the gain of PA2423G. Applying a voltage between 0V and Vcc will adjust the gain between -15dB and 21 dB. Used in combination with a variable drive level to PA2423G, the $V_{CTL}$ function can greatly optimize the PAE of the system at all four Bluetooth$^{tm}$ transmitted power levels.

By applying approximately 1.4V to $V_{CTL}$, for example, a Class1 radio can be modified to a Class2 radio with the PA2423G consuming only 15mA.

By implementing a resistor DAC, the $V_{CTL}$ pin can interface with Bluetooth$^{tm}$ transceivers offering digital and programmable outputs.

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