ELPIDA

DATA SHEET

288M bits Direct Rambus DRAM

μPD488588 (512K words × 18 bits × 32s banks)

Description

The Direct Rambus DRAM (Direct RDRAM) is a general purpose high-performance memory device suitable for use in a broad range of applications including computer memory, graphics, video, and any other application where high bandwidth and low latency are required.

The μPD488588 is 288Mbits Direct Rambus DRAM (RDRAM®), organized as 16M words by 18 bits.

The use of Rambus Signaling Level (RSL) technology permits 600MHz to 800MHz transfer rates while using conventional system and board design technologies. Direct RDRAM devices are capable of sustained data transfers at 1.25ns per two bytes (10ns per sixteen bytes).

The architecture of the Direct RDRAMs allows the highest sustained bandwidth for multiple, simultaneous randomly addressed memory transactions.
The separate control and data buses with independent row and column control yield over 95% bus efficiency. The Direct RDRAM's four banks support up to four simultaneous transactions.

System oriented features for mobile, graphics and large memory systems include power management, byte masking.

The μPD488588 is offered in a CSP horizontal package suitable for desktop as well as low-profile add-in card and mobile applications. Direct RDRAMs operate from a 2.5V supply.

Features

- Highest sustained bandwidth per DRAM device
  - — 1.6 GB/s sustained data transfer rate
  - — Separate control and data buses for maximized efficiency
  - — Separate row and column control buses for easy scheduling and highest performance
  - — 32 banks: four transactions can take place simultaneously at full bandwidth data rates
- Low latency features
  - — Write buffer to reduce read latency
  - — 3 precharge mechanisms for controller flexibility
  - — Interleaved transactions
- Advanced power management:
  - — Multiple low power states allows flexibility in power consumption versus time to active state
  - — Power-down self-refresh
- Overdrive current mode
- Organization: 2K bytes pages and 32 banks, x 18
- Uses Rambus Signaling Level (RSL) for up to 800MHz operation
- Package : 80-ball FBGA (μBGA®) (17.16 × 10.2)

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Elpida Memory, Inc. is a joint venture DRAM company of NEC Corporation and Hitachi, Ltd.

Ordering Information

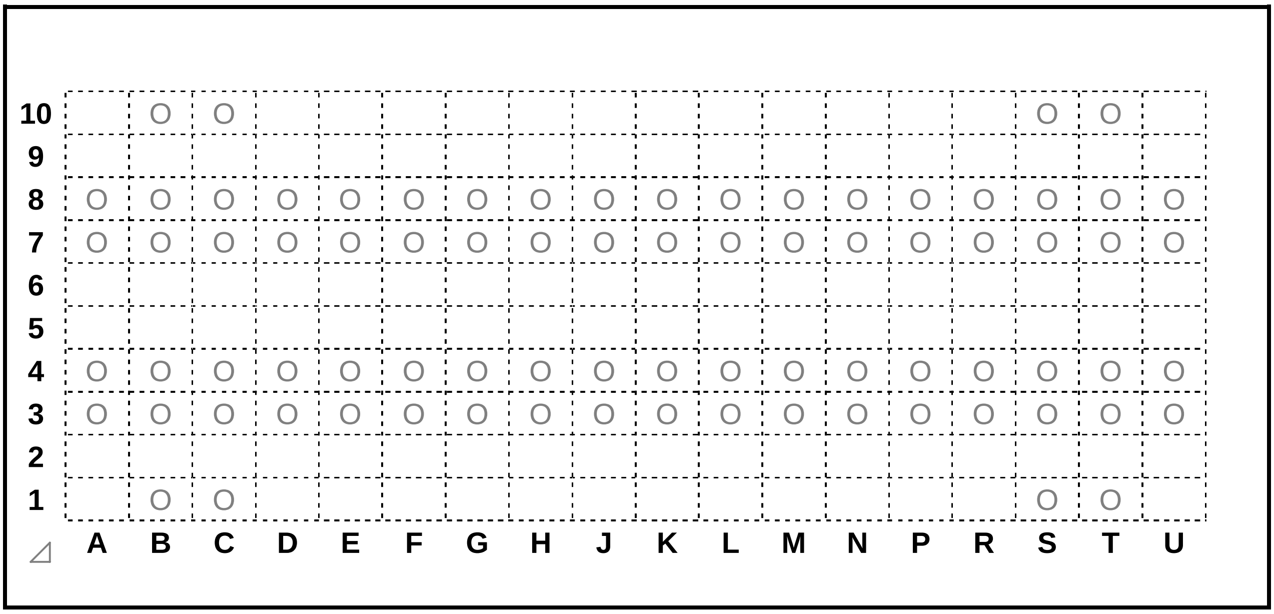
Part number	Organization* words × bits × Internal Banks	Clock frequency MHz (max.)	/RAS access time (ns)	Package
μPD488588FF-C60-53-DH1	512K x 18 x 32s	600	53	80-ball FBGA (μBGA) (17.16 × 10.2)
μPD488588FF-C71-45-DH1		711	45	
μPD488588FF-C80-45-DH1		800	45	

Note: The “32s” designation indicates that this RDRAM core is composed of 32 banks which use a “split” bank architecture

Pin Configuration

80-ball FBGA (μBGA) (17.16 × 10.2)

Top View



10		V_{DD}	GND													GND	V_{DD}	
9																		
8	GND	V_{DD}	CMD	V_{DD}	GND	GNDa	GNDa	V_{DD}	V_{DD}	GND	GND	V_{DD}	V_{DD}	GND	GND	VCMOS	V_{DD}	GND
7	V_{DD}	DQA8	DQA7	DQA5	DQA3	DQA1	CTMN	CTM	ROW2	ROW0	COL3	COL1	DQB1	DQB3	DQB5	DQB7	DQB8	V_{DD}
6																		
5																		
4	GND	GND	DQA6	DQA4	DQA2	DQA0	CFM	CFMN	ROW1	COL4	COL2	COL0	DQB0	DQB2	DQB4	DQB6	GND	GND
3	V_{DD}	GND	SCK	VCMOS	GND	V_{DD}	GND	V_{DD}a	V_{REF}	GND	V_{DD}	GND	GND	V_{DD}	SIO0	SIO1	GND	V_{DD}
2																		
1		V_{DD}	GND													GND	V_{DD}	
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U

Note Some signals can be applied because this pin is not connected to the inside of the chip.

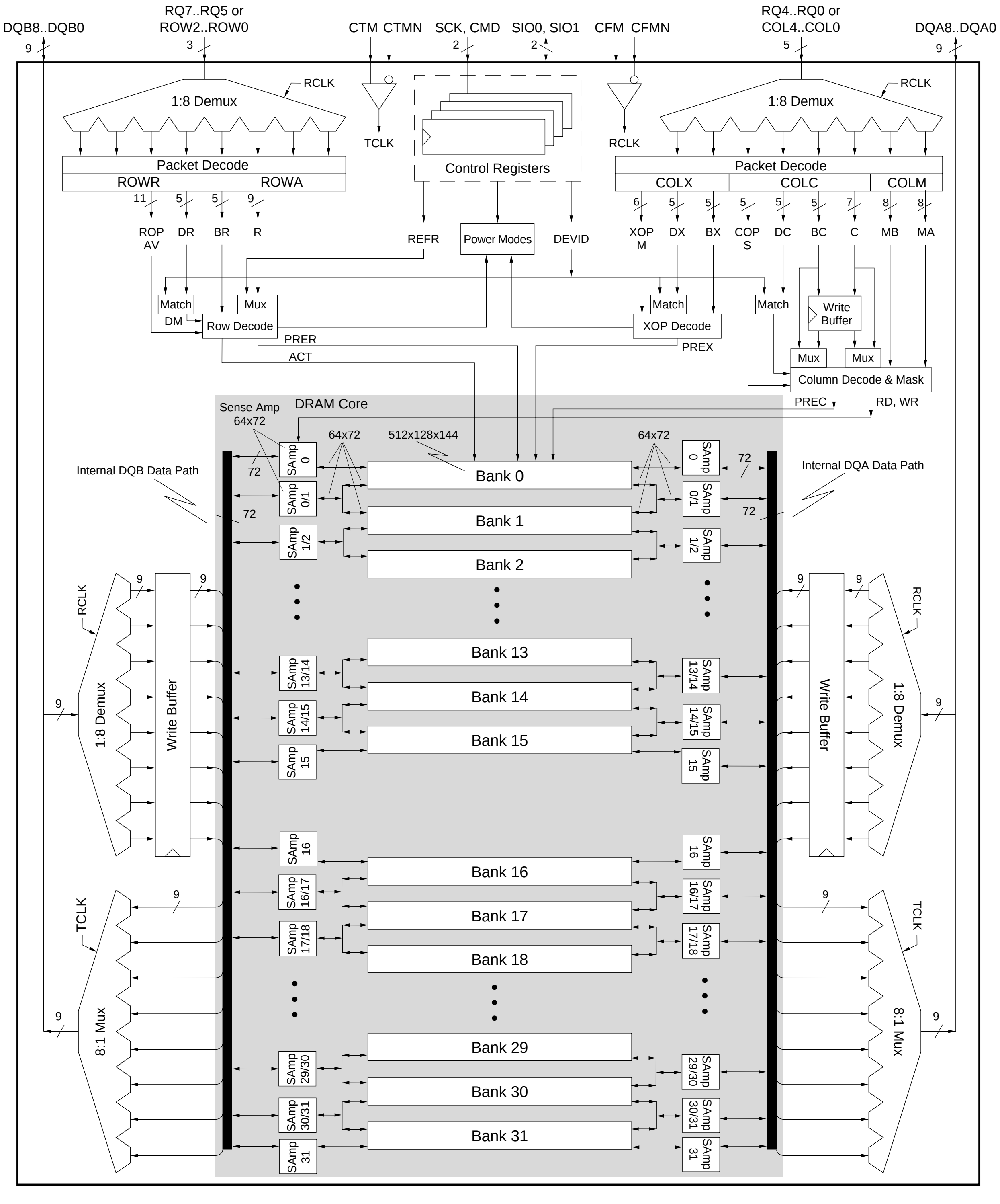
Pin Description

Signal	Input / Output	Type	#pins	Description
SIO0, SIO1	Input / Output	CMOS Note1	2	Serial input/output. Pins for reading from and writing to the control registers using a serial access protocol. Also used for power management.
CMD	Input	CMOS Note1	1	Command input. Pins used in conjunction with SIO0 and SIO1 for reading from and writing to the control registers. Also used for power management.
SCK	Input	CMOS Note1	1	Serial clock input. Clock source used for reading from and writing to the control registers.
V_{DD}			18	Supply voltage for the RDRAM core and interface logic.
V_{DDa}			1	Supply voltage for the RDRAM analog circuitry.
V_{CMOS}			2	Supply voltage for CMOS input/output pins.
GND			22	Ground reference for RDRAM core and interface.
GND_a			2	Ground reference for RDRAM analog circuitry.
DQA8..DQA0	Input / Output	RSL Note2	9	Data byte A. Nine pins which carry a byte of read or write data between the Channel and the RDRAM.
CFM	Input	RSL Note2	1	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
CFMN	Input	RSL Note2	1	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
V_{REF}			1	Logic threshold reference voltage for RSL signals.
CTMN	Input	RSL Note2	1	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
CTM	Input	RSL Note2	1	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
ROW2..ROW0	Input	RSL Note2	3	Row access control. Three pins containing control and address information for row accesses.
COL4..COL0	Input	RSL Note2	5	Column access control. Five pins containing control and address information for column accesses.
DQB8..DQB0	Input / Output	RSL Note2	9	Data byte B. Nine pins which carry a byte of read or write data between the Channel and the RDRAM.
Total pin count per package			80	

Notes 1. All CMOS signals are high-true ; a high voltage is a logic one and a low voltage is logic zero.

2. All RSL signals are low-true ; a low voltage is a logic one and a high voltage is logic zero.

Block Diagram



CONTENTS

1. General Description

The figure on page 5 is a block diagram of the μPD488588. It consists of two major blocks : a “core” block built from banks and sense amps similar to those found in other types of DRAM, and a Direct Rambus interface block which permits an external controller to access this core at up to 1.6 GB/s.

Control Registers: The CMD, SCK, SIO0, and SIO1 pins appear in the upper center of the block diagram. They are used to write and read a block of control registers. These registers supply the RDRAM configuration information to a controller and they select the operating modes of the device. The nine bit REFR value is used for tracking the last refreshed row. Most importantly, the five bits DEVID specifies the device address of the RDRAM on the Channel.

Clocking: The CTM and CTMN pins (Clock-To-Master) generate TCLK (Transmit Clock), the internal clock used to transmit read data. The CFM and CFMN pins (Clock-From-Master) generate RCLK (Receive Clock), the internal clock signal used to receive write data and to receive the ROW and COL pins.

DQA, DQB Pins: These 18 pins carry read (Q) and write (D) data across the Channel. They are multiplexed / de-multiplexed from / to two 72-bit data paths (running at one-eighth the data frequency) inside the RDRAM.

Banks: The 32 Mbyte core of the RDRAM is divided into 32 one-Mbyte banks, each organized as 512 rows, with each row containing 128 dualocts (2K bytes), and each dualoct containing 16 bytes. A dualoct is the smallest unit of data that can be addressed.

Sense Amps: The RDRAM contains 34 sense amps. Each sense amp consists of 1,024 bytes of fast storage (512 for DQA and 512 for DQB) and can hold one-half of one row of one bank of the RDRAM. The sense amp may hold any of the 512 half-rows of an associated bank. However, each sense amp is shared between two adjacent banks of the RDRAM (except for numbers 0, 15, 30, and 31). This introduces the restriction that adjacent banks may not be simultaneously accessed.

RQ Pins: These pins carry control and address information. They are broken into two groups. RQ7..RQ5 are also called ROW2..ROW0, and are used primarily for controlling row accesses. RQ4..RQ0 are also called COL4..COL0, and are used primarily for controlling column accesses.

ROW Pins: The principle use of these three pins is to manage the transfer of data between the banks and the sense amps of the RDRAM. These pins are de-multiplexed into a 24-bit ROWA (row-activate) or ROWR (row-operation) packet.

COL Pins: The principle use of these five pins is to manage the transfer of data between the DQA/DQB pins and the sense amps of the RDRAM. These pins are de-multiplexed into a 23-bit COLC (column-operation) packet and either a 17-bit COLM (mask) packet or a 17-bit COLX (extended-operation) packet.

ACT Command: An ACT (activate) command from an ROWA packet causes one of the 512 rows of the selected bank to be loaded to its associated sense amps (two 512 byte sense amps for DQA and two for DQB).

PRER Command: A PRER (precharge) command from an ROWR packet causes the selected bank to release its two associated sense amps, permitting a different row in that bank to be activated, or permitting adjacent banks to be activated.

RD Command: The RD (read) command causes one of the 128 dualocts of one of the sense amps to be transmitted on the DQA/DQB pins of the Channel.

WR Command: The WR (write) command causes a dualoct received from the DQA/DQB data pins of the Channel to be loaded into the write buffer. There is also space in the write buffer for the BC bank address and C column address information. The data in the write buffer is automatically retired (written with optional bytemask) to one of the 128 dualocts of one of the sense amps during a subsequent COP command. A retire can take place during a RD, WR, or NOCOP to another device, or during a WR or NOCOP to the same device. The write buffer will not retire during a RD to the same device. The write buffer reduces the delay needed for the internal DQA/DQB data path turn-around.

PREC Precharge: The PREC, RDA and WRA commands are similar to NOCOP, RD and WR, except that a precharge operation is performed at the end of the column operation. These commands provide a second mechanism for performing precharge.

PREX Precharge: After a RD command, or after a WR command with no byte masking (M=0), a COLX packet may be used to specify an extended operation (XOP). The most important XOP command is PREX. This command provides a third mechanism for performing precharge.

2. Packet Format

Figure 2-1 shows the formats of the ROWA and ROWR packets on the ROW pins. Table 2-1 describes the fields which comprise these packets. DR4T and DR4F bits are encoded to contain both the DR4 device address bit and a framing bit which allows the ROWA or ROWR packet to be recognized by the RDRAM.

The AV (ROWA/ROWR packet selection) bit distinguishes between the two packet types. Both the ROWA and ROWR packet provide a five bit device address and a four bit bank address. An ROWA packet uses the remaining bits to specify a nine bit row address, and the ROWR packet uses the remaining bits for an eleven bit opcode field. Note the use of the “RsvX” notation to reserve bits for future address field extension.

Figure 2-1 also shows the formats of the COLC, COLM, and COLX packets on the COL pins. Table 2-2 describes the fields which comprise these packets.

The COLC packet uses the S (Start) bit for framing. A COLM or COLX packet is aligned with this COLC packet, and is also framed by the S bit.

The 23 bit COLC packet has a five bit device address, a four bit bank address, a six bit column address, and a four bit opcode. The COLC packet specifies a read or write command, as well as some power management commands.

The remaining 17 bits are interpreted as a COLM (M=1) or COLX (M=0) packet. A COLM packet is used for a COLC write command which needs bytemask control. The COLM packet is associated with the COLC packet from a time t_{RTR} earlier. An COLX packet may be used to specify an independent precharge command. It contains a five bit device address, a four bit bank address, and a five bit opcode. The COLX packet may also be used to specify some housekeeping and power management commands. The COLX packet is framed within a COLC packet but is not otherwise associated with any other packet.

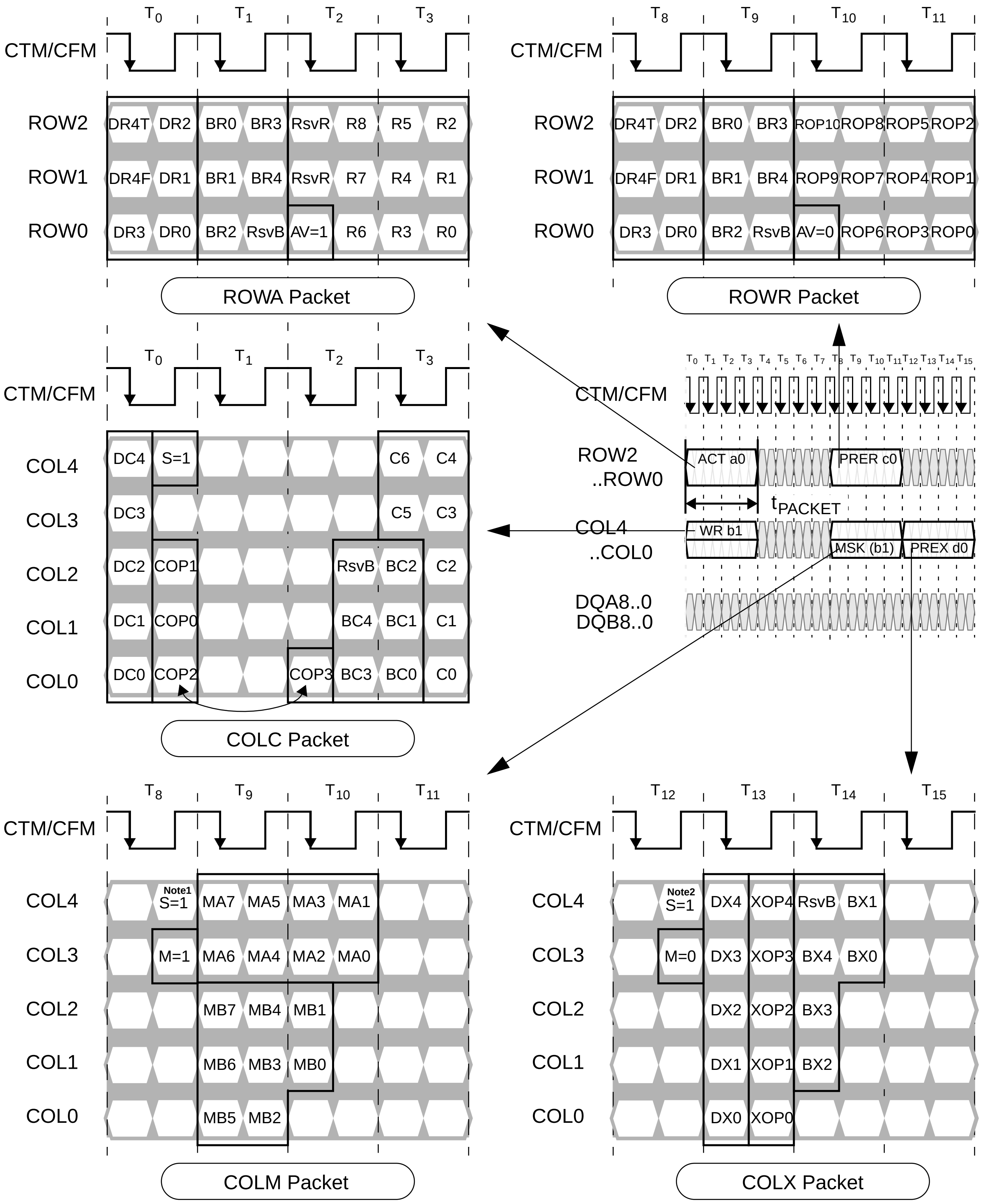
Table 2-1 Field Description for ROWA Packet and ROWR Packet

Field	Description
DR4T, DR4F	Bits for framing (recognizing) a ROWA or ROWR packet. Also encodes highest device address bit.
DR3..DR0	Device address for ROWA or ROWR packet.
BR4..BR0	Bank address for ROWA or ROWR packet. RsvB denotes bits ignored by the RDRAM.
AV	Selects between ROWA packet (AV=1) and ROWR packet (AV=0).
R8..R0	Row address for ROWA packet. RsvR denotes bits reserved for future row address extension.
ROP10..ROP0	Opcode field for ROWR packet. Specifies precharge, refresh, and power management functions.

Table 2-2 Field Description for COLC Packet, COLM Packet, and COLX Packet

Field	Description
S	Bit for framing (recognizing) a COLC packet, and indirectly for framing COLM and COLX packets.
DC4..DC0	Device address for COLC packet.
BC4..BC0	Bank address for COLC packet. RsvB denotes bits reserved for future extension (controller drivers 0's).
C6..C0	Column address for COLC packet.
COP3..COP0	Opcode field for COLC packet. Specifies read, write, precharge, and power management functions.
M	Selects between COLM packet (M=1) and COLX packet (M=0).
MA7..MA0	Bytemask write control bits. 1=write, 0=no-write. MA0 controls the earliest byte on DQA8..0.
MB7..MB0	Bytemask write control bits. 1=write, 0=no-write. MB0 controls the earliest byte on DQB8..0.
DX4..DX0	Device address for COLX packet.
BX4..BX0	Bank address for COLX packet. RsvB denotes bits reserved for future extension (controller drivers 0's).
XOP4..XOP0	Opcode field for COLX packet. Specifies precharge, I_{OL} control, and power management functions.

Figure 2-1 Packet Formats



Notes 1. The COLM is associated with a previous COLC, and is aligned with the present COLC, indicated by the Start bit (S=1) position.

2. The COLX is aligned with the present COLC, indicates by the Start bit (S=1) position.

3. Field Encoding Summary

Table 3-1 shows how the six device address bits are decoded for the ROWA and ROWR packets. The DR4T and DR4F encoding merges a fifth device bit with a framing bit. When neither bit is asserted, the device is not selected. Note that a broadcast operation is indicated when both bits are set. Broadcast operation would typically be used for refresh and power management commands. If the device is selected, the DM (DeviceMatch) signal is asserted and an ACT or ROP command is performed.

Table 3-1 Device Field Encodings for ROWA Packet and ROWR Packet

DR4T	DR4F	Device Selection	Device Match signal (DM)
1	1	All devices (broadcast)	DM is set to 1
0	1	One device selected	DM is set to 1 if {DEVID4..DEVID0} == {0, DR3..DR0} else DM is set to 0
1	0	One device selected	DM is set to 1 if {DEVID4..DEVID0} == {1, DR3..DR0} else DM is set to 0
0	0	No packet present	DM is set to 0

Table 3-2 shows the encodings of the remaining fields of the ROWA and ROWR packets. An ROWA packet is specified by asserting the AV bit. This causes the specified row of the specified bank of this device to be loaded into the associated sense amps.

An ROWR packet is specified when AV is not asserted. An 11 bit opcode field encodes a command for one of the banks of this device. The PRER command causes a bank and its two associated sense amps to precharge, so another row or an adjacent bank may be activated.

The REFA (refresh-activate) command is similar to the ACT command, except the row address comes from an internal register REFR, and REFR is incremented at the largest bank address. The REFP (refresh-precharge) command is identical to a PRER command.

The NAPR, NAPRC, PDNR, ATTN, and RLXR commands are used for managing the power dissipation of the RDRAM and are described in more detail in “**23. Power State Management**”. The TCEN and TCAL commands are used to adjust the output driver slew rate and they are described in more detail in “**25. Current and Temperature Control**”.

Table 3-2 ROWA Packet and ROWR Packet Field Encodings

DM [Note1]	AV	ROP10..ROP0 Field									Name	Command Description
		10	9	8	7	6	5	4	3	2 : 0		
0	—	—	—	—	—	—	—	—	—	---	—	No operation.
1	1	Row address									ACT	Activate row R8..R0 of bank BR4..BR0 of device and move device to ATTN[Note2].
1	0	1	1	0	0	0	x[Note3]	x	x	000	PRER	Precharge bank BR4..BR0 of this device.
1	0	0	0	0	1	1	0	0	x	000	REFA	Refresh (activate) row REFR8..REFR0 of bank BR3..BR0 of device. Increment REFR if BR4..BR0=11111 (see Figure 24-1).
1	0	1	0	1	0	1	0	0	x	000	REFP	Precharge bank BR4..BR0 of this device after REFA (see Figure 24-1).
1	0	x	x	0	0	0	0	1	x	000	PDNR	Move this device into the powerdown (PDN) power state (see figure 23-3).
1	0	x	x	0	0	0	1	0	x	000	NAPR	Move this device into the nap (NAP) power state (see Figure 23-3).
1	0	x	x	0	0	0	1	1	x	000	NAPRC	Move this device into the nap (NAP) power state conditionally.
1	0	x	x	x	x	x	x	x	0	000	ATTN[Note2]	Move this device into the attention (ATTN) power state (see Figure 23-1).
1	0	x	x	x	x	x	x	x	1	000	RLXR	Move this device into the standby (STBY) power state (see Figure 23-2).
1	0	0	0	0	0	0	0	0	x	001	TCAL	Temperature calibrate this device (see figure 25-2).
1	0	0	0	0	0	0	0	0	x	010	TCEN	Temperature calibrate/enable this device (see Figure 25-2).
1	0	0	0	0	0	0	0	0	0	000	NOROP	No operation.

Notes 1. The DM (Device Match signal) value is determined by the DR4T, DR4F, DR3..DR0 field of the ROWA and ROWR packets. See Table 3-1.

2. The ATTN command does not cause a RLX-to-ATTN transition for a broadcast operation (DR4T/DR4F=1/1).

3. An “x” entry indicates which commands may be combined. For instance, the three commands PRER/NAPRC/RLXR may be specified in one ROP value (011000111000).

Table 3-3 shows the COP field encoding. The device must be in the ATTN power state in order to receive COLC packets. The COLC packet is used primarily to specify RD (read) and WR (write) commands. Retire operations (moving data from the write buffer to a sense amp) happen automatically. See Figure 15-1 for a more detailed description.

The COLC packet can also specify a PREC command, which precharges a bank and its associated sense amps. The RDA/WRA commands are equivalent to a combining RD/WR with a PREC. RLXC (relax) performs a power mode transition. See **23. Power State Management**.

Table 3-3 COLC Packet Field Encodings

S	DC4..DC0 (select device)[Note1]	COP3..0	Name	Command Description
0	- - - -	- - - - -	—	No operation.
1	/= (DEVID4..0)	- - - - -	—	Retire write buffer of this device.
1	== (DEVID4..0)	x000[Note2]	NOCOP	Retire write buffer of this device.
1	== (DEVID4..0)	x001	WR	Retire write buffer of this device, then write column C6..C0 of bank BC4..BC0 to write buffer.
1	== (DEVID4..0)	x010	RSRV	Reserved, no operation.
1	== (DEVID4..0)	x011	RD	Read column C6..C0 of bank BC4..BC0 of this device.
1	== (DEVID4..0)	x100	PREC	Retire write buffer of this device, then precharge bank BC4..BC0 (see Figure 12-2).
1	== (DEVID4..0)	x101	WRA	Same as WR, but precharge bank BC4..BC0 after write buffer (with new data) is retired.
1	== (DEVID4..0)	x110	RSRV	Reserved, no operation.
1	== (DEVID4..0)	x111	RDA	Same as RD, but precharge bank BC4..BC0 afterward.
1	== (DEVID4..0)	1xxx	RLXC	Move this device into the standby (STBY) power state (see Figure 23-2).

Notes 1. "/=" means not equal, "==" means equal.

2. An "x" entry indicates which commands may be combined. For instance, the two commands WR/RLXC may be specified in one COP value(1001).

Table 3-4 shows the COLM and COLX field encodings. The M bit is asserted to specify a COLM packet with two 8 bit bytemask fields MA and MB. If the M bit is not asserted, an COLX is specified. It has device and bank address fields, and an opcode field. The primary use of the COLX packet is to permit an independent PREX (precharge) command to be specified without consuming control bandwidth on the ROW pins. It is also used for the CAL (calibrate) and SAM (sample) current control commands (see **25. Current and Temperature Control**), and for the RLXX power mode command (see **23. Power State Management**).

Table 3-4 COLM Packet and COLX Packet Field Encodings

M	DX4..DX0 (select device)	XOP4..0	Name	Command Description
1	- - - -	-	MSK	MB/MA bytemasks used by WR/WRA.
0	/= (DEVID4..0)	-	—	No operation.
0	== (DEVID4..0)	00000	NOXOP	No operation.
0	== (DEVID4..0)	1xxx0[Note]	PREX	Precharge bank BX4..BX0 of this device (see Figure 12-2).
0	== (DEVID4..0)	x10x0	CAL	Calibrate (drive) I_{OL} current for this device (see Figure 25-1).
0	== (DEVID4..0)	x11x0	CAL / SAM	Calibrate (drive) and Sample (update) I_{OL} current for this device (see Figure 25-1).
0	== (DEVID4..0)	xxx10	RLXX	Move this device into the standby (STBY) power state (see Figure 23-2).
0	== (DEVID4..0)	xxxx1	RSRV	Reserved, no operation.

Note An "x" entry indicates which commands may be combined. For instance, the two commands PREX/RLXX may be specified in one XOP value (10010).

4. DQ Packet Timing

Figure 4-1 shows the timing relationship of COLC packets with D and Q data packets. This document uses a specific convention for measuring time intervals between packets: all packets on the ROW and COL pins (ROWA, ROWR, COLC, COLM, COLX) use the trailing edge of the packet as a reference point, and all packets on the DQA/DQB pins (D and Q) use the leading edge of the packet as a reference point.

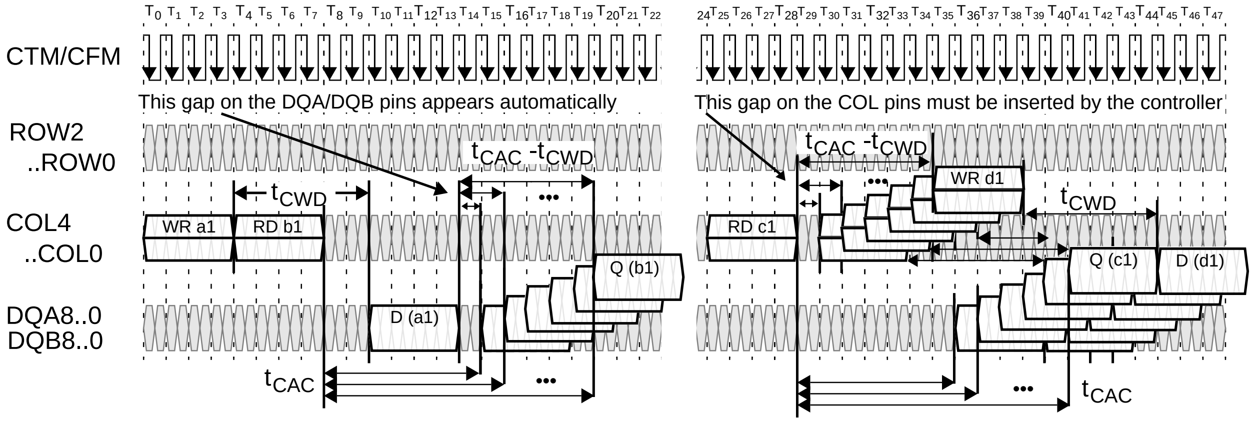
An RD or RDA command will transmit a dualoct of read data Q a time t_{CAC} later. This time includes one to five cycles of round-trip propagation delay on the Channel. The t_{CAC} parameter may be programmed to a one of a range of values (7, 8, 9, 10, 11, or 12 t_{CYCLE}). The value chosen depends upon the number of RDRAM devices on the Channel and the RDRAM timing bin. See Figure 22-1(5/7) “**TPARM Register**” for more information.

A WR or WRA command will receive a dualoct of write data D a time t_{CWD} later. This time does not need to include the round-trip propagation time of the Channel since the COLC and D packets are traveling in the same direction.

When a Q packet follows a D packet (shown in the left half of the figure), a gap (t_{CAC}-t_{CWD}) will automatically appear between them because the t_{CWD} value is always less than the t_{CAC} value. There will be no gap between the two COLC packets with the WR and RD commands which schedule the D and Q packets.

When a D packet follows a Q packet (shown in the right half of the figure), no gap is needed between them because the t_{CWD} value is less than the t_{CAC} value. However, a gap of t_{CAC} - t_{CWD} or greater must be inserted between the COLC packets with the RD WR commands by the controller so the Q and D packets do not overlap.

Figure 4-1 Read (Q) and Write (D) Data Packet - Timing for t_{CAC} = 7,8,9,10,11 or 12 t_{CYCLE}



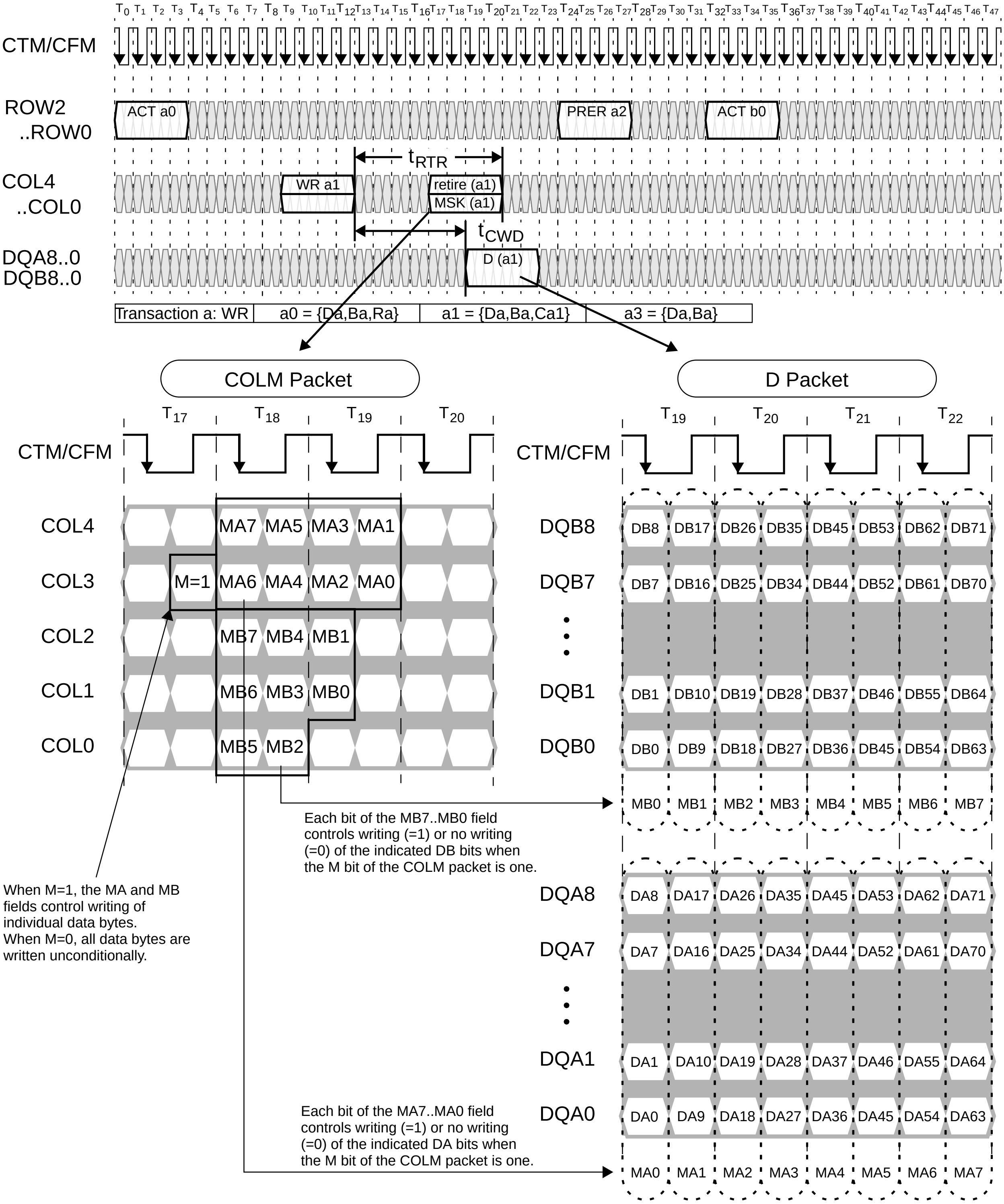
5. COLM Packet to D Packet Mapping

Figure 5-1 shows a write operation initiated by a WR command in a COLC packet. If a subset of the 16 bytes of write data are to be written, then a COLM packet is transmitted on the COL pins a time t_{RTR} after the COLC packet containing the WR command. The M bit of the COLM packet is set to indicate that it contains the MA and MB mask fields. Note that this COLM packet is aligned with the COLC packet which causes the write buffer to be retired. See Figure 15-1 for more details.

If all 16 bytes of the D data packet are to be written, then no further control information is required. The packet slot that would have been used by the COLM packet (t_{RTR} after the COLC packet) is available to be used as an COLX packet. This could be used for a PREX precharge command or for a housekeeping command (this case is not shown). The M bit is not asserted in an COLX packet and causes all 16 bytes of the previous WR to be written unconditionally. Note that a RD command will never need a COLM packet, and will always be able to use the COLX packet option (a read operation has no need for the byte-write-enable control bits).

The figure 5-1 also shows the mapping between the MA and MB fields of the COLM packet and bytes of the D packet on the DQA and DQB pins. Each mask bit controls whether a byte of data is written (=1) or not written (=0).

Figure 5-1 Mapping between COLM Packet and D Packet for WR Command



	T17		T18		T19		T20	
COL4			MA7	MA5	MA3	MA1		
COL3		M=1	MA6	MA4	MA2	MA0		
COL2			MB7	MB4	MB1			
COL1			MB6	MB3	MB0			
COL0			MB5	MB2				

	T19		T20		T21		T22	
DQB8	DB8	DB17	DB26	DB35	DB45	DB53	DB62	DB71
DQB7	DB7	DB16	DB25	DB34	DB44	DB52	DB61	DB70
• • •								
DQB1	DB1	DB10	DB19	DB28	DB37	DB46	DB55	DB64
DQB0	DB0	DB9	DB18	DB27	DB36	DB45	DB54	DB63
	MB0	MB1	MB2	MB3	MB4	MB5	MB6	MB7
DQA8	DA8	DA17	DA26	DA35	DA45	DA53	DA62	DA71
DQA7	DA7	DA16	DA25	DA34	DA44	DA52	DA61	DA70
• • •								
DQA1	DA1	DA10	DA19	DA28	DA37	DA46	DA55	DA64
DQA0	DA0	DA9	DA18	DA27	DA36	DA45	DA54	DA63
	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7

Each bit of the MB7..MB0 field controls writing (=1) or no writing (=0) of the indicated DB bits when the M bit of the COLM packet is one.

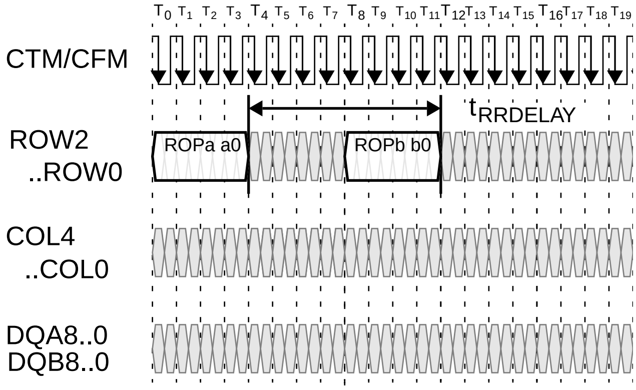
When M=1, the MA and MB fields control writing of individual data bytes.
When M=0, all data bytes are written unconditionally.

Each bit of the MA7..MA0 field controls writing (=1) or no writing (=0) of the indicated DA bits when the M bit of the COLM packet is one.

6. ROW-to-ROW Packet Interaction

Figure 6-1 shows two packets on the ROW pins separated by an interval $t_{RRDELAY}$ which depends upon the packet contents. No other ROW packets are sent to banks {Ba, Ba+1, Ba-1} between packet “a” and packet “b” unless noted otherwise.

Figure 6-1 ROW-to-ROW Packet Interaction - Timing



Transaction a: ROPa	a0 = {Da,Ba,Ra}
Transaction b: ROPb	b0= {Db,Bb,Rb}

Table 6-1 summarizes the $t_{RRDELAY}$ values for all possible cases.

Cases RR1 through RR4 show two successive ACT commands. In case RR1, there is no restriction since the ACT commands are to different devices. In case RR2, the t_{RR} restriction applies to the same device with non-adjacent banks. Cases RR3 and RR4 are illegal (as shown) since bank Ba needs to be precharged. If a PRER to Ba, Ba+1, or Ba-1 is inserted, $t_{RRDELAY}$ is t_{RC} (t_{RAS} to the PRER command, and t_{RP} to the next ACT).

Cases RR5 through RR8 show an ACT command followed by a PRER command. In cases RR5 and RR6, there are no restrictions since the commands are to different devices or to non-adjacent banks of the same device. In cases RR7 and RR8, the t_{RAS} restriction means the activated bank must wait before it can be precharged.

Cases RR9 through RR12 show a PRER command followed by an ACT command. In cases RR9 and RR10, there are essentially no restrictions since the commands are to different devices or to non-adjacent banks of the same device. RR10a and RR10b depend upon whether a bracketed bank (Ba+-1) is precharged or activated. In cases RR11 and RR12, the same and adjacent banks must all wait t_{RP} for the sense amp and bank to precharge before being activated.

Cases RR13 through RR16 summarize the combinations of two successive PRER commands. In case RR13 there is no restriction since two devices are addressed. In RR14, t_{PP} applies, since the same device is addressed. In RR15 and RR16, the same bank or an adjacent bank may be given repeated PRER commands with only the t_{PP} restriction.

Two adjacent banks can’t be activate simultaneously. A precharge command to one bank will thus affect the state of the adjacent banks (and sense amps). If bank Ba is activate and a PRER is directed to Ba, then bank Ba will be precharged along with sense amps Ba-1/Ba and Ba/Ba+1. If bank Ba+1 is activate and a PRER is directed to Ba, then bank Ba+1 will be precharged along with sense amps Ba/Ba+1 and Ba+1/Ba+2. If bank Ba-1 is activate and a PRER is directed to Ba, then bank Ba-1 will be precharged along with sense amps Ba/Ba-1 and Ba-1/Ba-2.

A ROW packet may contain commands other than ACT or PRER. The REFA and REFP commands are equivalent to ACT and PRER for interaction analysis purposes. The interaction rules of the NAPR, NAPRC, PDNR, RLXR, ATTN, TCAL, and TCEN commands are discussed in later section (see Table 3-2 for cross-ref).

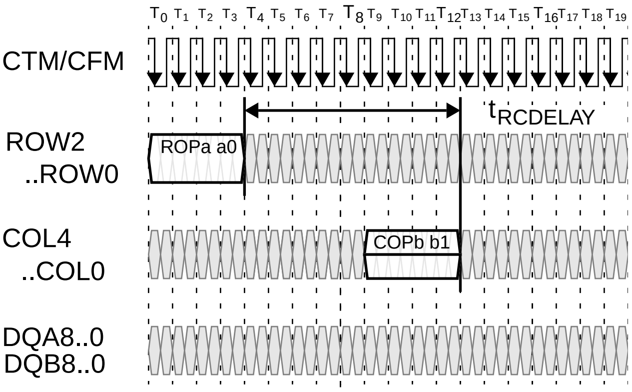
Table 6-1 ROW-to-ROW Packet Interaction - Rules

Case #	ROPa	Da	Ba	Ra	ROPb	Db	Bb	Rb	$t_{RRDELAY}$	Example
RR1	ACT	Da	Ba	Ra	ACT	/= Da	xxxx	x..x	t_{PACKET}	Figure 10-2
RR2	ACT	Da	Ba	Ra	ACT	== Da	/= {Ba, Ba+1, Ba-1}	x..x	t_{RR}	Figure 10-2
RR3	ACT	Da	Ba	Ra	ACT	== Da	== {Ba+1, Ba-1}	x..x	t_{RC} - illegal unless PRER to Ba / Ba+1 / Ba-1	Figure 10-1
RR4	ACT	Da	Ba	Ra	ACT	== Da	== {Ba}	x..x	t_{RC} - illegal unless PRER to Ba / Ba+1 / Ba-1	Figure 10-1
RR5	ACT	Da	Ba	Ra	PRER	/= Da	xxxx	x..x	t_{PACKET}	Figure 10-2
RR6	ACT	Da	Ba	Ra	PRER	== Da	/= {Ba, Ba+1, Ba-1}	x..x	t_{PACKET}	Figure 10-2
RR7	ACT	Da	Ba	Ra	PRER	== Da	== {Ba+1, Ba-1}	x..x	t_{RAS}	Figure 10-1
RR8	ACT	Da	Ba	Ra	PRER	== Da	== {Ba}	x..x	t_{RAS}	Figure 13-1
RR9	PRER	Da	Ba	Ra	ACT	/= Da	xxxx	x..x	t_{PACKET}	Figure 10-3
RR10	PRER	Da	Ba	Ra	ACT	== Da	/= {Ba, Ba+-1, Ba+-2}	x..x	t_{PACKET}	Figure 10-3
RR10a	PRER	Da	Ba	Ra	ACT	== Da	== {Ba+2}	x..x	t_{PACKET}/t_{RP} if Ba+1 is precharged/activated.	
RR10b	PRER	Da	Ba	Ra	ACT	== Da	== {Ba-2}	x..x	t_{PACKET}/t_{RP} if Ba-1 is precharged/activated.	
RR11	PRER	Da	Ba	Ra	ACT	== Da	== {Ba+1, Ba-1}	x..x	t_{RP}	Figure 10-1
RR12	PRER	Da	Ba	Ra	ACT	== Da	== {Ba}	x..x	t_{RP}	Figure 10-1
RR13	PRER	Da	Ba	Ra	PRER	/= Da	xxxx	x..x	t_{PACKET}	Figure 10-3
RR14	PRER	Da	Ba	Ra	PRER	== Da	/= {Ba, Ba+1, Ba-1}	x..x	t_{PP}	Figure 10-3
RR15	PRER	Da	Ba	Ra	PRER	== Da	== {Ba+1, Ba-1}	x..x	t_{PP}	Figure 10-3
RR16	PRER	Da	Ba	Ra	PRER	== Da	== {Ba}	x..x	t_{PP}	Figure 10-3

7. ROW-to-COL Packet Interaction

Figure 7-1 shows two packets on the ROW and COL pins. They must be separated by an interval $t_{RCDELAY}$ which depends upon the packet contents.

Figure 7-1 ROW-to-COL Packet Interaction- Timing



Transaction a: ROPa	a0 = {Da,Ba,Ra}
Transaction b: COPb	b1= {Db,Bb,Cb1}

Table 7-1 summarizes the $t_{RCDELAY}$ values for all possible cases. Note that if the COL packet is earlier than the ROW packet, it is considered a COL-to-ROW packet interaction.

Cases RC1 through RC5 summarize the rules when the ROW packet has an ACT command. Figure 13-1 and Figure 14-1 show examples of RC5 - an activation followed by a read or write. RC4 is an illegal situation, since a read or write of a precharged banks is being attempted (remember that for a bank to be activated, adjacent banks must be precharged). In cases RC1, RC2, and RC3, there is no interaction of the ROW and COL packets.

Cases RC6 through RC8 summarize the rules when the ROW packet has a PRER command. There is either no interaction (RC6 through RC9) or an illegal situation with a read or write of a precharged bank (RC9).

The COL pins can also schedule a precharge operation with a RDA, WRA, or PREC command in a COLC packet or a PREX command in a COLX packet. The constraints of these precharge operations may be converted to equivalent PRER command constraints using the rules summarized in Figure 12-2.

Table 7-1 ROW-to-COL Packet Interaction - Rules

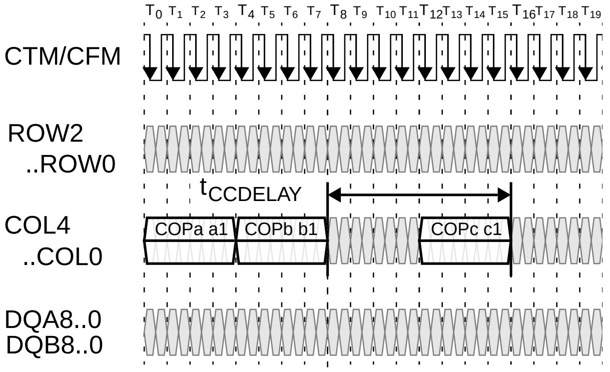
Case #	ROPa	Da	Ba	Ra	COPb	Db	Bb	Cb1	$t_{RCDELAY}$	Example
RC1	ACT	Da	Ba	Ra	NOCOP, RD, retire	/= Da	xxxx	x..x	0	
RC2	ACT	Da	Ba	Ra	NOCOP	== Da	xxxx	x..x	0	
RC3	ACT	Da	Ba	Ra	RD, retire	== Da	/= {Ba, Ba+1, Ba-1}	x..x	0	
RC4	ACT	Da	Ba	Ra	RD, retire	== Da	== {Ba+1, Ba-1}	x..x	Illegal	
RC5	ACT	Da	Ba	Ra	RD, retire	== Da	== {Ba}	x..x	t_{RCD}	Figure 13-1
RC6	PRER	Da	Ba	Ra	NOCOP, RD, retire	/= Da	xxxx	x..x	0	
RC7	PRER	Da	Ba	Ra	NOCOP	== Da	xxxx	x..x	0	
RC8	PRER	Da	Ba	Ra	RD, retire	== Da	/= {Ba, Ba+1, Ba-1}	x..x	0	
RC9	PRER	Da	Ba	Ra	RD, retire	== Da	== {Ba+1, Ba-1}	x..x	Illegal	

8. COL-to-COL Packet Interaction

Figure 8-1 shows three arbitrary packets on the COL pins. Packets “b” and “c” must be separated by an interval $t_{CCDELAY}$ which depends upon the command and address values in all three packets. Table 8-1 summarizes the $t_{CCDELAY}$ values for all possible cases.

Cases CC1 through CC5 summarize the rules for every situation other than the case when COPb is a WR command and COPc is a RD command. In CC3, when a RD command is followed by a WR command, a gap of t_{CAC} - t_{CWD} must be inserted between the two COL packets. See Figure 4-1 for more explanation of why this gap is needed. For cases CC1, CC2, CC4, and CC5, there is no restriction ($t_{CCDELAY}$ is t_{CC}).

Figure 8-1 COL-to-COL Packet Interaction- Timing



Transaction a: COPa	a1 = {Da,Ba,Ca1}
Transaction b: COPb	b1 = {Db,Bb,Cb1}
Transaction c: COPc	c1 = {Dc,Bc,Cc1}

In cases CC6 through CC10, COPb is a WR command and COPc is a RD command. The $t_{CCDELAY}$ value needed between these two packets depends upon the command and address in the packet with COPa. In particular, in case CC6 when there is WR-WR-RD command sequence directed to the same device, a gap will be needed between the packets with COPb and COPc. The gap will need a COLC packet with a NOCOP command directed to any device in order to force an automatic retire to take place. Figure 15-2 (right) provides a more detailed explanation of this case.

In case CC10, there is a RD-WR-RD sequence directed to the same device. If a prior write to the same device is unretired when COPa is issued, then a gap will be needed between the packets with COPb and COPc as in case CC6. The gap will need a COLC packet with a NOCOP command directed to any device in order to force an automatic retire to take place.

Cases CC7, CC8, and CC9 have no restriction ($t_{CCDELAY}$ is t_{CC}).

For the purposes of analyzing COL-to-ROW interactions, the PREC, WRA, and RDA commands of the COLC packet are equivalent to the NOCOP, WR, and RD commands. These commands also cause a precharge operation PREC to take place. This precharge may be converted to an equivalent PRER command on the ROW pins using the rules summarized in Figure 12-2.

Table 8-1 COL-to-COL Packet Interaction - Rules

Case #	COPa	Da	Ba	Ca1	COPb	Db	Bb	Cb1	COPc	Dc	Bc	Cc1	$t_{CCDELAY}$	Example
CC1	xxxx	xxxxx	x..x	x..x	NOCOP	Db	Bb	Cb1	xxxx	xxxxx	x..x	x..x	t_{CC}	
CC2	xxxx	xxxxx	x..x	x..x	RD, WR	Db	Bb	Cb1	NOCOP	xxxxx	x..x	x..x	t_{CC}	
CC3	xxxx	xxxxx	x..x	x..x	RD	Db	Bb	Cb1	WR	xxxxx	x..x	x..x	$t_{CC}+t_{CAC}-t_{CWD}$	Figure 4-1
CC4	xxxx	xxxxx	x..x	x..x	RD	Db	Bb	Cb1	RD	xxxxx	x..x	x..x	t_{CC}	Figure 13-1
CC5	xxxx	xxxxx	x..x	x..x	WR	Db	Bb	Cb1	WR	xxxxx	x..x	x..x	t_{CC}	Figure 14-1
CC6	WR	== Db	x	x..x	WR	Db	Bb	Cb1	RD	== Db	x..x	x..x	t_{RTR}	Figure 15-1
CC7	WR	== Db	x	x..x	WR	Db	Bb	Cb1	RD	/= Db	x..x	x..x	t_{CC}	
CC8	WR	/= Db	x	x..x	WR	Db	Bb	Cb1	RD	== Db	x..x	x..x	t_{CC}	
CC9	NOCOP	== Db	x	x..x	WR	Db	Bb	Cb1	RD	== Db	x..x	x..x	t_{CC}	
CC10	RD	== Db	x	x..x	WR	Db	Bb	Cb1	RD	== Db	x..x	x..x	t_{CC}	

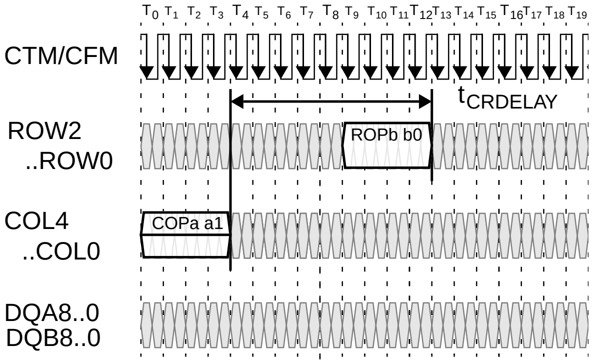
9. COL-to-ROW Packet Interaction

Figure 9-1 shows arbitrary packets on the COL and ROW pins. They must be separated by an interval $t_{CRDELAY}$ which depends upon the command and address values in the packets. Table 9-1 summarizes the $t_{CRDELAY}$ value for all possible cases.

Cases CR1, CR2, CR3, and CR9 show no interaction between the COL and ROW packets, either because one of the commands is a NOP or because the packets are directed to different devices or to non-adjacent banks.

Case CR4 is illegal because an already-activated bank is to be re-activated without being precharged. Case CR5 is illegal because an adjacent bank can't be activated or precharged until bank Ba is precharged first.

Figure 9-1 COL-to-ROW Packet Interaction- Timing



Transaction a: COPa	a1= {Da,Ba,Ca1}
Transaction b: ROPb	b0= {Db,Bb,Rb}

In case CR6, the COLC packet contains a RD command, and the ROW packet contains a PRER command for the same bank. The t_{RDP} parameter specifies the required spacing.

Likewise, in case CR7, the COLC packet causes an automatic retire to take place, and the ROW packet contains a PRER command for the same bank. The t_{RTP} parameter specifies the required spacing.

Case CR8 is labeled “Hazardous” because a WR command should always be followed by an automatic retire before a precharge is scheduled. Figure 15-3 shows an example of what can happen when the retire is not able to happen before the precharge.

For the purposes of analyzing COL-to-ROW interactions, the PREC, WRA, and RDA commands of the COLC packet are equivalent to the NOCOP, WR, and RD commands. These commands also cause a precharge operation to take place. This precharge may converted to an equivalent PRER command on the ROW pins using the rules summarized in Figure 12-2.

A ROW packet may contain commands other than ACT or PRER. The REFA and REFP commands are equivalent to ACT and PRER for interaction analysis purposes. The interaction rules of the NAPR, PDNR, and RLXR commands are discussed in a later section.

Table 9-1 COL-to-ROW Packet Interaction - Rules

Case #	COPa	Da	Ba	Ca1	ROPb	Db	Bb	Rb	$t_{CRDELAY}$	Example
CR1	NOCOP	Da	Ba	Ca1	x..x	xxxxx	xxxxx	x..x	0	
CR2	RD/WR	Da	Ba	Ca1	x..x	/= Da	xxxxx	x..x	0	
CR3	RD/WR	Da	Ba	Ca1	x..x	== Da	/= {Ba, Ba+1, Ba-1}	x..x	0	
CR4	RD/WR	Da	Ba	Ca1	ACT	== Da	== {Ba}	x..x	Illegal	
CR5	RD/WR	Da	Ba	Ca1	ACT	== Da	== {Ba+1, Ba-1}	x..x	Illegal	
CR6	RD	Da	Ba	Ca1	PRER	== Da	== {Ba, Ba+1, Ba-1}	x..x	t_{RDP}	Figure 13-1
CR7	retire [Note 1]	Da	Ba	Ca1	PRER	== Da	== {Ba, Ba+1, Ba-1}	x..x	t_{RTP}	Figure 14-1
CR8	WR [Note 2]	Da	Ba	Ca1	PRER	== Da	== {Ba, Ba+1, Ba-1}	x..x	0	Figure 15-3
CR9	xxxx	Da	Ba	Ca1	NOROP	xxxxx	xxxxx	x..x	0	

Notes 1. This is any command which permits the write buffer of device Da to retire (see Table 3-3). “Ba” is the bank address in the write buffer.

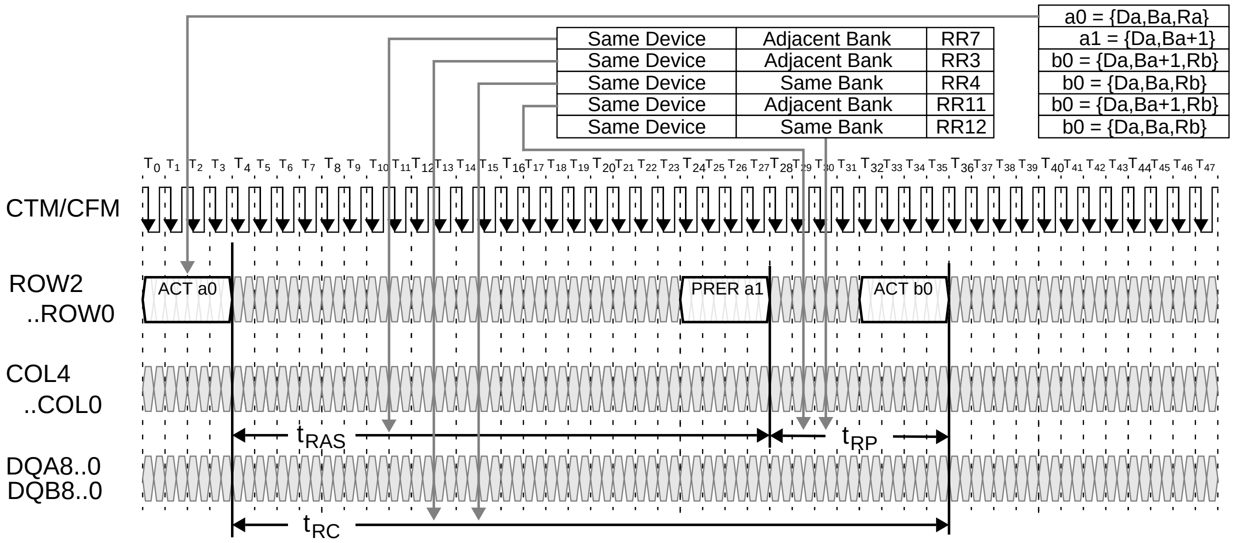
2. This situation is hazardous because the write buffer will be left unretired while the targeted bank is precharged. See Figure 15-3.

10. ROW-to-ROW Examples

Figure 10-1 shows examples of some of the ROW-to-ROW packet spacings from Table 6-1. A complete sequence of activate and precharge commands is directed to a bank. The RR8 and RR12 rules apply to this sequence. In addition to satisfying the t_{RAS} and t_{RP} timing parameters, the separation between ACT commands to the same bank must also satisfy the t_{RC} timing parameter (RR4).

When a bank is activated, it is necessary for adjacent banks to remain precharged. As a result, the adjacent banks will also satisfy parallel timing constraints; in the example, the RR11 and RR3 rules are analogous to the RR12 and RR4 rules.

Figure 10-1 Row Packet Example

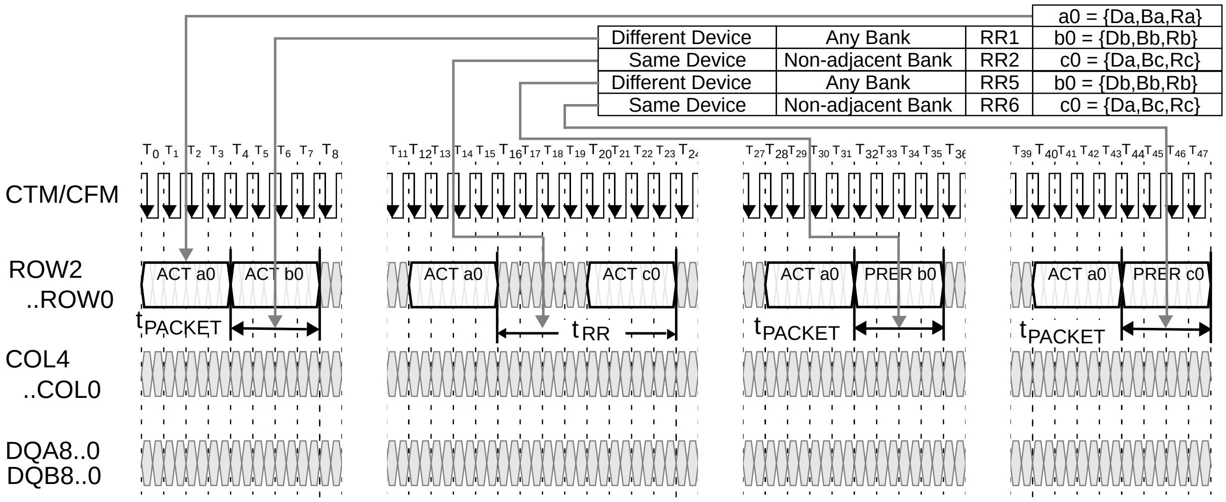


Same Device	Adjacent Bank	RR7
Same Device	Adjacent Bank	RR3
Same Device	Same Bank	RR4
Same Device	Adjacent Bank	RR11
Same Device	Same Bank	RR12

a0 = {Da,Ba,Ra}
a1 = {Da,Ba+1}
b0 = {Da,Ba+1,Rb}
b0 = {Da,Ba,Rb}
b0 = {Da,Ba+1,Rb}
b0 = {Da,Ba,Rb}

Figure 10-2 shows examples of the ACT-to-ACT (RR1, RR2) and ACT-to-PRER (RR5, RR6) command spacings from Table 6-1. In general, the commands in ROW packets may be spaced an interval t_{PACKET} apart unless they are directed to the same or adjacent banks or unless they are a similar command type (both PRER or both ACT) directed to the same device.

Figure 10-2 Row Packet Example

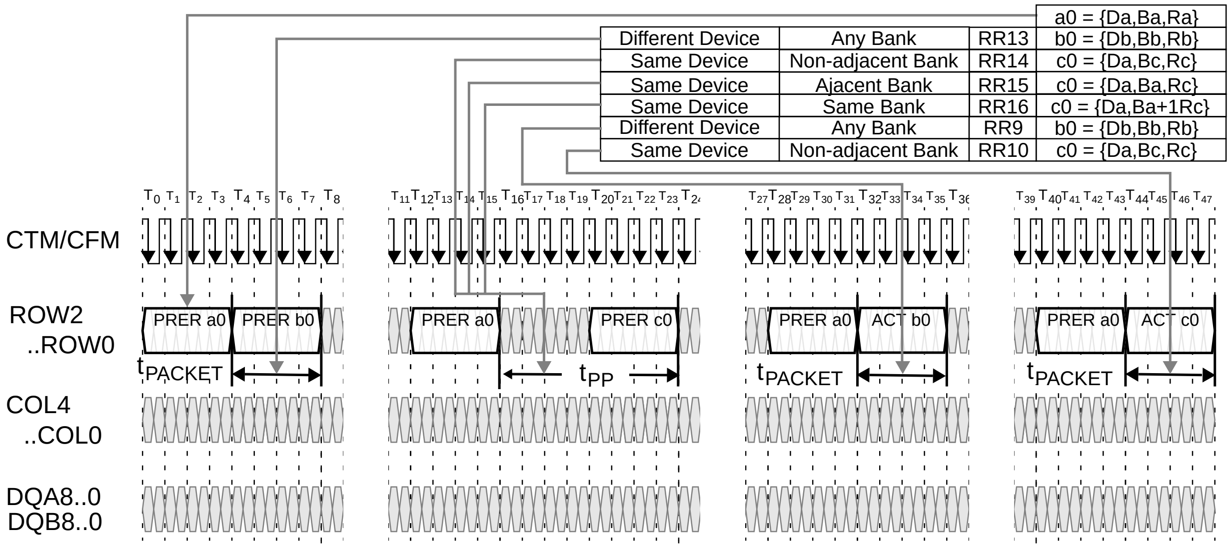


Different Device	Any Bank	RR1
Same Device	Non-adjacent Bank	RR2
Different Device	Any Bank	RR5
Same Device	Non-adjacent Bank	RR6

a0 = {Da,Ba,Ra}
b0 = {Db,Bb,Rb}
c0 = {Da,Bc,Rc}
b0 = {Db,Bb,Rb}
c0 = {Da,Bc,Rc}

Figure 10-3 shows examples of the PRER-to-PRER (RR13, RR14) and PRER-to-ACT (RR9, RR10) command spacings from Table 6-1. The RR15 and RR16 cases (PRER-to-PRER to same or adjacent banks) are not shown, but are similar to RR14. In general, the commands in ROW packets may be spaced an interval t_{PACKET} apart unless they are directed to the same or adjacent banks or unless they are a similar command type (both PRER or both ACT) directed to the same device.

Figure 10-3 Row Packet Example



			a0 = {Da,Ba,Ra}
Different Device	Any Bank	RR13	b0 = {Db,Bb,Rb}
Same Device	Non-adjacent Bank	RR14	c0 = {Da,Bc,Rc}
Same Device	Ajacent Bank	RR15	c0 = {Da,Ba,Rc}
Same Device	Same Bank	RR16	c0 = {Da,Ba+1Rc}
Different Device	Any Bank	RR9	b0 = {Db,Bb,Rb}
Same Device	Non-adjacent Bank	RR10	c0 = {Da,Bc,Rc}

11. Row and Column Cycle Description

Activate: A row cycle begins with the activate (ACT) operation. The activation process is destructive; the act of sensing the value of a bit in a bank's storage cell transfers the bit to the sense amp, but leaves the original bit in the storage cell with an incorrect value.

Restore: Because the activation process is destructive, a hidden operation called restore is automatically performed. The restore operation rewrites the bits in the sense amp back into the storage cells of the activated row of the bank.

Read/Write: While the restore operation takes place, the sense amp may be read (RD) and written (WR) using column operations. If new data is written into the sense amp, it is automatically forwarded to the storage cells of the bank so the data in the activated row and the data in the sense amp remain identical.

Precharge: When both the restore operation and the column operations are completed, the sense amp and bank are precharged (PRE). This leaves them in the proper state to begin another activate operation.

Intervals: The activate operation requires the interval $t_{RCD,MIN}$ to complete. The hidden restore operation requires the interval $t_{RAS,MIN}$ - $t_{RCD,MIN}$ to complete. Column read and write operations are also performed during the $t_{RAS,MIN}$ - $t_{RCD,MIN}$ interval (if more than about four column operations are performed, this interval must be increased). The precharge operation requires the interval $t_{RP,MIN}$ to complete.

Adjacent Banks: An RDRAM with a "s" designation (512K x 18 x 32s) indicates it contains "split banks". This means the sense amps are shared between two adjacent banks. The only exception is that sense amp 0, 15, 30, and 31 are not shared. When a row in a bank is activated, the two adjacent sense amps are connected to (associated with) that bank and are not available for use by the two adjacent banks. These two adjacent banks must remain precharged while the selected bank goes through its activate, restore, read/write, and precharge operations.

For example (referring to the block diagram), if bank 5 is accessed, sense amp 4/5 and sense amp 5/6 will both be loaded with one of the 512 rows (with 1,024 bytes loaded into each sense amp from the 2K byte row – 512 bytes to the DQA side and 512 bytes to the DQB side). While this row from bank 5 is being accessed, no rows may be accessed in banks 4 or 6 because of the sense amp sharing.

12. Precharge Mechanisms

Figure 12-1 shows an example of precharge with the ROWR packet mechanism. The PRER command must occur a time t_{RAS} after the ACT command, and a time t_{RP} before the next ACT command. This timing will serve as a baseline against which the other precharge mechanisms can be compared.

Figure 12-1 Precharge via PRER Command in ROWR Packet

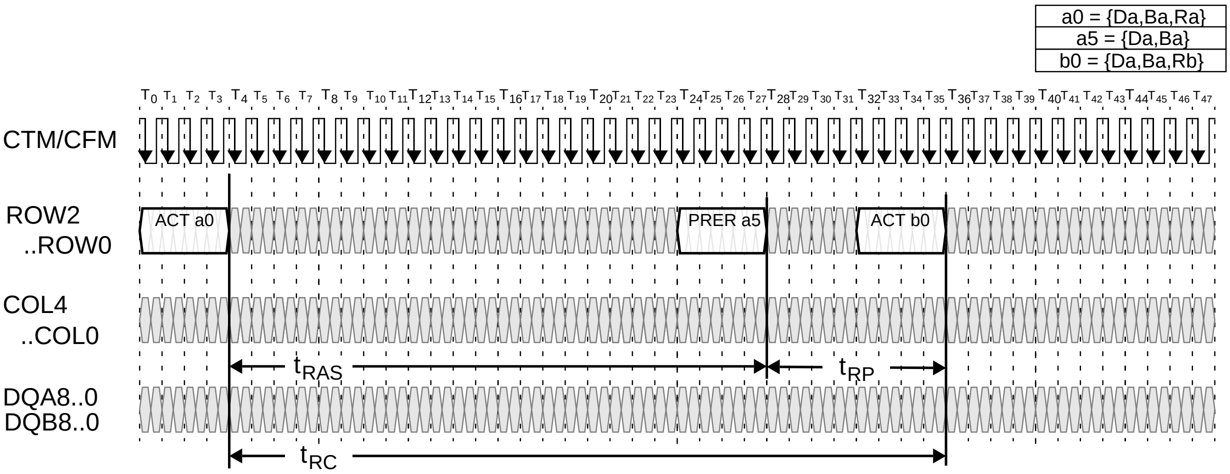


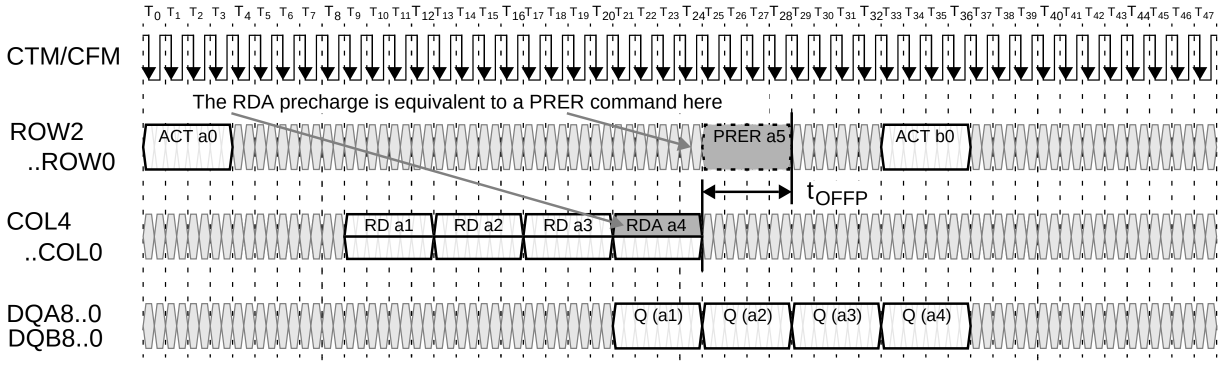
Figure 12-2 (top) shows an example of precharge with a RDA command. A bank is activated with an ROWA packet on the ROW pins. Then, a series of four dualocts are read with RD commands in COLC packets on the COL pins. The fourth of these commands is a RDA, which causes the bank to automatically precharge when the final read has finished. The timing of this automatic precharge is equivalent to a PRER command in an ROWR packet on the ROW pins that is offset a time t_{OFFP} from the COLC packet with the RDA command. The RDA command should be treated as a RD command in a COLC packet as well as a simultaneous (but offset) PRER command in an ROWR packet when analyzing interactions with other packets.

Figure 12-2 (middle) shows an example of precharge with a WRA command. As in the RDA example, a bank is activated with an ROWA packet on the ROW pins. Then, two dualocts are written with WR commands in COLC packets on the COL pins. The second of these commands is a WRA, which causes the bank to automatically precharge when the final write has been retired. The timing of this automatic precharge is equivalent to a PRER command in an ROWR packet on the ROW pins that is offset a time t_{OFFP} from the COLC packet that causes the automatic retire. The WRA command should be treated as a WR command in a COLC packet as well as a simultaneous (but offset) PRER command in an ROWR packet when analyzing interactions with other packets. Note that the automatic retire is triggered by a COLC packet a time t_{RTR} after the COLC packet with the WR command unless the second COLC contains a RD command to the same device. This is described in more detail in Figure 15-1.

Figure 12-2 (bottom) shows an example of precharge with a PREX command in an COLX packet. A bank is activated with an ROWA packet on the ROW pins. Then, a series of four dualocts are read with RD commands in COLC packets on the COL pins. The fourth of these COLC packets includes an COLX packet with a PREX command. This causes the bank to precharge with timing equivalent to a PRER command in an ROWR packet on the ROW pins that is offset a time t_{OFFP} from the COLX packet with the PREX command.

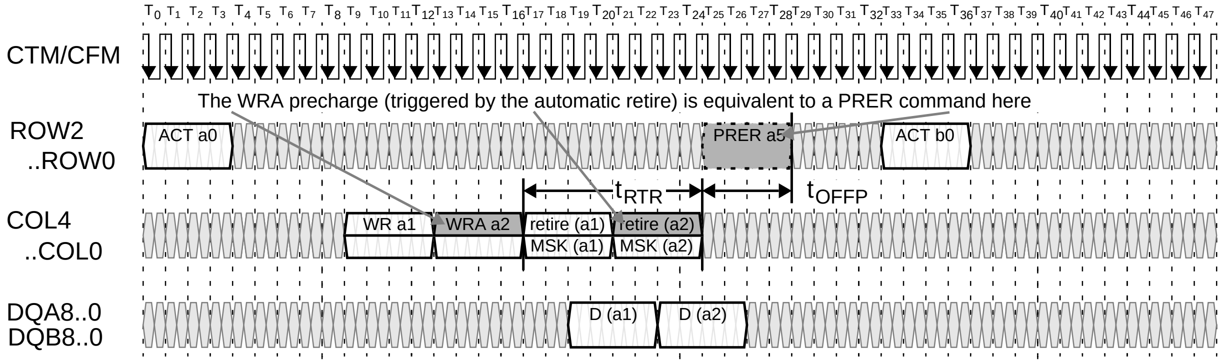
Figure 12-2 Offsets for Alternate Precharge Mechanisms

COLC Packet: RDA Precharge Offset



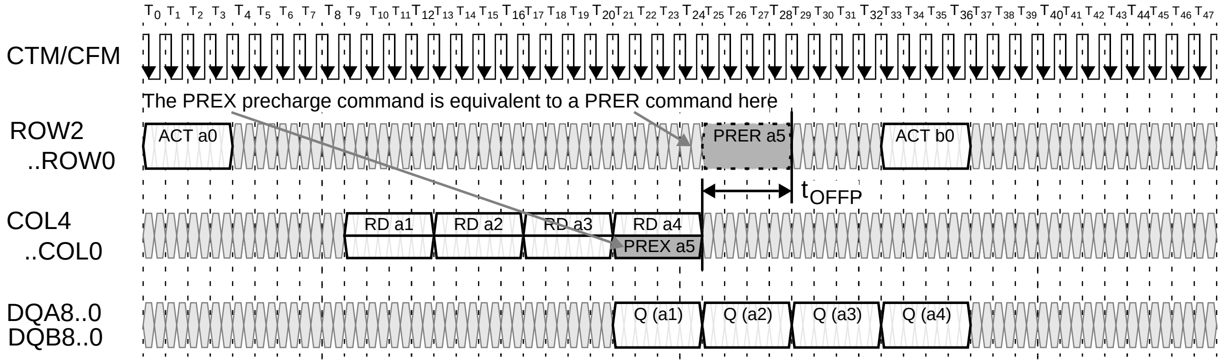
Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	
		a3 = {Da,Ba,Ca3}	a4 = {Da,Ba,Ca4}	a5 = {Da,Ba}

COLC Packet: WDA Precharge Offset



Transaction a: WR	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	a5 = {Da,Ba}

COLX Packet: PREX Precharge Offset



Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	
		a3 = {Da,Ba,Ca3}	a4 = {Da,Ba,Ca4}	a5 = {Da,Ba}

13. Read Transaction - Example

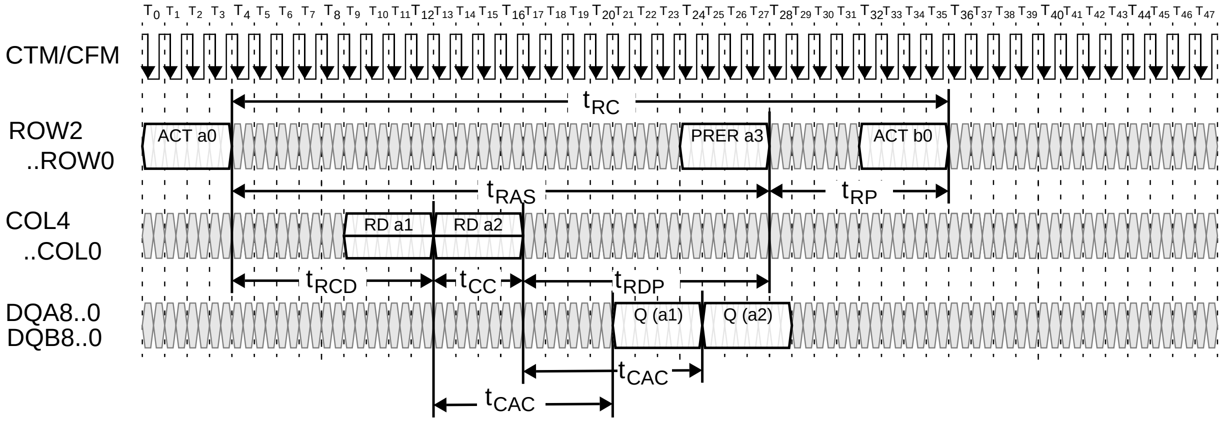
Figure 13-1 shows an example of a read transaction. It begins by activating a bank with an ACT a0 command in an ROWA packet. A time t_{RCD} later a RD a1 command is issued in a COLC packet. Note that the ACT command includes the device, bank, and row address (abbreviated as a0) while the RD command includes device, bank, and column address (abbreviated as a1). A time t_{CAC} after the RD command the read data dualoct Q (a1) is returned by the device. Note that the packets on the ROW and COL pins use the end of the packet as a timing reference point, while the packets on the DQA/DQB pins use the beginning of the packet as a timing reference point.

A time t_{CC} after the first COLC packet on the COL pins a second is issued. It contains a RD a2 command. The a2 address has the same device and bank address as the a1 address (and a0 address), but a different column address. A time t_{CAC} after the second RD command a second read data dualoct Q(a2) is returned by the device.

Next, a PRER a3 command is issued in an ROWR packet on the ROW pins. This causes the bank to precharge so that a different row may be activated in a subsequent transaction or so that an adjacent bank may be activated. The a3 address includes the same device and bank address as the a0, a1, and a2 addresses. The PRER command must occur a time t_{RAS} or more after the original ACT command (the activation operation in any DRAM is destructive, and the contents of the selected row must be restored from the two associated sense amps of the bank during the t_{RAS} interval). The PRER command must also occur a time t_{RDP} or more after the last RD command. Note that the t_{RDP} value shown is greater than the $t_{RDP,MIN}$ specification in "**36.Timing Parameters**". This transaction example reads two dualocts, but there is actually enough time to read three dualocts before t_{RDP} becomes the limiting parameter rather than t_{RAS}. If four dualocts were read, the packet with PRER would need to shift right (be delayed) by one t_{CYCLE} (note-this case is not shown).

Finally, an ACT b0 command is issued in an ROWR packet on the ROW pins. The second ACT command must occur a time t_{RC} or more after the first ACT command and a time t_{RP} or more after the PRER command. This ensures that the bank and its associated sense amps are precharged. This example assumes that the second transaction has the same device and bank address as the first transaction, but a different row address. Transaction b may not be started until transaction a has finished. However, transactions to other banks or other devices may be issued during transaction a.

Figure 13-1 Read Transaction Example



Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: xx	b0 = {Da,Ba,Rb}			

14. Write Transaction - Example

Figure 14-1 shows an example of a write transaction. It begins by activating a bank with an ACT a0 command in an ROWA packet. A time t_{RCD} - t_{RTR} later a WR a1 command is issued in a COLC packet (note that the t_{RCD} interval is measured to the end of the COLC packet with the first retire command). Note that the ACT command includes the device, bank, and row address (abbreviated as a0) while the WR command includes device, bank, and column address (abbreviated as a1). A time t_{CWD} after the WR command the write data dualoct D(a1) is issued. Note that the packets on the ROW and COL pins use the end of the packet as a timing reference point, while the packets on the DQA/DQB pins use the beginning of the packet as a timing reference point.

A time t_{CC} after the first COLC packet on the COL pins a second COLC packet is issued. It contains a WR a2 command. The a2 address has the same device and bank address as the a1 address (and a0 address), but a different column address. A time t_{CWD} after the second WR command a second write data dualoct D(a2) is issued.

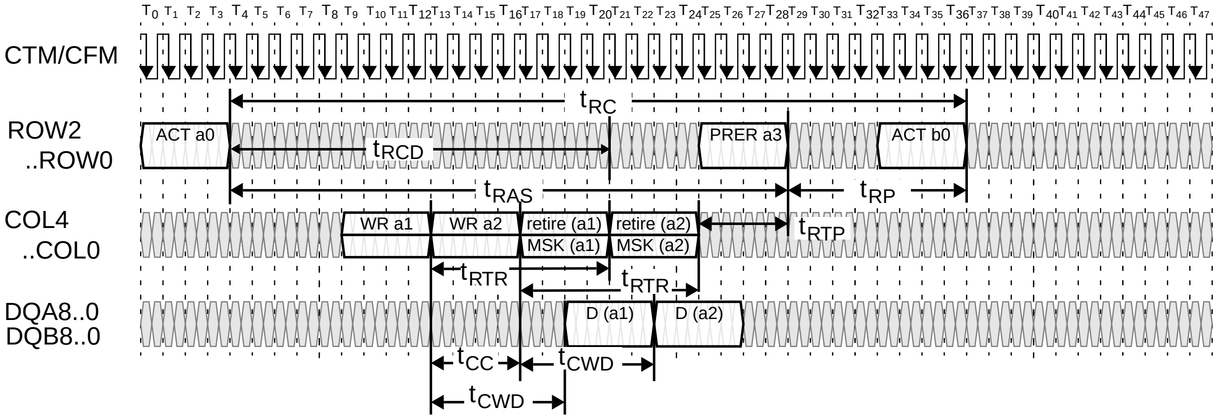
A time t_{RTR} after each WR command an optional COLM packet MSK (a1) is issued, and at the same time a COLC packet is issued causing the write buffer to automatically retire. See Figure 15-1 for more detail on the write/retire mechanism. If a COLM packet is not used, all data bytes are unconditionally written. If the COLC packet which causes the write buffer to retire is delayed, then the COLM packet (if used) must also be delayed.

Next, a PRER a3 command is issued in an ROWR packet on the ROW pins. This causes the bank to precharge so that a different row may be activated in a subsequent transaction or so that an adjacent bank may be activated. The a3 address includes the same device and bank address as the a0, a1, and a2 addresses. The PRER command must occur a time t_{RAS} or more after the original ACT command (the activation operation in any DRAM is destructive, and the contents of the selected row must be restored from the two associated sense amps of the bank during the t_{RAS} interval).

A PRER a3 command is issued in an ROWR packet on the ROW pins. The PRER command must occur a time t_{RTP} or more after the last COLC which causes an automatic retire.

Finally, an ACT b0 command is issued in an ROWR packet on the ROW pins. The second ACT command must occur a time t_{RC} or more after the first ACT command and a time t_{RP} or more after the PRER command. This ensures that the bank and its associated sense amps are precharged. This example assumes that the second transaction has the same device and bank address as the first transaction, but a different row address. Transaction b may not be started until transaction a has finished. However, transactions to other banks or other devices may be issued during transaction a.

Figure 14-1 Write Transaction Example



Transaction a: WR	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: xx	b0 = {Da,Ba,Rb}			

15. Write/Retire - Examples

The process of writing a dualoct into a sense amp of an RDRAM bank occurs in two steps. The first step consists of transporting the write command, write address, and write data into the write buffer. The second step happens when the RDRAM automatically retires the write buffer (with an optional bytemask) into the sense amp. This two-step write process reduces the natural turn-around delay due to the internal bidirectional data pins.

Figure 15-1 (left) shows an example of this two step process. The first COLC packet contains the WR command and an address specifying device, bank and column. The write data dualoct follows a time t_{CWD} later. This information is loaded into the write buffer of the specified device. The COLC packet which follows a time t_{RTR} later will retire the write buffer. The retire will happen automatically unless (1) a COLC packet is not framed (no COLC packet is present and the S bit is zero), or (2) the COLC packet contains a RD command to the same device. If the retire does not take place at time t_{RTR} after the original WR command, then the device continues to frame COLC packets, looking for the first that is not a RD directed to itself. A bytemask MSK(a1) may be supplied in a COLM packet aligned with the COLC that retires the write buffer at time t_{RTR} after the WR command.

The memory controller must be aware of this two-step write/retire process. Controller performance can be improved, but only if the controller design accounts for several side effects.

Figure 15-1 (right) shows the first of these side effects. The first COLC packet has a WR command which loads the address and data into the write buffer. The third COLC causes an automatic retire of the write buffer to the sense amp. The second and fourth COLC packets (which bracket the retire packet) contain RD commands with the same device, bank and column address as the original WR command. In other words, the same dualoct address that is written is read both before and after it is actually retired. The first RD returns the old dualoct value from the sense amp before it is overwritten. The second RD returns the new dualoct value that was just written.

Figure 15-1 Normal Retire (left) and Retire/Read Ordering (right)

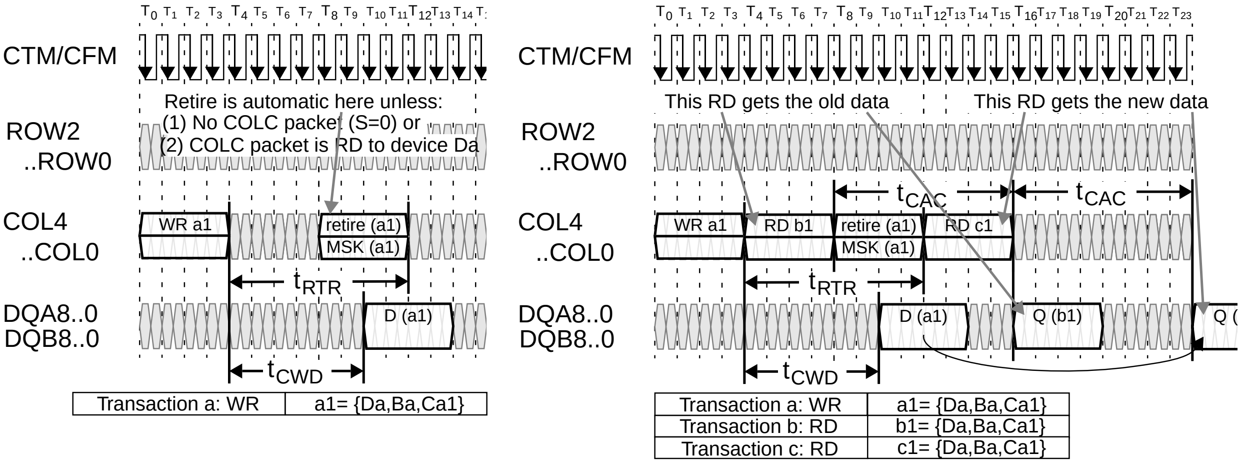
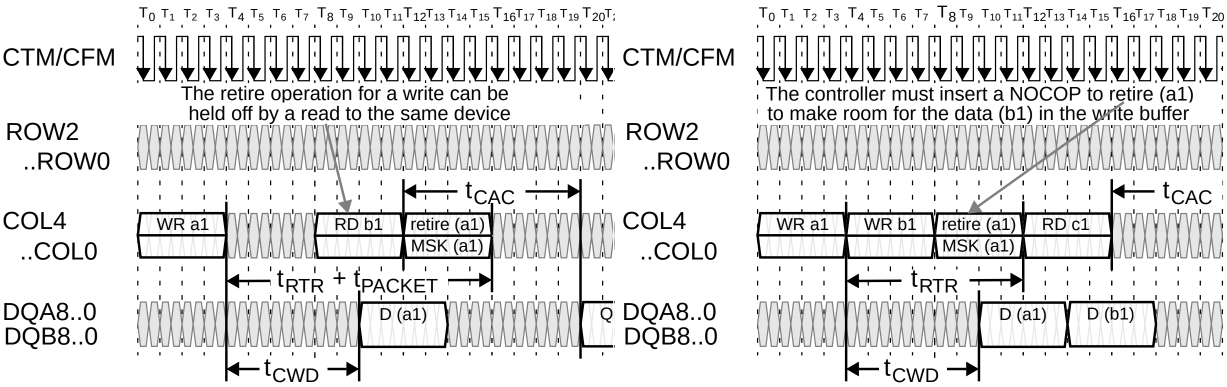


Figure 15-2 (left) shows the result of performing a RD command to the same device in the same COLC packet slot that would normally be used for the retire operation. The read may be to any bank and column address; all that matters is that it is to the same device as the WR command. The retire operation and MSK(a1) will be delayed by a time t_{PACKET} as a result. If the RD command used the same bank and column address as the WR command, the old data from the sense amp would be returned. If many RD commands to the same device were issued instead of the single one that is shown, then the retire operation would be held off an arbitrarily long time. However, once a RD to another device or a WR or NOCOP to any device is issued, the retire will take place. Figure 15-2 (right) illustrates a situation in which the controller wants to issue a WR-WR-RD COLC packet sequence, with all commands addressed to the same device, but addressed to any combination of banks and columns.

The RD will prevent a retire of the first WR from automatically happening. But the first dualoct D(a1) in the write buffer will be overwritten by the second WR dualoct D(b1) if the RD command is issued in the third COLC packet. Therefore, it is required in this situation that the controller issue a NOCOP command in the third COLC packet, delaying the RD command by a time of t_{PACKET}. This situation is explicitly shown in Table 8-1 for the cases in which $t_{CCDELAY}$ is equal to t_{RTR}.

Figure 15-2 Retire Held Off by Read (left) and Controller Forces WWR Gap (right)

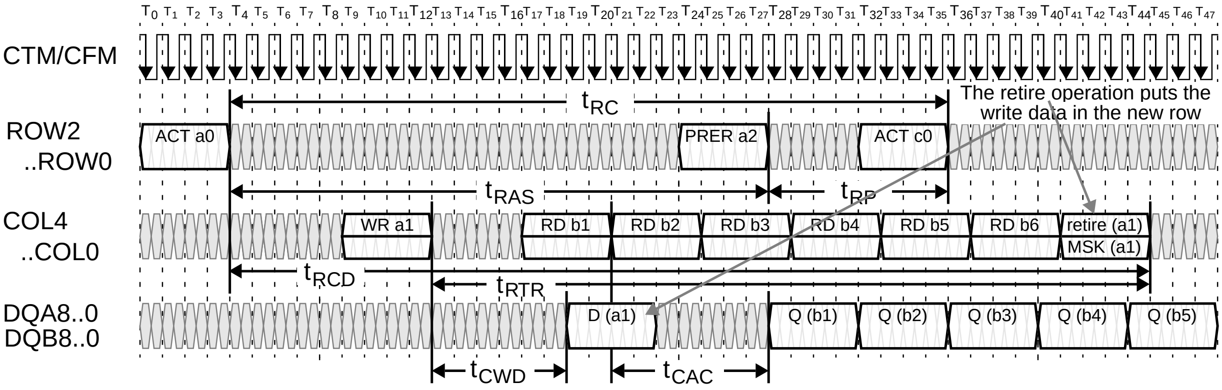


Transaction a: WR	a1= {Da,Ba,Ca1}
Transaction b: RD	b1= {Da,Bb,Cb1}

Transaction a: WR	a1= {Da,Ba,Ca1}
Transaction b: WR	b1= {Da,Bb,Cb1}
Transaction c: RD	c1= {Da,Bc,Cc1}

Figure 15-3 shows a possible result when a retire is held off for a long time (an extended version of Figure 15-2-left). After a WR command, a series of six RD commands are issued to the same device (but to any combination of bank and column addresses). In the meantime, the bank Ba to which the WR command was originally directed is precharged, and a different row Rc is activated. When the retire is automatically performed, it is made to this new row, since the write buffer only contains the bank and column address, not the row address. The controller can insure that this doesn't happen by never precharging a bank with an unretired write buffer. Note that in a system with more than one RDRAM, there will never be more than two RDRAMs with unretired write buffers. This is because a WR command issued to one device automatically retires the write buffers of all other devices written a time t_{RTR} before or earlier.

Figure 15-3 Retire Held Off by Reads to Same Device, Write Buffer Retired to New Row



Transaction a: WR	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2 = {Da,Ba}
Transaction b: RD	b1 = {Da,Bb,Cb1}	b2 = {Da,Bb,Cb2}	b3= {Da,Bb,Cb3}
	b4 = {Da,Bb,Cb4}	b5 = {Da,Bb,Cb5}	b6 = {Da,Bb,Cb6}
Transaction c: WR	c0 = {Da,Ba,Rc}		

WARNING
This sequence is hazardous
and must be used with caution

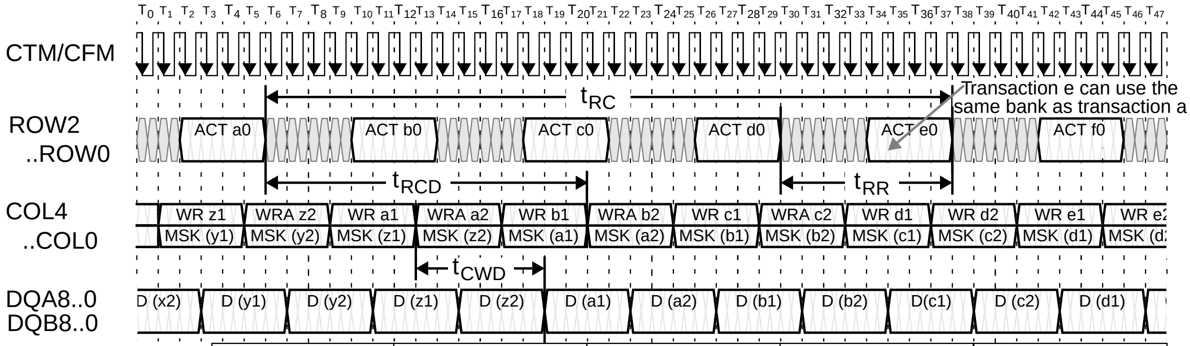
16. Interleaved Write - Example

Figure 16-1 shows an example of an interleaved write transaction. Transactions similar to the one presented in Figure 14-1 are directed to non-adjacent banks of a single RDRAM. This allows a new transaction to be issued once every t_{RR} interval rather than once every t_{RC} interval (four times more often). The DQ data pin efficiency is 100% with this sequence.

With two dualocts of data written per transaction, the COL, DQA, and DQB pins are fully utilized. Banks are precharged using the WRA autoprecharge option rather than the PRER command in an ROWR packet on the ROW pins.

In this example, the first transaction is directed to device Da and bank Ba. The next three transactions are directed to the same device Da, but need to use different, non-adjacent banks Bb, Bc, Bd so there is no bank conflict. The fifth transaction could be redirected back to bank Ba without interference, since the first transaction would have completed by then (t_{RC} has elapsed). Each transaction may use any value of row address (Ra, Rb, ...) and column address (Ca1, Ca2, Cb1, Cb2, ...).

Figure 16-1 Interleaved Write Transaction with Two Dualoct Data Length

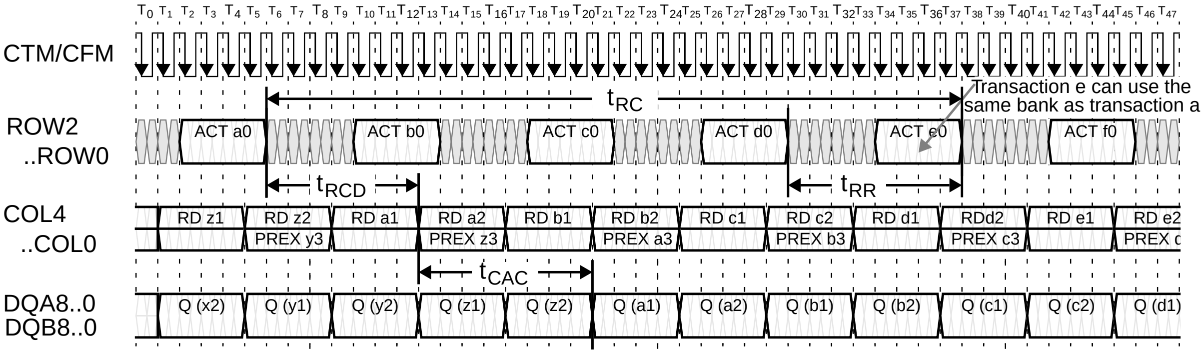


Transaction y: WR	y0 = {Da,Ba+4,Ry}	y1 = {Da,Ba+4,Cy1}	y2= {Da,Ba+4,Cy2}	y3 = {Da,Ba+4}
Transaction z: WR	z0 = {Da,Ba+6,Rz}	z1 = {Da,Ba+6,Cz1}	z2= {Da,Ba+6,Cz2}	z3 = {Da,Ba+6}
Transaction a: WR	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2= {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: WR	b0 = {Da,Ba+2,Rb}	b1 = {Da,Ba+2,Cb1}	b2= {Da,Ba+2,Cb2}	b3 = {Da,Ba+2}
Transaction c: WR	c0 = {Da,Ba+4,Rc}	c1 = {Da,Ba+4,Cc1}	c2= {Da,Ba+4,Cc2}	c3 = {Da,Ba+4}
Transaction d: WR	d0 = {Da,Ba+6,Rd}	d1 = {Da,Ba+6,Cd1}	d2= {Da,Ba+6,Cd2}	d3 = {Da,Ba+6}
Transaction e: WR	e0 = {Da,Ba,Re}	e1 = {Da,Ba,Ce1}	e2= {Da,Ba,Ce2}	e3 = {Da,Ba}
Transaction f: WR	f0 = {Da,Ba+2,Rf}	f1 = {Da,Ba+2,Cf1}	f2= {Da,Ba+2,Cf2}	f3 = {Da,Ba+2}

17. Interleaved Read - Example

Figure 17-1 shows an example of interleaved read transactions. Transactions similar to the one presented in Figure 13-1 are directed to non-adjacent banks of a single RDRAM. The address sequence is identical to the one used in the previous write example. The DQ data pins efficiency is also 100%. The only difference with the write example (aside from the use of the RD command rather than the WR command) is the use of the PREX command in a COLX packet to precharge the banks rather than the RDA command. This is done because the PREX is available for a readtransaction but is not available for a masked write transaction.

Figure 17-1 Interleaved Read Transaction with Two Dualoct Data Length



Transaction y: RD	y0 = {Da,Ba+4,Ry}	y1 = {Da,Ba+4,Cy1}	y2= {Da,Ba+4,Cy2}	y3 = {Da,Ba+4}
Transaction z: RD	z0 = {Da,Ba+6,Rz}	z1 = {Da,Ba+6,Cz1}	z2= {Da,Ba+6,Cz2}	z3 = {Da,Ba+6}
Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2= {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: RD	b0 = {Da,Ba+2,Rb}	b1 = {Da,Ba+2,Cb1}	b2= {Da,Ba+2,Cb2}	b3 = {Da,Ba+2}
Transaction c: RD	c0 = {Da,Ba+4,Rc}	c1 = {Da,Ba+4,Cc1}	c2= {Da,Ba+4,Cc2}	c3 = {Da,Ba+4}
Transaction d: RD	d0 = {Da,Ba+6,Rd}	d1 = {Da,Ba+6,Cd1}	d2= {Da,Ba+6,Cd2}	d3 = {Da,Ba+6}
Transaction e: RD	e0 = {Da,Ba,Re}	e1 = {Da,Ba,Ce1}	e2= {Da,Ba,Ce2}	e3 = {Da,Ba}
Transaction f: RD	f0 = {Da,Ba+2,Rf}	f1 = {Da,Ba+2,Cf1}	f2= {Da,Ba+2,Cf2}	f3 = {Da,Ba+2}

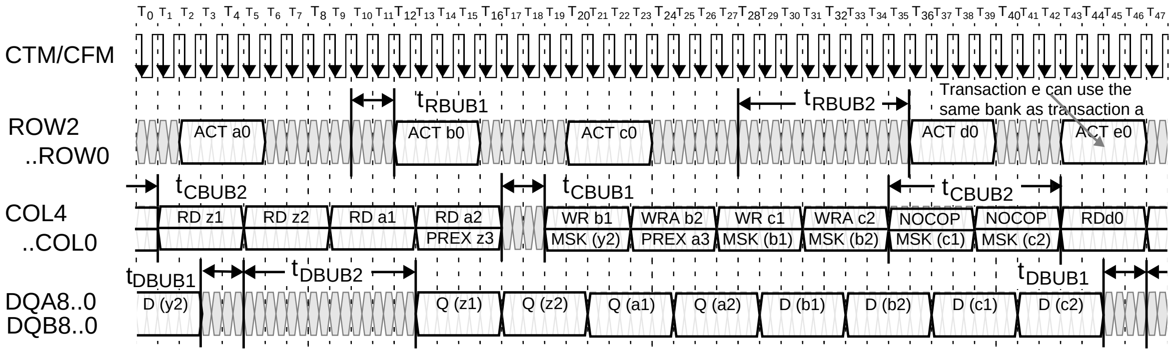
18. Interleaved RRWW - Example

Figure 18-1 shows a steady-state sequence of 2-dualoct RD/RD/WR/WR.. transactions directed to non-adjacent banks of a single RDRAM. This is similar to the interleaved write and read examples in Figure 16-1 and Figure 17-1 except that bubble cycles need to be inserted by the controller at read/write boundaries. The DQ data pin efficiency for the example in Figure 18-1 is 32/42 or 76%. If there were more RDRAMs on the Channel, the DQ pin efficiency would approach 32/34 or 94% for the two-dualoct RRWW sequence (this case is not shown).

In Figure 18-1, the first bubble type t_{CBUB1} is inserted by the controller between a RD and WR command on the COL pins. This bubble accounts for the round-trip propagation delay that is seen by read data, and is explained in detail in Figure 4-1. This bubble appears on the DQA and DQB pins as t_{DBUB1} between a write data dualoct D and read data dualoct Q. This bubble also appears on the ROW pins as t_{RBUB1}.

The second bubble type t_{CBUB2} is inserted (as a NOCOP command) by the controller between a WR and RD command on the COL pins when there is a WR-WR-RD sequence to the same device. This bubble enables write data to be retired from the write buffer without being lost, and is explained in detail in Figure 15-2. There would be no bubble if address c0 and address d0 were directed to different devices. This bubble appears on the DQA and DQB pins as t_{DBUB2} between a write data dualoct D and read data dualoct Q. This bubble also appears on the ROW pins as t_{RBUB2}.

Figure 18-1 Interleaved RRWW Sequence with Two Dualoct Data Length



Transaction y: WR	y0 = {Da,Ba+4,Ry}	y1 = {Da,Ba+4,Cy1}	y2= {Da,Ba+4,Cy2}	y3 = {Da,Ba+4}
Transaction z: RD	z0 = {Da,Ba+6,Rz}	z1 = {Da,Ba+6,Cz1}	z2= {Da,Ba+6,Cz2}	z3 = {Da,Ba+6}
Transaction a: RD	a0 = {Da,Ba,Ra}	a1 = {Da,Ba,Ca1}	a2= {Da,Ba,Ca2}	a3 = {Da,Ba}
Transaction b: WR	b0 = {Da,Ba+2,Rb}	b1 = {Da,Ba+2,Cb1}	b2= {Da,Ba+2,Cb2}	b3 = {Da,Ba+2}
Transaction c: WR	c0 = {Da,Ba+4,Rc}	c1 = {Da,Ba+4,Cc1}	c2= {Da,Ba+4,Cc2}	c3 = {Da,Ba+4}
Transaction d: RD	d0 = {Da,Ba+6,Rd}	d1 = {Da,Ba+6,Cd1}	d2= {Da,Ba+6,Cd2}	d3 = {Da,Ba+6}
Transaction e: RD	e0 = {Da,Ba,Re}	e1 = {Da,Ba,Ce1}	e2= {Da,Ba,Ce2}	e3 = {Da,Ba}
Transaction f: WR	f0 = {Da,Ba+2,Rf}	f1 = {Da,Ba+2,Cf1}	f2= {Da,Ba+2,Cf2}	f3 = {Da,Ba+2}

19. Control Register Transactions

The RDRAM has two CMOS input pins SCK and CMD and two CMOS input/output pins SIO0 and SIO1. These provide serial access to a set of control registers in the RDRAM. These control registers provide configuration information to the controller during the initialization process. They also allow an application to select the appropriate operating mode of the RDRAM. SCK (serial clock) and CMD (command) are driven by the controller to all RDRAMs in parallel. SIO0 and SIO1 are connected (in a daisy chain fashion) from one RDRAM to the next. In normal operation, the data on SIO0 is repeated on SIO1, which connects to SIO0 of the next RDRAM (the data is repeated from SIO1 to SIO0 for a read data packet). The controller connects to SIO0 of the first RDRAM.

Write and read transactions are each composed of four packets, as shown in Figure 19-1 and Figure 19-2. Each packet consists of 16 bits, as summarized in Table 20-1 and Table 20-2. The packet bits are sampled on the falling edge of SCK. A transaction begins with a SRQ (Serial Request) packet. This packet is framed with a 11110000 pattern on the CMD input (note that the CMD bits are sampled on both the falling edge and the rising edge of SCK). The SRQ packet contains the SOP3..SOP0 (Serial Opcode) field, which selects the transaction type. The SDEV5..SDEV0 (Serial Device address) selects one of the 32 RDRAMs. If SBC (Serial Broadcast) is set, then all RDRAMs are selected. The SA (Serial Address) packet contains a 12 bit address for selecting a control register.

A write transaction has a SD (Serial Data) packet next. This contains 16 bits of data that is written into the selected control register. A SINT (Serial Interval) packet is last, providing some delay for any side-effects to take place. A read transaction has a SINT packet, then a SD packet. This provides delay for the selected RDRAM to access the control register. The SD read data packet travels in the opposite direction (towards the controller) from the other packet types. The SCK cycle time will accommodate the total delay.

Figure 19-1 Serial Write (SWR) Transaction to Control Register

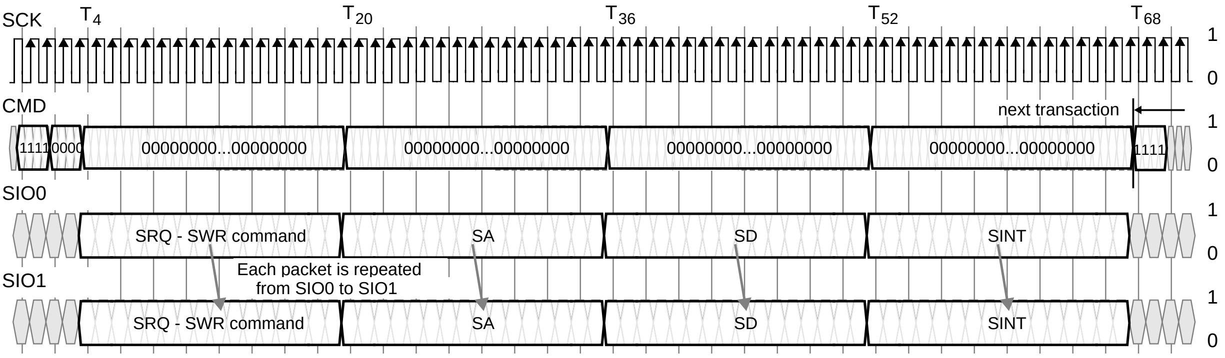
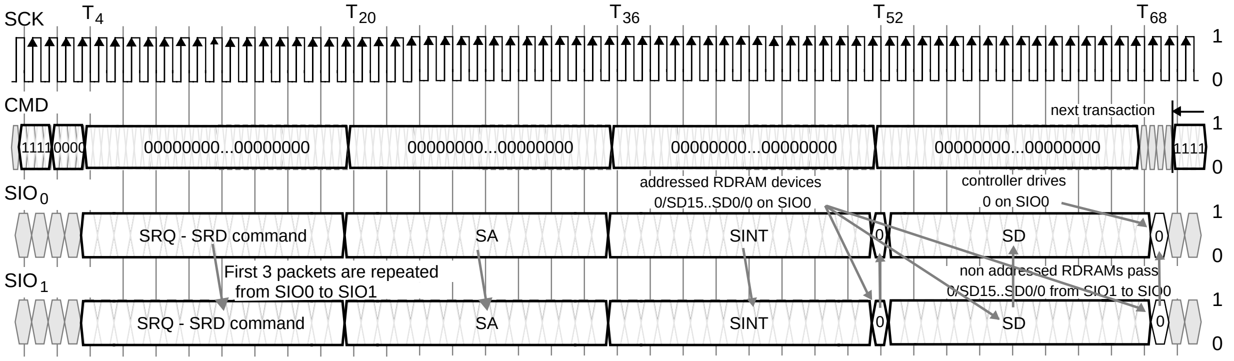


Figure 19-2 Serial Read (SRD) Transaction Control Register



20. Control Register Packets

Table 20-1 summarizes the formats of the four packet types for control register transactions. Table 20-2 summarizes the fields that are used within the packets.

Figure 20-1 shows the transaction format for the SETR, CLRR, and SETF commands. These transactions consist of a single SRQ packet, rather than four packets like the SWR and SRD commands. The same framing sequence on the CMD input is used, however. These commands are used during initialization prior to any control register read or write transactions.

Figure 20-1 SETR, CLRR, SETF Transaction

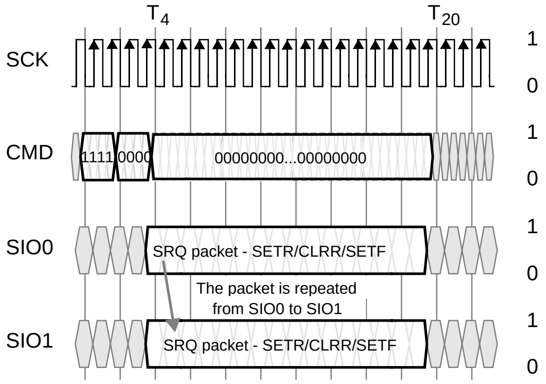


Table 20-1 Control Register Packet Formats

SCK Cycle	SIO0 or SIO1 for SRQ	SIO0 or SIO1 for SA	SIO0 or SIO1 for SINT	SIO0 or SIO1 for SD	SCK Cycle	SIO0 or SIO1 for SRQ	SIO0 or SIO1 for SA	SIO0 or SIO1 for SINT	SIO0 or SIO1 for SD
0	rsrv	rsrv	0	SD15	8	SOP1	SA7	0	SD7
1	rsrv	rsrv	0	SD14	9	SOP0	SA6	0	SD6
2	rsrv	rsrv	0	SD13	10	SBC	SA5	0	SD5
3	rsrv	rsrv	0	SD12	11	SDEV4	SA4	0	SD4
4	rsrv	SA11	0	SD11	12	SDEV3	SA3	0	SD3
5	SDEV5	SA10	0	SD10	13	SDEV2	SA2	0	SD2
6	SOP3	SA9	0	SD9	14	SDEV1	SA1	0	SD1
7	SOP2	SA8	0	SD8	15	SDEV0	SA0	0	SD0

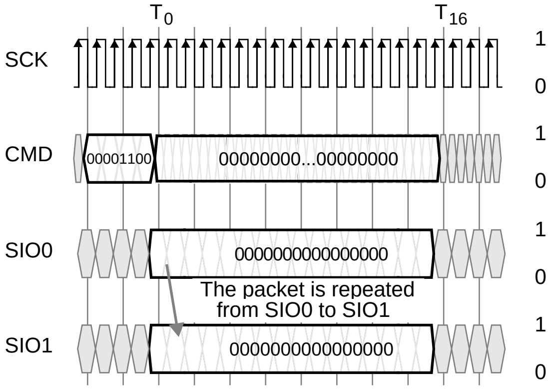
Table 20-2 Field Description for Control Register Packets

Field	Description
rsrv	Reserved. Should be driven as “0” by controller.
SOP3..SOP0	0000 - SRD. Serial read of control register {SA11..SA0} of RDRAM {SDEV5..SDEV0}.
	0001 - SWR. Serial write of control register {SA11..SA0} of RDRAM {SDEV5..SDEV0}.
	0010 - SETR. Set Reset bit, all control registers assume their reset values.[Note] 16 t_{SCYCLE} delay until CLRR command.
	0100 - SETF. Set fast (normal) clock mode. 4 t_{SCYCLE} delay until next command.
	1011 - CLRR. Clear Reset bit, all control registers retain their reset values.[Note] 4 t_{SCYCLE} delay until next command.
	1111 - NOP. No serial operation.
	0011, 0101 – 1010, 1100 – 1110 – RSRV. Reserved encodings.
SDEV5..SDEV0	Serial device. Compared to SDEVID5..SDEVID0 field of INIT control register field to select the RDRAM to which the transaction is directed.
SBC	Serial broadcast. When set, RDRAMs ignore {SDEV5..SDEV0} for RDRAM selection.
SA11..SA0	Serial address. Selects which control register of the selected RDRAM is read or written.
SD15..SD0	Serial data. The 16 bits of data written to or read from the selected control register of the selected RDRAM.

Note The SETR and CLRR commands must always be applied in two successive transactions to RDRAMs; i.e. they may not be used in isolation. This is called “SETR/CLRR Reset”.

21. Initialization

Figure 21-1 SIO Pin Reset Sequence



The packet is repeated from SIO0 to SIO1

Initialization refers to the process that a controller must go through after power is applied to the system or the system is reset. The controller prepares the RDRAM sub-system for normal Channel operation by (primarily) using a sequence of control register transactions on the serial CMOS pins. The following steps outline the sequence seen by the various memory subsystem components (including the RDRAM components) during initialization. This sequence is available in the form of reference code. Contact Rambus Inc. for more information.

1.0 Start Clocks

This step calculates the proper clock frequencies for PClk (controller logic), SynClk (RAC block), RefClk (DRCG component), CTM (RDRAM component), and SCK (SIO block).

2.0 RAC Initialization

This step causes the INIT block to generate a sequence of pulses which resets the RAC, performs RAC maintainance operations, and measures timing intervals in order to ensure clock stability.

3.0 RDRAM Initialization

This stage performs most of the steps needed to initialize the RDRAMs. The rest are performed in stages 5.0, 6.0, and 7.0. All of the steps in 3.0 are carried out through the SIO block interface.

3.1/3.2 SIO Reset

After a delay of t_{PAUSE} from step 1.0, this reset operation is performed before any SIO control register read or write transactions. It clears six registers (TEST34, CCA, CCB, SKIP, TEST78, and TEST79) and places the INIT register into a special state (all bits cleared except SKP and SDEVID fields are set to ones).

3.3 Write TEST77 Register

The TEST77 register must be explicitly written with zeros before any other registers are read or written.

3.4 Write TCYCLE Register

The TCYCLE register is written with the cycle time t_{CYCLE} of the CTM clock (for Channel and RDRAMs) in units of 64ps. The t_{CYCLE} value is determined in stage 1.0.

3.5 Write SDEVID Register

The SDEVID (serial device identification) register of the RDRAM is written with a unique address value so that directed SIO read and write transactions can be performed. This address value increases from 0 to 31 according to the distance an RDRAM is from the ASIC component on the SIO bus (the closest RDRAM is address 0).

3.6 Write DEVID Register

The DEVID (device identification) register of the RDRAM is written with a unique address value so that directed memory read and write transactions can be performed. This address value increases from 0 to 31. The DEVID value is not necessarily the same as the SDEVID value. RDRAMs are sorted into regions of the same core configuration (number of bank, row, and column address bits and core type).

3.7 Write PDNX, PDNXA Registers

The PDNX and PDNXA registers are written with values that are used to measure the timing intervals connected with an exit from the PDN (powerdown) power state.

3.8 Write NAPX Register

The NAPX register is written with values that are used to measure the timing intervals connected with an exit from the NAP power state.

3.9 Write TPARM Register

The TPARM register is written with values which determine the time interval between a COL packet with a memory read command and the Q packet with the read data on the Channel. The values written set the RDRAM to the minimum value permitted for the system. This will be adjusted later in stage 6.0.

3.10 Write TCDLY1 Register

The TCDLY1 register is written with values which determine the time interval between a COL packet with a memory read command and the Q packet with the read data on the Channel. The values written set the RDRAM to the minimum value permitted for the system. This will be adjusted later in stage 6.0.

3.11 Write TFRM Register

The TFRM register is written with a value that is related to the t_{RCD} parameter for the system. The t_{RCD} parameter is the time interval between a ROW packet with an activate command and the COL packet with a read or write command.

3.12 SETR/CLRR

First write the following registers with the indicated values:

TEST78	0004_{16}
TEST34	0040_{16}

Next, the RDRAM is given a SETR command and a CLRR command through the SIO block. This sequence performs a second reset operation on the RDRAMs. Then the TEST34 and TEST78 registers are rewritten with zero, in that order.

3.13 Write CCA and CCB Registers

These registers are written with a value halfway between their minimum and maximum values. This shortens the time needed for the RDRAMs to reach their steady-state current control values in stage 5.0.

3.14 Powerdown Exit

The RDRAM is in the PDN power state at this point. A broadcast PDNExit command is performed by the SIO block to place the RDRAMs in the RLX (relax) power state in which they are ready to receive ROW packets.

3.15 SETF

The RDRAM is given a SETF command through the SIO block. One of the operations performed by this step is to generate a value for the AS (autoskip) bit in the SKIP register and fix the RDRAM to a particular read domain.

4.0 Controller Configuration

This stage initializes the controller block. Each step of this stage will set a field of the ConfigRMC[63:0] bus to the appropriate value. Other controller implementations will have similar initialization requirements, and this stage may be used as a guide.

4.1 Initial Read Data Offset

The ConfigRMC bus is written with a value which determines the time interval between a COL packet with a memory read command and the Q packet with the read data on the Channel. The value written sets RMC.d1 to the minimum value permitted for the system. This will be adjusted later in stage 6.0.

4.2 Configure Row/Column Timing

This step determines the values of the $t_{RAS,MIN}$, $t_{RP,MIN}$, $t_{RC,MIN}$, $t_{RCD,MIN}$, $t_{RR,MIN}$, and $t_{PP,MIN}$ RDRAM timing parameters that are present in the system. The ConfigRMC bus is written with values that will be compatible with all RDRAM devices that are present.

4.3 Set Refresh Interval

This step determines the values of the $t_{REF,MAX}$ RDRAM timing parameter that are present in the system. The ConfigRMC bus is written with a value that will be compatible with all RDRAM devices that are present.

4.4 Set Current Control Interval

This step determines the values of the $t_{CCTRL,MAX}$ RDRAM timing parameter that are present in the system. The ConfigRMC bus is written with a value that will be compatible with all RDRAM devices that are present.

4.5 Set Slew Rate Control Interval

This step determines the values of the $t_{TEMP,MAX}$ RDRAM timing parameter that are present in the system. The ConfigRMC bus is written with a value that will be compatible with all RDRAM devices that are present.

4.6 Set Bank/Row/Col Address Bits

This step determines the number of RDRAM bank, row, and column address bits that are present in the system. It also determines the RDRAM core types (independent, doubled, or split) that are present. The ConfigRMC bus is written with a value that will be compatible with all RDRAM devices that are present.

5.0 RDRAM Current Control

This step causes the INIT block to generate a sequence of pulses which performs RDRAM maintenance operations.

6.0 RDRAM Core, Read Domain Initialization

This stage completes the RDRAM initialization

6.1 RDRAM Core Initialization

A sequence of 192 memory refresh transactions is performed in order to place the cores of all RDRAMs into the proper operating state.

6.2 RDRAM Read Domain Initialization

A memory write and memory read transaction is performed to the RDRAM to determine which read domain the RDRAM occupies. The programmed delay of the RDRAM is then adjusted so the total RDRAM read delay (propagation delay plus programmed delay) is constant. The TPARM and TCDLY1 registers of the RDRAM is rewritten with the appropriate read delay values. The ConfigRMC bus is also rewritten with an updated value.

7.0 Other RDRAM Register Fields

This stage rewrites the INIT register with the final values of the LSR, NSR, and PSR fields.

In essence, the controller must read all the read-only configuration registers of all RDRAMs (or it must read the SPD device present on each RIMM), it must process this information, and then it must write all the read-write registers to place the RDRAMs into the proper operating mode.

Initialization Note :

1. During the initialization process, it is necessary for the controller to perform 128 current control operations (3xCAL, 1xCAL/SAM) and one temperature calibrate operation (TCEN/TCAL) after reset or after powerdown (PDN) exit.
2. The behavior of μPD488588 at initialization is as follows. It is distinguished by the "S28IECO" bit in the SPD. S28IECO=1: Upon powerup, the device enters PDN state. The serial operations SETR, CLRR, and SETF require a SDEVID match.
   See the document detailing the reference initialization procedure for more information on how to handle this in a system.
3. After the step of equalizing the total read delay of the RDRAM has been completed (i.e. after the TCDLY0 and TCDLY1 fields have been written for the final time), a single final memory read transaction should be made to the RDRAM in order to ensure that the output pipeline stages have been cleared.
4. The SETF command (in the serial SRQ packet) should only be issued once during the Initialization process, as should the SETR and CLRR commands.
5. The CLRR command (in the serial SRQ packet) leaves some of the contents of the memory core in an indeterminate state.

22. Control Register Summary

Table 22-1 summarizes the RDRAM control registers. Detail is provided for each control register in Figure 22-1. Read-only bits which are shaded gray are unused and return zero. Read-write bits which are shaded gray are reserved and should always be written with zero. The RIMM™ SPD Application Note (DL-0054) of Rambus Inc. describes additional read-only configuration registers which are present on Direct RIMMs.

The state of the register fields are potentially affected by the IO Reset operation or the SETR/CLRR operation. This is indicated in the text accompanying each register diagram.

Table 22-1 Control Register Summary (1/2)

SA11..SA0	Register	Field	read-write/ read-only	Description
021_{16}	INIT	SDEVID	read-write, 6 bits	Serial device ID. Device address for control register read/write.
		PSX	read-write, 1 bit	Power select exit. PDN/NAP exit with device addr on DQA5..0.
		SRP	read-write, 1 bit	SIO repeater. Used to initialize RDRAM.
		NSR	read-write, 1 bit	NAP self-refresh. Enables self-refresh in NAP mode.
		PSR	read-write, 1 bit	PDN self-refresh. Enables self-refresh in PDN mode.
		LSR	read-write, 1 bit	Low power self-refresh. Enables low power self-refresh.
		TEN	read-write, 1 bit	Temperature sensing enable.
		TSQ	read-write, 1 bit	Temperature sensing output.
		DIS	read-write, 1 bit	RDRAM disable.
		IDM	read-write, 1 bit	Interleaved Device Mode enable.
022_{16}	TEST34	TEST34	read-write, 16 bits	Test register. Do not read or write after SIO reset.
023_{16}	CNFGA	REFBIT	read-only, 3 bits	Refresh bank bits. Used for multi-bank refresh.
		DBL	read-only, 1 bit	Double. Specifies doubled-bank architecture.
		MVER	read-only, 6 bits	Manufacturer version. Manufacturer identification number.
		PVER	read-only, 6 bits	Protocol version. Specifies version of Direct protocol supported.
024_{16}	CNFGB	BYT	read-only, 1 bit	Byte. Specifies an 8-bit or 9-bit byte size.
		DEVTYP	read-only, 3 bits	Device type. Device can be RDRAM or some other device category.
		SPT	read-only, 1 bit	Split-core. Each core half is an individual dependent core.
		CORG	read-only, 6 bits	Core organization. Bank, row, column address field sizes.
		SVER	read-only, 6 bits	Stepping version. Mask version number.
040_{16}	DEVID	DEVID	read-write, 5 bits	Device ID. Device address for memory read/write.
041_{16}	REFB	REFB	read-write, 4 bits	Refresh bank. Next bank to be refreshed by self-refresh.
042_{16}	REFR	REFR	read-write, 9 bits	Refresh row. Next row to be refreshed by REFA, self-refresh.
043_{16}	CCA	CCA	read-write, 7 bits	Current control A. Controls I_{OL} output current for DQA.
		ASYMA	read-write, 2 bits	Asymmetry control. Controls asymmetry of V_{OL}/V_{OH} swing for DQA.
044_{16}	CCB	CCB	read-write, 7 bits	Current control B. Controls I_{OL} output current for DQB.
		ASYMB	read-write, 2 bits	Asymmetry control. Controls asymmetry of V_{OL}/V_{OH} swing for DQB.
045_{16}	NAPX	NAPXA	read-write, 5 bits	NAP exit. Specifies length of NAP exit phase A.
		NAPX	read-write, 5 bits	NAP exit. Specifies length of NAP exit phase A + phase B.
		DQS	read-write, 1 bit	DQ select. Selects CMD framing for NAP/PDN exit.
046_{16}	PDNXA	PDNXA	read-write, 13 bits	PDN exit. Specifies length of PDN exit phase A.

Table 22-1 Control Register Summary (2/2)

SA11..SA0	Register	Field	read-write/ read-only	Description
047_{16}	PDNX	PDNX	read-write, 13 bits	PDN exit. Specifies length of PDN exit phase A + phase B.
048_{16}	TPARM	TCAS	read-write, 2 bits	t_{CAS-C} core parameter. Determines t_{OFFP} datasheet parameter.
		TCLS	read-write, 2 bits	t_{CLS-C} core parameter. Determines t_{CAC} and t_{OFFP} parameters.
		TCDLY0	read-write, 3 bits	$t_{CDLY0-C}$ core parameter. Programmable delay for read data.
049_{16}	TFRM	TFRM	read-write, 4 bits	t_{FRM-C} core parameter. Determines ROW - COL packet framing interval.
$04a_{16}$	TCDLY1	TCDLY1	read-write, 3 bits	t_{CDLY-1} core parameter. Programmable delay for read data.
$04c_{16}$	TCYCLE	TCYCLE	read-write, 14 bits	t_{CYCLE} datasheet parameter. Specifies cycle time in 64ps units.
$04b_{16}$	SKIP	AS	read-only, 1 bit	Autoskip value established by the SETF command.
		MSE	read-write, 1 bit	Manual skip enable. Allows the MS value to override the AS value.
		MS	read-write, 1 bit	Manual skip value.
$04d_{16}$-	TEST77	TEST77	read-write, 16 bits	Test register. Write with zero after SIO reset.
$04e_{16}$-	TEST78	TEST78	read-write, 16 bits	Test register. Do not read or write after SIO reset.
$04f_{16}$-	TEST79	TEST79	read-write, 16 bits	Test register. Do not read or write after SIO reset.
080_{16}-Off_{16}	reserved	reserved	vendor-specific	Vendor-specific test registers. Do not read or write after SIO reset.

Figure 22-1 Control Registers (1/7)

Control Register : INIT

Address : 021_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDM	SDE VID5	DIS	TSQ	TEN	LSR	PSR	NSR	SRP	PSX	0	SDEVID4..0				

Read/write register.

Reset values are undefined except as affected by SIO Reset as noted below. SETR/CLRR Reset does not affect this register.

Field	Description	Reset value
SDEVID5..0	Serial Device Identification. Compared to SDEVID5..0 serial address field of serial request packet for register read/write transactions. This determines which RDRAM is selected for the register read or write operation.	$3f_{16}$
DIS	RDRAM disable. DIS=1 causes RDRAM to ignore NAP/PDN exit sequence, DIS=0 permit normal operation. This mechanism disables an RDRAM.	0
TSQ	Temperature Sensing Output. TSQ=1 when a temperature trip point has been exceeded, TSQ=0 when it has not. TSQ is available during a current control operation (see Figure 25-1).	
TEN	Temperature Sensing Enable. TEN=1 enables temperature sensing circuitry, permitting the TSQ bit to be read to determine if a thermal trip point has been exceeded.	0
LSR	Low Power Self-Refresh. This function is not supported. LSR value must be 0.	0
PSR	PDN Self-Refresh. PSR=1 enables self-refresh in PDN mode. PSR can't be set while in PDN mode.	0
NSR	NAP Self-Refresh. NSR=1 enables self-refresh in NAP mode. NSR can't be set while in NAP mode.	0
SRP	SIO Repeater. Controls value on SIO1; SIO1=SIO0 if SRP=1, SIO1=1 if SRP=0.	1
PSX	Power Exit Select. PDN and NAP are exited with (=0) or without (=1) a device address on the DQA5..0 pins. PDEV5 (on DQA5) selectes broadcast (1) or directed (0) exit. For a dircted exit, PDEV4..0 (on DQA4..0) is compared to DEVID4..0 to select a device.	

Control Register : CNFGA

Address : 023_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PVER5..0=000001						MVER5..0=mmmmmm						DBL1	REFBIT2..0=101		

Read only register.

Field	Description
PVER5..0	Protocol Version. Specifies the Direct Protocol version used by this device: 0 – Reserved 1 – Version 1 protocol. 2 – Version 1 plus Interleaved Device Mode. 3 to 63 – Reserved
MVER5..0	Manufacturer Version. Specifies the manufacturer identification number.
DBL	Doubled-Bank. DBL=1 means the device uses a doubled-bank architecture with adjacent-bank dependency. DBL=0 means no dependency.
REFBIT2..0	Refresh Bank Bits. Specifies the number of bank address bits used by REFA and REFP commands. Permits multi-bank refresh in future RDRAMs.

Caution In RDRAMs with protocol version 1 PVER[5:0] =000001, the range of the PDNX field (PDNX[2:0] in the PDNX register) may not be large enough to specify the location of the restricted interval in Figure 23-3. In this case, the effective t_{S4} parameter must increase and no row or column packets may overlap the restricted interval. See Figure 23-3 and Timing conditions table.

Figure 22-1 Control Registers (2/7)

Control Register : CNFGB

Address : 024_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SVER5..0=ssssss						CORG4..0=01000					SPT0	DEVTYP2..0=000			BYTB

Read only register.

Field	Description
SVER5..0	Stepping version. Specifies the mask version number of this device.
CORG4..0	Core organization. This field specifies the number of bank (5 bits), row (9 bits), and column (7 bits) address bits.
SPT	Split-core. SPT=1 means the core is split, SPT=0 means it is not.
DEVTYP2..0	Device type. DEVTYP=000 means that this device is an RDRAM.
BYT	Byte width. B=1 means the device reads and writes 9-bit memory bytes.B=0 means 8 bits.

Control Register : TEST34

Address : 022_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Read/write register.

Reset values of TEST34 is zero (from SIO Reset).

This register are used for testing purposes. It must not be read or written after SIO Reset.

Control Register : DEVID

Address : 040_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	DEVID4..0				

Read/write register.

Reset value is undefined.

Field	Description
DEVID4..0	Device Identification register. DEVID4..DEVID0 is compared to DR4..DR0, DC4..DC0, and DX4..DX0 fields for all memory read or write transactions. This determines which RDRAM is selected for the memory read or write transaction.

Figure 22-1 Control Registers (3/7)

Control Register : REFB **Address : 041_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	REFB4..0				

Read/write register.

Field	Description	Reset value
REFB4..0	Refresh Bank Register. REFB4..REFB0 is the bank that will be refreshed next during self-refresh. REFB4..0 is incremented after each self-refresh activate and precharge operation pair.	0

Control Register : REFR **Address : 042_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	REFR8..0								

Read/write register.

Field	Description	Reset value
REFR8..0	Refresh Row register. REFR8..REFR0 is the row that will be refreshed next by the REFA command or by self-refresh. REFR8..0 is incremented when BR4..0=11111 for the REFA command. REFR8..0 is incremented when REFB4..0=11111 for self-refresh.	0

Control Register : CCA **Address : 043_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	ASYM A0	CCA6..0						

Read/write register.

Field	Description	Reset value
ASYMA0	ASYMA0 control the asymmetry of the V_{OL}/V_{OH} voltage swing about the V_{REF} reference voltage for the DQA8..0 pins. ASYMA0 ODF 0 0.00 1 0.12 Where ODF is the Over Drive Factor (the extra I_{OL} current sunk by an RSL output when ASYMA0 is set).	0
CCA6..0	Current Control A. Controls the I_{OL} output current for the DQA8..DQA0 pins.	

Control Register : CCB **Address : 044_{16}**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	ASYM B0	CCB6..0						

Read/write register.

Field	Description	Reset value
ASYMB0	ASYMB0 control the asymmetry of the V_{OL}/V_{OH} voltage swing about the V_{REF} reference voltage for the DQB8..0 pins. ASYMB0 ODF 0 0.00 1 0.12 Where ODF is the Over Drive Factor (the extra I_{OL} current sunk by an RSL output when ASYMB0 is set).	0
CCB6..0	Current Control B. Controls the I_{OL} output current for the DQB8..DQB0 pins.	

Figure 22-1 Control Registers (4/7)

Control Register : NAPX

Address : 045_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	DQS	NAPX4..0					NAPXA4..0				

Read/write register.
Reset value is undefined.
Note t_{SCYCLE} is t_{CYCLE1} (SCK cycle time).

Field	Description
DQS	DQ Select. This field specifies the number of SCK cycles (0 ≥ 0.5 cycles, 1 ≥ 1.5 cycles) between the CMD pin framing sequence and the device selection on DQ5..0. see Figure 23-4. This field must be written with a ”1” for this RDRAM.
NAPX4..0	Nap Exit Phase A plus B. This field specifies the number of SCK cycles during the first plus second phases for exiting NAP mode. It must satisfy: $NAPX \bullet t_{SCYCLE} \geq NAPXA \bullet t_{SCYCLE} + t_{NAPXB,MAX}$ Do not set this field to zero.
NAPXA4..0	Nap Exit Phase A. This field specifies the number of SCK cycles during the first phase for exiting NAP mode. It must satisfy: $NAPXA \bullet t_{SCYCLE} \geq t_{NAPXA,MAX}$ Do not set this field to zero.

Control Register : PDNXA

Address : 046_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	PDNXA12..0												

Read/write register.
Reset value is undefined.

Field	Description
PDNXA4..0	PDN Exit Phase A. This field specifies the number of (64•SCK cycle) units during the first phase for exiting PDN mode. It must satisfy: $PDNXA \bullet 64 \bullet t_{SCYCLE} \geq t_{PDNXA,MAX}$ Do not set this field to zero. Note – only PDNXA4..0 are implemented. Note – t_{SCYCLE} is t_{CYCLE1} (SCK cycle time).

Control Register : PDNX

Address : 047_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	PDNX12..0												

Read/write register.
Reset value is undefined.

Field	Description
PDNX2..0	PDN Exit Phase A puls B. This field specifies the number of (256•SCK cycle) units during the first plus second phases for exiting PDN mode. It should satisfy: $PDNX \bullet 256 \bullet t_{SCYCLE} \geq PDNXA \bullet 64 \bullet t_{SCYCLE} + t_{PDNXB,MAX}$ It this equation can’t be satisfied, then the maximum PDNX value should be written, and the t_{S4} / t_{H4} timing window will be modified (see Figure 23-4). Do not set this field to zero. Note – only PDNX2..0 are implemented. Note – t_{SCYCLE} is t_{CYCLE1} (SCK cycle time).

Figure 22-1 Control Registers (5/7)

Control Register : TPARM

Address : 048_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	TCDLY0			TCLS		TCAL	

Read/write register.

Reset value is undefined.

Field	Description
TCDLY0	Specifies the $t_{CDLY0\text{-}C}$ core parameter in t_{CYCLE} units. This adds a programmable delay to Q (read data) packets, permitting round trip read delay to all device to be equalized. This field may be written with the values “010” ($2\bullet t_{CYCLE}$) through “101” ($5\bullet t_{CYCLE}$).
TCLS1..0	Specifies the $t_{CLS\text{-}C}$ core parameter in t_{CYCLE} units. Should be “10” ($2\bullet t_{CYCLE}$).
TCAS1..0	Specifies the $t_{CAS\text{-}C}$ core parameter in t_{CYCLE} units. This should be “10” ($2\bullet t_{CYCLE}$).

The equations relating the core parameters to the datasheet parameters follow:

$t_{CAS\text{-}C}=2\bullet t_{CYCLE}$

$t_{CLS\text{-}C}=2\bullet t_{CYCLE}$

$t_{CPS\text{-}C}=1\bullet t_{CYCLE}$ Not programmable

$t_{OFFP}=t_{CPS\text{-}C}+t_{CAS\text{-}C}+t_{CLS\text{-}C}-1\bullet t_{CYCLE}$

$=4\bullet t_{CYCLE}$

$t_{RCD}=t_{RCD\text{-}C}+1\bullet t_{CYCLE}-t_{CLS\text{-}C}$

$=t_{RCD\text{-}C}-1\bullet t_{CYCLE}$

$t_{CAC}=3\bullet t_{CYCLE}+t_{CLS\text{-}C}+t_{CDLY0\text{-}C}+t_{CDLY1\text{-}C}$ (see table below programming ranges)

TCDLY0	$t_{CDLY0\text{-}C}$	TCDLY1	$t_{CDLY1\text{-}C}$	t_{CAC}@t_{CYCLE}=3.30 ns	t_{CAC}@t_{CYCLE}=2.50 ns
010	$2\bullet t_{CYCLE}$	000	$0\bullet t_{CYCLE}$	$7\bullet t_{CYCLE}$	not allowed
011	$3\bullet t_{CYCLE}$	000	$0\bullet t_{CYCLE}$	$8\bullet t_{CYCLE}$	$8\bullet t_{CYCLE}$
011	$3\bullet t_{CYCLE}$	001	$1\bullet t_{CYCLE}$	$9\bullet t_{CYCLE}$	$9\bullet t_{CYCLE}$
011	$3\bullet t_{CYCLE}$	010	$2\bullet t_{CYCLE}$	$10\bullet t_{CYCLE}$	$10\bullet t_{CYCLE}$
100	$4\bullet t_{CYCLE}$	010	$2\bullet t_{CYCLE}$	$11\bullet t_{CYCLE}$	$11\bullet t_{CYCLE}$
101	$5\bullet t_{CYCLE}$	010	$2\bullet t_{CYCLE}$	$12\bullet t_{CYCLE}$	$12\bullet t_{CYCLE}$

Control Register : TFRM

Address : 049_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TFRM3..0			

Read/write register.

Reset value is undefined.

Field	Description
TFRM3..0	Specifies the position of the framing point in t_{CYCLE} units. This value must be greater than or equal to the $t_{FRM,MIN}$ parameter. This is the minimum offset between a ROW packet (which places a device at ATTN) and the first COL packet (directed to that device) which must be framed. This field may be written with the value “0111” ($7\bullet t_{CYCLE}$) through “1010” ($10\bullet t_{CYCLE}$). TFRM is usually set to the value which matches the largest $t_{RCD,MIN}$ parameter (modulo $4\bullet t_{CYCLE}$) that is present in an RDRAM in the memory system. Thus, if an RDRAM with $t_{RCD,MIN}=11\bullet t_{CYCLE}$ were present, then TFRM would be programmed to $7\bullet t_{CYCLE}$.

Figure 22-1 Control Registers (6/7)

Control Register : TCDLY1 **Address : $04a_{16}$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	TCDLY1		

Read/write register.
Reset value is undefined.

Field	Description
TCDLY1	Specifies the value of the $t_{CDLY1-C}$ core parameter in t_{CYCLE} units. This adds a programmable delay to Q (read data) packets, permitting round trip read to delay all devices to be equalized. This field may be written with the values “000” (0•t_{CYCLE}) through “010” (2•t_{CYCLE}). Refer to TPARM Register for more details.

Control Register : SKIP **Address : $04b_{16}$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	AS	MSE	MS	0	0	0	0	0	0	0	0	0	0

Read/write register (except AS field).
Reset value is zero (SIO Reset).

Field	Description
MS	Manual skip (MS must be 1 when MSE=1). > During initialization, the RDRAMs at the furthest point in the fifth read domain may have selected the AS=0 value, placing them at the closest point in a sixth read domain. Setting the MSE/MS fields to 1/1 overrides the autoskip value and returns them to the furthest point of the fifth read domain.
MSE	Manual skip enable (0=auto, 1=manual).
AS	Autoskip. Read-only value determined by autoskip circuit and stored when SETF serial command is received by RDRAM during initialization. In Figure34-1, AS=1 corresponds to the early Q(a1) packet and AS=0 to the Q(a1) packet one t_{CYCLE} later for the four uncertain cases.

Control Register : TCYCLE **Address : $04c_{16}$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	TCYCLE13..0													

Read/write register.
Reset value is undefined.

Field	Description
TCYCLE13..0	Specifies the value of the t_{CYCLE} datasheet parameter in 64ps units. For the $t_{CYCLE,MIN}$ of 2.50 ns (2500ps), this field should be written with the value “00027_{16}” (39•64ps).

Figure 22-1 Control Registers (7/7)

Control Register : TEST77	**Address : $04d_{16}$**
Control Register : TEST78	**Address : $04e_{16}$**
Control Register : TEST79	**Address : $04f_{16}$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Read/write register.

Field	Description	Reset value
TEST77	It must be written with zero after SIO reset. These registers must only be used for testing purposes.	—
TEST78	Do not read or written after SIO reset.	0
TEST79	Do not read or written after SIO reset.	0

23. Power State Management

Table 23-1 summarizes the power states available to a Direct RDRAM. In general, the lowest power states have the longest operational latencies. For example, the relative power levels of PDN state and STBY state have a ratio of about 1:110, and the relative access latencies to get read data have a ratio of about 250:1.

PDN state is the lowest power state available. The information in the RDRAM core is usually maintained with self-refresh; an internal timer automatically refreshes all rows of all banks. PDN has a relatively long exit latency because the TCLK/RCLK block must resynchronize itself to the external clock signal.

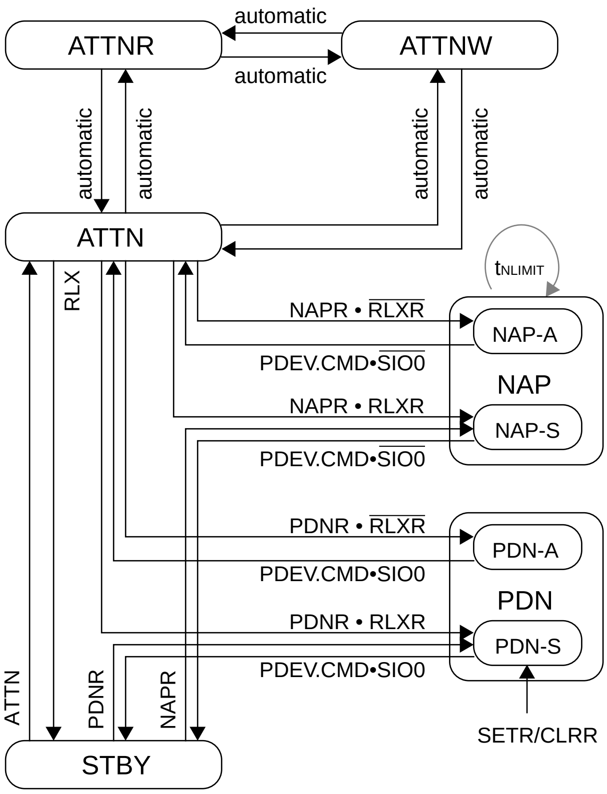
NAP state is another low-power state in which either self-refresh or REFA-refresh are used to maintain the core. See **24. Refresh** for a description of the two refresh mechanisms. NAP has a shorter exit latency than PDN because the TCLK/RCLK block maintains its synchronization state relative to the external clock signal at the time of NAP entry. This imposes a limit (t_{NLIMIT}) on how long an RDRAM may remain in NAP state before briefly returning to STBY or ATTN to update this synchronization state.

Table 23-1 Power State Summary

Power State	Description	Blocks consuming power	Power state	Description	Blocks consuming power
PDN	Powerdown state.	Self-refresh	NAP	Nap state. Similar to PDN except lower wake-up latency.	Self-refresh or REFA-refresh TCLK/RCLK-Nap
STBY	Standby state. Ready for ROW packets.	REFA-refresh TCLK/RCLK ROW demux receiver	ATTN	Attention state. Ready for ROW and COL packets.	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver
ATTNR	Attention read state. Ready for ROW and COL packets. Sending Q (read data) packets.	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver DQ mux transmitter Core power	ATTNW	Attention write state. Ready for ROW and COL packets. Ready for D (write data) packets.	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver DQ demux receiver Core power

Figure 23-1 summarizes the transition conditions needed for moving between the various power states. Note that NAP and PDN have been divided into two substates (NAP-A/NAP-S and PDN-A/PDN-S) to account for the fact that a NAP or PDN exit may be made to either ATTN or STBY states.

Figure 23-1 Power State Transition Diagram



Notation:
SETR/CLRR - SETR/CLRR Reset sequence in SRQ packet
PDNR - PDNR command in ROWR packet
NAPR - NAPR command in ROWR packet
RLXR - RLX command in ROWR packet
RLX - RLX command in ROWR,COLC,COLX packets
SIO0 - SIO0 input value
PDEV.CMD - (PDEV=DEVID)•(CMD=01)
ATTN - ROWA packet(non-broadcast) or ROWR packet
(non-broadcast) with ATTN command

At initialization, the SETR/CLRR Reset sequence will put the RDRAM into PDN-S state. The PDN exit sequence involves an optional PDEV specification and bits on the CMD and SIO_{IN} pins.

Once the RDRAM is in STBY, it will move to the ATTN/ATTNR/ATTNW states when it receives a non-broadcast ROWA packet or non-broadcast ROWR packet with the ATTN command. The RDRAM returns to STBY from these three states when it receives a RLX command. Alternatively, it may enter NAP or PDN state from ATTN or STBY states with a NAPR or PDNR command in an ROWR packet. The PDN or NAP exit sequence involves an optional PDEV specification and bits on the CMD and SIO0 pins. The RDRAM returns to the ATTN or STBY state it was originally in when it first entered NAP or PDN.

An RDRAM may only remain in NAP state for a time t_{NLIMIT}. It must periodically return to ATTN or STBY.

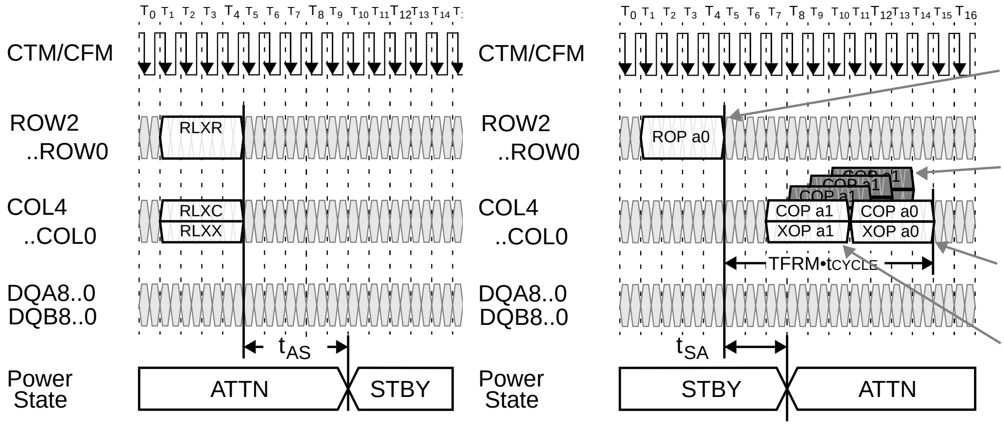
The NAPRC command causes a napdown operation if the RDRAM's NCBIT is set. The NCBIT is not directly visible. It is undefined on reset. It is set by a NAPR command to the RDRAM, and it is cleared by an ACT command to the RDRAM. It permits a controller to manage a set of RDRAMs in a mixture of power states.

STBY state is the normal idle state of the RDRAM. In this state all banks and sense amps have usually been left precharged and ROWA and ROWR packets on the ROW pins are being monitored. When a non-broadcast ROWA packet or non-broadcast ROWR packet(with the ATTN command) packet addressed to the RDRAM is seen, the RDRAM enters ATTN state (see the right side of Figure 23-2). This requires a time t_{SA} during which the RDRAM activates the specified row of the specified bank. A time TFRM•t_{CYCLE} after the ROW packet, the RDRAM will be able to frame COL packets (TFRM is a control register field – see Figure 22-1(5/7) "**TFRM Register**"). Once in ATTN state, the RDRAM will automatically transition to the ATTNW and ATTNR states as it receives WR and RD commands.

Once the RDRAM is in ATTN, ATTNW, or ATTNR states, it will remain there until it is explicitly returned to the STBY state with a RLX command. A RLX command may be given in an ROWR, COLC, or COLX packet (see the left side of Figure 23-2). It is usually given after all banks of the RDRAM have been precharged; if other banks are still activated, then the RLX command would probably not be given.

If a broadcast ROWA packet or ROWR packet (with the ATTN command) is received, the RDRAM's power state doesn't change. If a broadcast ROWR packet with RLXR command is received, the RDRAM goes to STBY.

Figure 23-2 STBY Entry (left) and STBY Exit (right)



ROP=non-broadcast ROWA or ROWR/ATTN

a0={d0, b0, r0}
a1={d1, b1, c1}

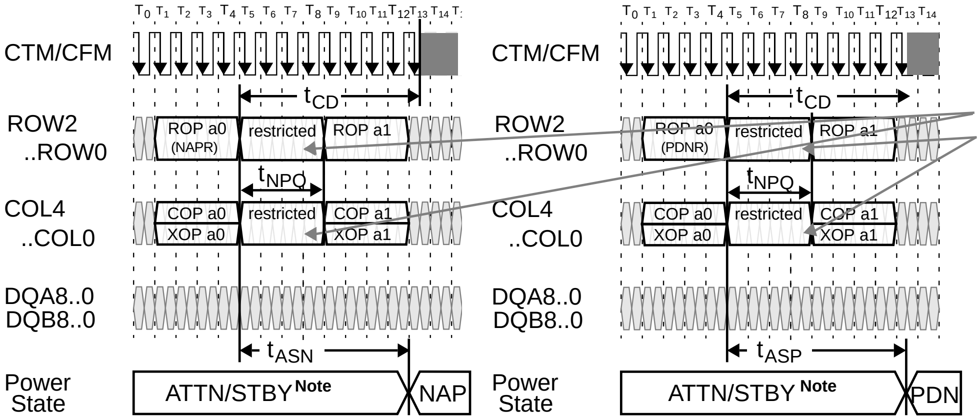
No COL packets may be placed in the three indicated positions; i.e. at (TFRM-{1,2,3})•t_{CYCLE}.

A COL packet to device d0 (or any other device) is okay at (TFRM)•t_{CYCLE} or later.

A COL packet to another device (d1!=d0) is okay at (TFRM-4)•t_{CYCLE} or earlier.

Figure 23-3 shows the NAP entry sequence (left). NAP state is entered by sending a NAPR command in a ROW packet. A time t_{ASN} is required to enter NAP state (this specification is provided for power calculation purposes). The clock on CTM/CFM must remain stable for a time t_{CD} after the NAPR command.

Figure 23-3 NAP Entry (left) and PDN Entry (right)



a0={d0, b0, r0, c0}
a1={d1, b1, c1, c1}

No ROW or COL packets directed to device d0 may overlap the restricted interval. No broadcast ROW packets may overlap the quiet interval.

ROW or COL packets to a device other than d0 may overlap the restricted interval.

ROW or COL packets directed to device d0 after the restricted interval will be ignored.

Note The(eventual) NAP/PDN exit will be to the same ATTN/STBY state the RDRAM was in prior to NAP/PDN entry

The RDRAM may be in ATTN or STBY state when the NAPR command is issued. When NAP state is exited, the RDRAM will return to the original starting state (ATTN or STBY). If it is in ATTN state and a RLXR command is specified with NAPR, then the RDRAM will return to STBY state when NAP is exited.

Figure 23-3 also shows the PDN entry sequence (right). PDN state is entered by sending a PDNR command in a ROW packet. A time t_{ASP} is required to enter PDN state (this specification is provided for power calculation purposes). The clock on CTM/CFM must remain stable for a time t_{CD} after the PDNR command.

The RDRAM may be in ATTN or STBY state when the PDNR command is issued. When PDN state is exited, the RDRAM will return to the original starting state (ATTN or STBY). If it is in ATTN state and a RLXR command is specified with PDNR, then the RDRAM will return to STBY state when PDN is exited. The current- and slew-rate-control levels are re-established.

The RDRAM's write buffer must be retired with the appropriate COP command before NAP or PDN are entered. Also, all the RDRAM's banks must be precharged before NAP or PDN are entered. The exception to this is if NAP is entered with the NSR bit of the INIT register cleared(disabling self-refresh in NAP). The commands for relaxing, retiring, and precharging may be given to the RDRAM as late as the ROPa0, COPa0, and XOPa0 packets in Figure 23-3. No broadcast packets nor packets directed to the RDRAM entering NAP or PDN may overlay the quiet window. This window extends for a time t_{NPQ} after the packet with the NAPR or PDNR command.

Figure 23-4 shows the NAP and PDN exit sequences. These sequences are virtually identical; the minor differences will be highlighted in the following description.

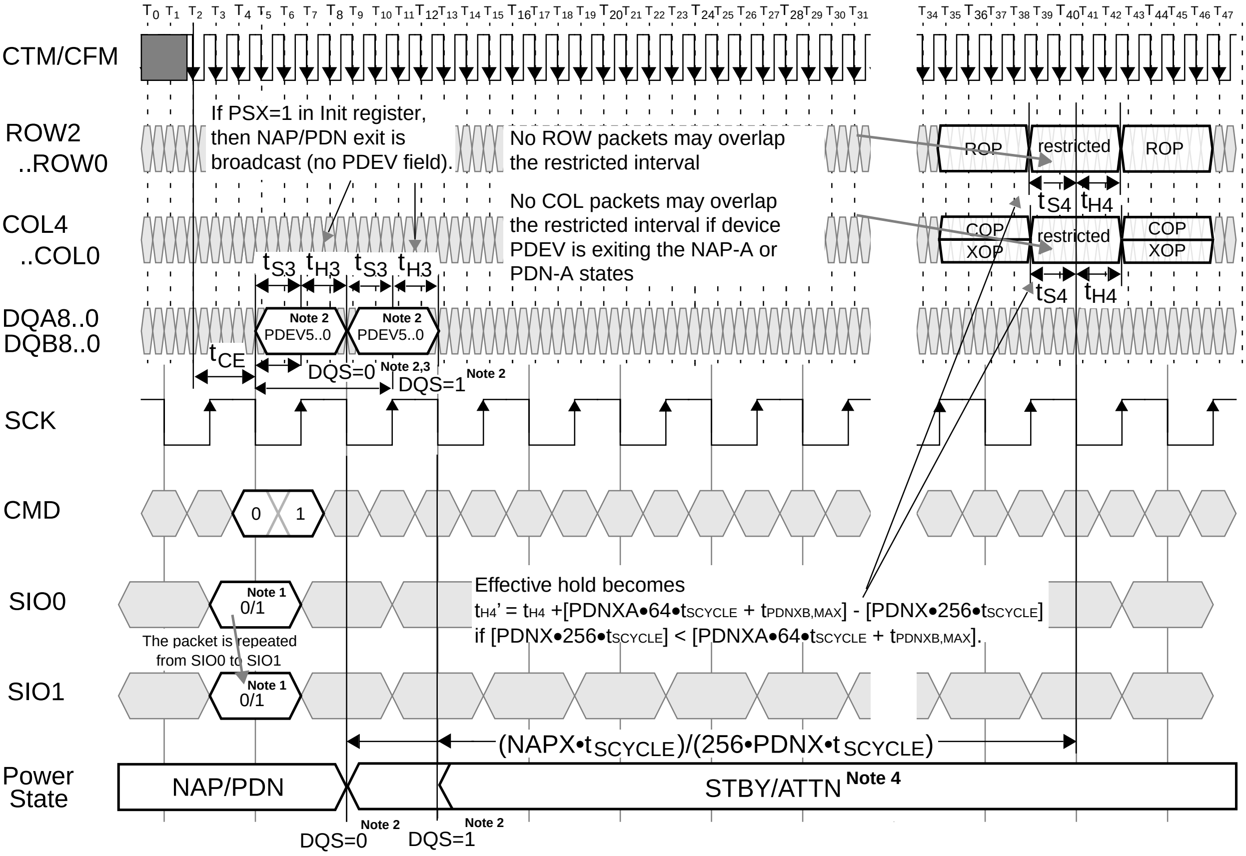
Before NAP or PDN exit, the CTM/CFM clock must be stable for a time t_{CE}. Then, on a falling and rising edge of SCK, if there is a “01” on the CMD input, NAP or PDN state will be exited. Also, on the falling SCK edge the SIO0 input must be at a 0 for NAP exit and 1 for PDN exit.

If the PSX bit of the INIT register is 0, then a device PDEV5..0 is specified for NAP or PDN exit on the DQA5..0 pins. This value is driven on the rising SCK edge 0.5 or 1.5 SCK cycles after the original falling edge, depending upon the value of the DQS bit of the NAPX register. If the PSX bit of the INIT register is 1, then the RDRAM ignores the PDEV5..0 address packet and exits NAP or PDN when the wake-up sequence is presented on the CMD wire. The ROW and COL pins must be quiet at a time t_{S4} / t_{H4} around the indicated falling SCK edge(timed with the PDNX or NAPX register fields). After that, ROW and COL packets may be directed to the RDRAM which is now in ATTN or STBY state.

Figure 23-5 shows the constraints for entering and exiting NAP and PDN states. On the left side, an RDRAM exits NAP state at the end of cycle T_3. This RDRAM may not re-enter NAP or PDN state for an interval of t_{NU0}. The RDRAM enters NAP state at the end of cycle T_{13}. This RDRAM may not re-exit NAP state for an interval of t_{NU1}. The equations for these two parameters depend upon a number of factors, and are shown at the bottom of the figure. NAPX is the value in the NAPX field in the NAPX register.

On the right side of Figure23-4, an RDRAM exits PDN state at the end of cycle T_3. This RDRAM may not re-enter PDN or NAP state for an interval of t_{PU0}. The RDRAM enters PDN state at the end of cycle T_{13}. This RDRAM may not re-exit PDN state for an interval of t_{PU1}. The equations for these two parameters depend upon a number of factors, and are shown at the bottom of the figure. PDNX is the value in the PDNX field in the PDNX register.

Figure 23-4 NAP and PDN Exit



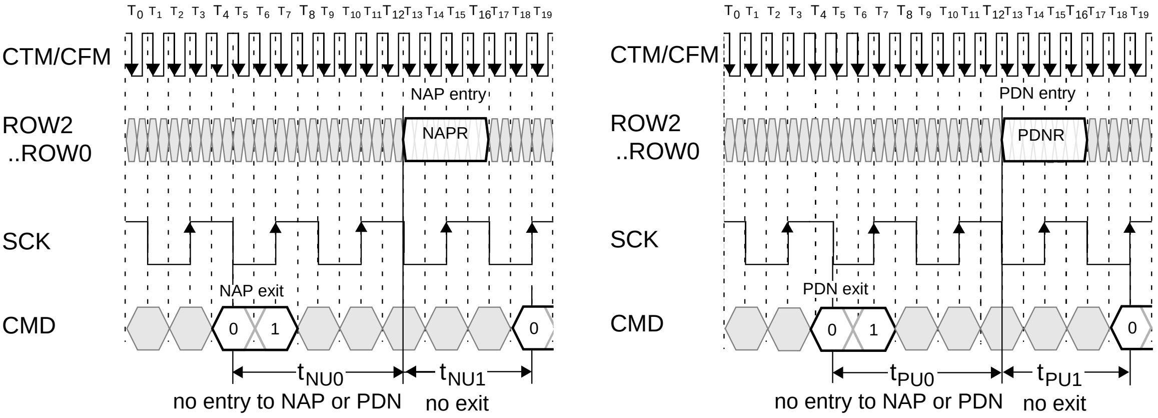
Notes 1. Use 0 for NAP exit, 1 for PDN exit

2. Device selection timing slot is selected by DQS field of NAPX register

3. The DQS field must be written with “1” for this RDRAM.

4. Exit to STBY or ATTN depends upon whether RLXR was asserted at NAP or PDN entry time

Figure 23-5 NAP Entry/Exit Windows (left) and PDN Entry/Exit Windows (right)



t_{NU0} =5•t_{CYCLE} +(2+NAPX)•t_{SCYCLE}
t_{NU1} =8•t_{CYCLE} - (0.5•t_{SCYCLE}) if NSR=0
=23•t_{CYCLE} if NSR=1

t_{PU0} =5•t_{CYCLE} +(2+256•PDNX)•t_{SCYCLE}
t_{PU1} =8•t_{CYCLE} - (0.5•t_{SCYCLE}) if PSR=0
=23•t_{CYCLE} if PSR=1

24. Refresh

RDRAMs, like any other DRAM technology, use volatile storage cells which must be periodically refreshed. This is accomplished with the REFA command. Figure 24-1 shows an example of this.

The REFA command in the transaction is typically a broadcast command (DR4T and DR4F are both set in the ROWR packet), so that in all devices bank number Ba is activated with row number REFR, where REFR is a control register in the RDRAM. When the command is broadcast and ATTN is set, the power state of the RDRAMs (ATTN or STBY) will remain unchanged. The controller increments the bank address Ba for the next REFA command. When Ba is equal to its maximum value, the RDRAM automatically increments REFR for the next REFA command.

On average, these REFA commands are sent once every $t_{REF} / 2^{BBIT+RBIT}$ (where BBIT are the number of bank address bits and RBIT are the number of row address bits) so that each row of each bank is refreshed once every t_{REF} interval.

The REFA command is equivalent to an ACT command, in terms of the way that it interacts with other packets (see Table 6-1). In the example, an ACT command is sent after t_{RR} to address b0, a different (non-adjacent) bank than the REFA command.

A second ACT command can be sent after a time t_{RC} to address c0, the same bank (or an adjacent bank) as the REFA command.

Note that a broadcast REFP command is issued a time t_{RAS} after the initial REFA command in order to precharge the refreshed bank in all RDRAMs. After a bank is given a REFA command, no other core operations(activate or precharge) should be issued to it until it receives a REFP.

It is also possible to interleave refresh transactions (not shown). In the figure, the ACT b0 command would be replaced by a REFA b0 command. The b0 address would be broadcast to all devices, and would be {Broadcast, Ba+2,REFR}. Note that the bank address should skip by two to avoid adjacent bank interference. A possible bank incrementing pattern would be: {12, 10, 5, 3, 0, 14, 9, 7, 4, 2, 13, 11, 8, 6, 1, 15, 28, 26, 21, 19, 16, 30, 25, 23, 20, 18, 29, 27, 24, 22, 17, 31}. Every time bank 31 is reached, a REFA command would automatically increment the REFR register.

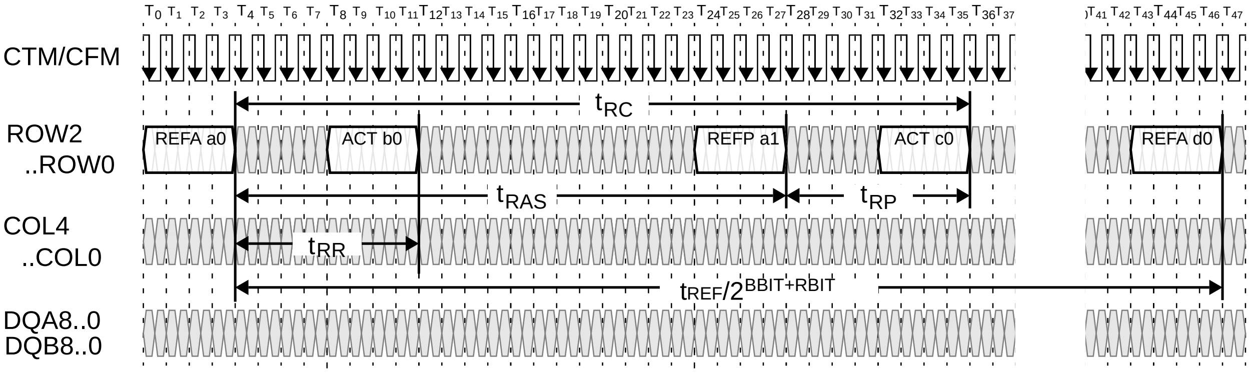
A second refresh mechanism is available for use in PDN and NAP power states. This mechanism is called self-refresh mode. When the PDN power state is entered, or when NAP power state is entered with the NSR control register bit set, then self-refresh is automatically started for the RDRAM.

Self-refresh uses an internal time base reference in the RDRAM. This causes an activate and precharge to be carried out once in every $t_{REF} / 2^{BBIT+RBIT}$ interval. The REFB and REFR control registers are used to keep track of the bank and row being refreshed.

Before a controller places an RDRAM into self-refresh mode, it should perform REFA/REFP refreshes until the bank address is equal to the maximum value. This ensures that no rows are skipped. Likewise, when a controller returns an RDRAM to REFA/REFP refresh, it should start with the minimum bank address value (zero).

Figure 24-2 illustrates the requirement imposed by the t_{BURST} parameter. After PDN or NAP (when self-refresh is enabled) power states are exited, the controller must refresh all banks of the RDRAM once during the interval t_{BURST} after the restricted interval on the ROW and COL buses. This will ensure that regardless of the state of self-refresh during PDN or NAP, the $t_{REF, MAX}$ parameter is met for all banks. During the t_{BURST} interval, the banks may be refreshed in a single burst, or they may be scattered throughout the interval. Note that the first and last banks to be refreshed in the t_{BURST} interval are numbers 12 and 31, in order to match the example refresh sequence.

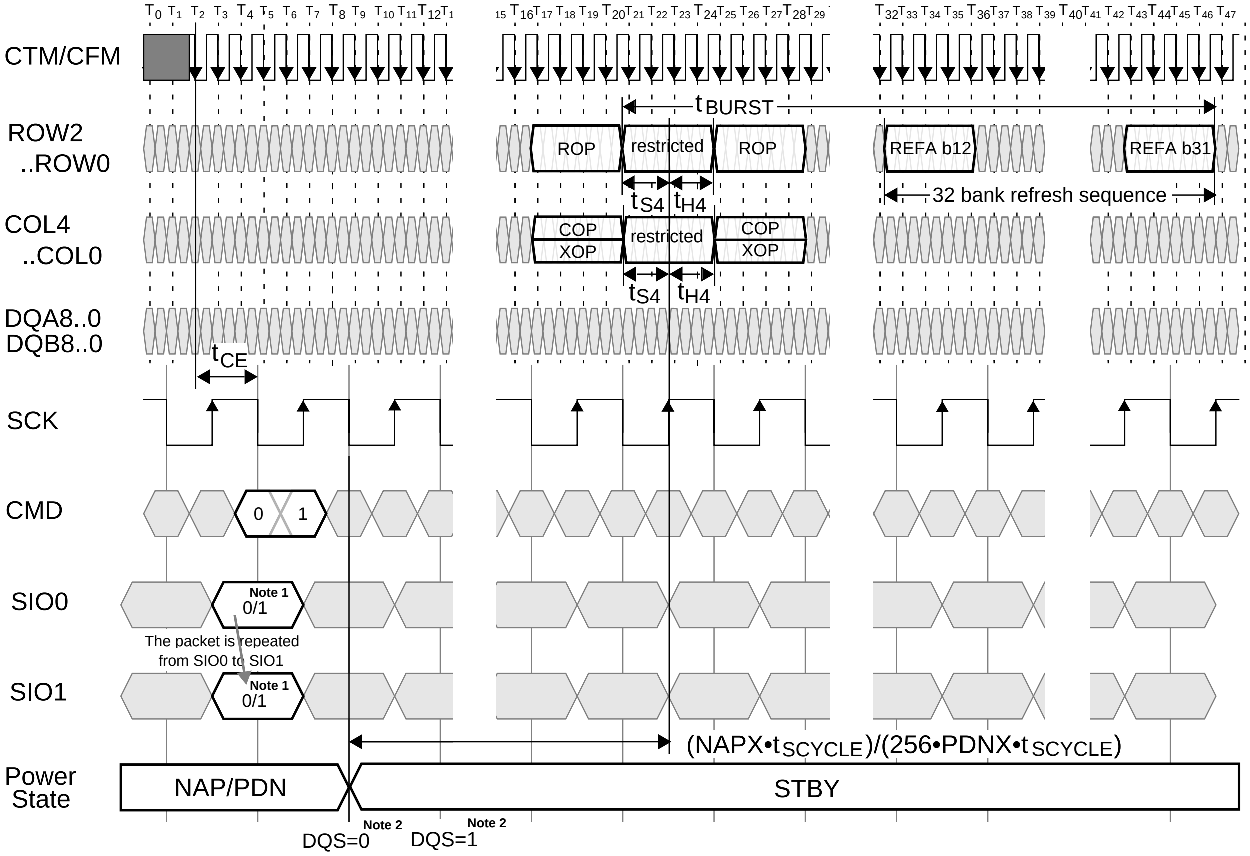
Figure 24-1 REFA/REFP Refresh Transaction Example



Transaction a: REFA	a0 = {Broadcast,Ba,REFR}	a1 = {Broadcast,Ba}
Transaction b: xx	b0 = {Db, /={Ba,Ba+1,Ba-1}, Rb}	
Transaction c: xx	c0 = {Dc, ==Ba, Rc}	
Transaction d: REFA	d0 = {Broadcast,Ba+1,REFR}	

BBIT = #bank address bits
RBIT = #row address bits
REFB = REFB3..REFB0
REFR = REFR8..REFR0

Figure 24-2 NAP/PDN Exit - tBURST Requirement



Notes 1. Use 0 for NAP exit, 1 for PDN exit

2. Device selection timing slot is selected by DQS field of NAPX register

25. Current and Temperature Control

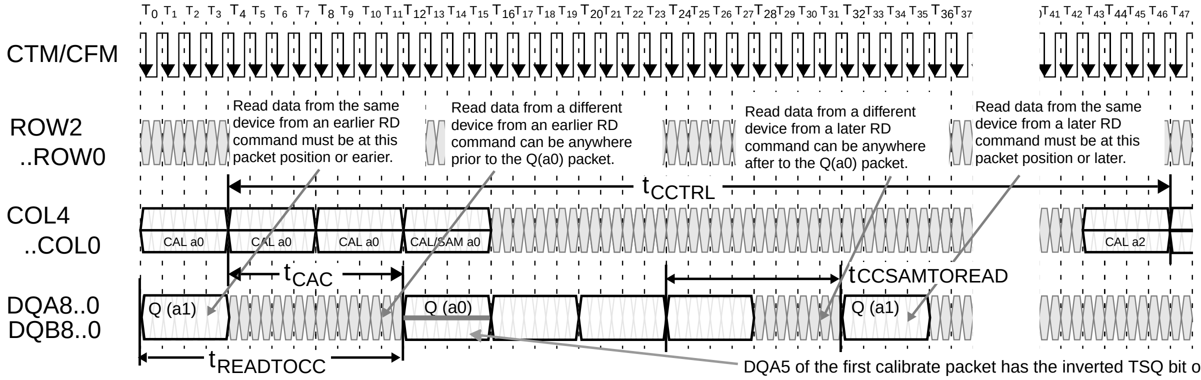
Figure 25-1 shows an example of a transaction which performs current control calibration. It is necessary to perform this operation once to every RDRAM in every t_{CCTRL} interval in order to keep the I_{OL} output current in its proper range.

This example uses four COLX packets with a CAL command. These cause the RDRAM to drive four calibration packets Q(a0) a time t_{CAC} later. An offset of t_{RDTOCC} must be placed between the Q(a0) packet and read data Q(a1) from the same device. These calibration packets are driven on the DQA4..3 and DQB4..3 wires. The TSQ bit of the INIT register is driven on the DQA5 wire during same interval as the calibration packets. The remaining DQA and DQB wires are not used during these calibration packets. The last COLX packet also contains a SAM command (concatenated with the CAL command). The RDRAM samples the last calibration packet and adjusts its I_{OL} current value.

Unlike REF commands, CAL and SAM commands cannot be broadcast. This is because the calibration packets from different devices would interfere. Therefore, a current control transaction must be sent every t_{CCTRL} /N, where N is the number of RDRAMs on the Channel. The device field Da of the address a0 in the CAL/SAM command should be incremented after each transaction.

Figure 25-2 shows an example of a temperature calibration sequence to the RDRAM. This sequence is broadcast once every t_{TEMP} interval to all the RDRAMs on the Channel. The TCEN and TCAL are ROP commands, and cause the slew rate of the output drivers to adjust for temperature drift. During the quiet interval $t_{TCQUIET}$ the devices being calibrated can't be read, but they can be written.

Figure 25-1 Current Control CAL/SAM Transaction Example

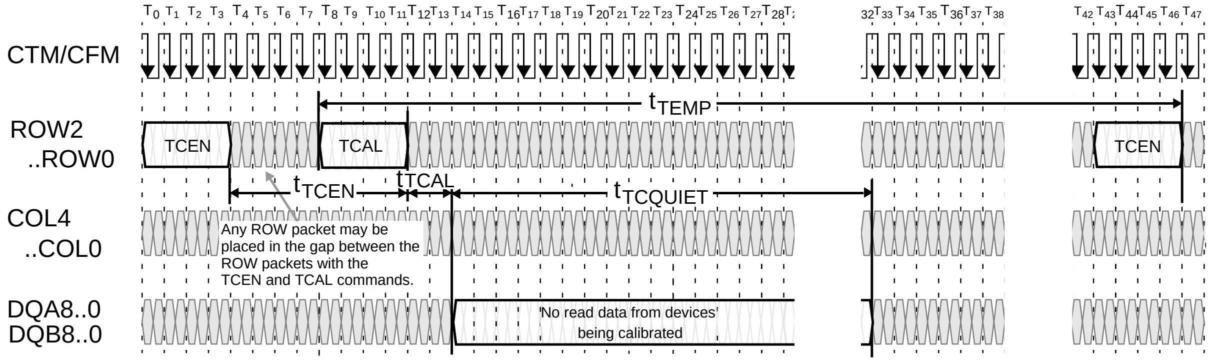


Transaction a0: CAL/SAM	a0 = {Da, Bx}
Transaction a1: RD	a1 = {Da, Bx}
Transaction a2: CAL/SAM	a2 = {Da, Bx}

DQA5 of the first calibrate packet has the inverted TSQ bit of INIT control register; i.e. logic 0 or high voltage means hot temperature. When used for monitoring, it should be enabled with the DQA3 bit (current control one value) in case there is no RDRAM present: HotTemp = /DQA5•DQA3

Note that DQB3 could be used instead of DQA3.

Figure 25-2 Temperature Calibration (TCEN-TCAL) Transactions to RDRAM



26. Electrical Conditions

Electrical Conditions

Symbol	Parameter and Conditions	MIN.	MAX.	Unit
Tj	Junction temperature under bias	—	100	°C
V_{DD}, V_{DDa}	Supply voltage	2.50 – 0.13	2.50 + 0.13	V
$V_{DD,N}$, $V_{DDa,N}$	Supply voltage droop (DC) during NAP interval (t_{NLIMT})	—	2.0	%
$V_{DD,N}$, $V_{DDa,N}$	Supply voltage ripple (AC) during NAP interval (t_{NLIMT})	–2.0	+2.0	%
V_{CMOS}	Supply voltage for CMOS pins (2.5V controllers)	2.50 – 0.13	2.50 + 0.25	V
	Supply voltage for CMOS pins (1.8V controllers)	1.80 – 0.1	1.80 + 0.2	V
V_{TERM}	Termination voltage	1.80 – 0.1	1.80 + 0.1	V
V_{REF}	Reference voltage	1.40 – 0.2	1.40 + 0.2	V
V_{DIL}	RSL data input - low voltage	V_{REF} – 0.5	V_{REF} – 0.2	V
V_{DIH}	RSL data input - high voltage	V_{REF} + 0.2	V_{REF} + 0.5	V
V_{DIS}	RSL data input swing : $V_{DIS} = V_{DIH} - V_{DIL}$	0.4	1.0	V
A_{DI}	RSL data asymmetry : $A_{DI} = [(V_{DIH} - V_{REF}) + (V_{DIL} - V_{REF})] / V_{DIS}$	0	–20	%
V_X	RSL clock input - crossing point of true and complement signals	1.3	1.8	V
V_{CM}	RSL clock input - common mode $V_{CM} = (V_{CIH} + V_{CIL}) / 2$	1.4	1.7	V
$V_{CIS, CTM}$	RSL clock input swing : $V_{CIS} = V_{CIH} - V_{CIL}$ (CTM, CTMN pins).	0.35	1.00	V
$V_{CIS, CFM}$	RSL clock input swing : $V_{CIS} = V_{CIH} - V_{CIL}$ (CFM, CFMN pins).	0.225	1.00	V
$V_{IL, CMOS}$	CMOS input low voltage	– 0.3	+ (V_{CMOS} / 2 – 0.25)	V
$V_{IH, CMOS}$	CMOS input high voltage	V_{CMOS} / 2+0.25	V_{CMOS} + 0.3	V

27. Timing Conditions

Timing Conditions

Symbol	Parameter		MIN.	MAX.	Unit	Figures
t_{CYCLE}	CTM and CFM cycle times	-C60	3.33	3.83	ns	Figure 30-1
		-C71	2.81	3.83		
		-C80	2.50	3.83		
t_{CR}, t_{CF}	CTM and CFM input rise and fall times		0.2	0.5	ns	Figure 30-1
t_{CH}, t_{CL}	CTM and CFM high and low times		40%	60%	t_{CYCLE}	Figure 30-1
t_{TR}	CTM-CFM differential	(MSE/MS=0/0)	0.0	1.0	t_{CYCLE}	Figure 22-1
		(MSE/MS=1/1) Note1	0.9	1.0		Figure 30-1
t_{DCW}	Domain crossing window		–0.1	+0.1	t_{CYCLE}	Figure 35-1
t_{DR}, t_{DF}	DQA/DQB/ROW/COL input rise/fall times		0.2	0.65	ns	Figure 31-1
t_S, t_H	DQA/DQB/ROW/COL-to-CFM setup/hold time	t_{CYCLE}=2.50ns	0.200 Note4	—	ns	Figure 31-1
		t_{CYCLE}=2.81ns	0.240 Note3,4	—		
		t_{CYCLE}=3.33ns	0.275 Note2,4	—		
t_{DR1}, t_{DF1}	SIO0, SIO1 input rise and fall times		—	5.0	ns	Figure 33-1
t_{DR2}, t_{DF2}	CMD,SCK input rise and fall times		—	2.0	ns	Figure 33-1
t_{CYCLE1}	SCK cycle time - Serial control register transactions		1,000	—	ns	Figure 33-1
	SCK cycle time - Power transitions		10	—	ns	Figure 33-1
t_{CH1}, t_{CL1}	SCK high and low times		4.25	—	ns	Figure 33-1
t_{S1}	CMD setup time to SCK rising or falling edge Note5		1.25	—	ns	Figure 33-1
t_{H1}	CMD hold time to SCK rising or falling edge Note5		1	—	ns	Figure 33-1
t_{S2}	SIO0 setup time to SCK falling edge		40	—	ns	Figure 33-1
t_{H2}	SIO0 hold time to SCK falling edge		40	—	ns	Figure 33-1
t_{S3}	PDEV setup time on DQA5..0 to SCK rising edge		0	—	ns	Figure 23-4, 33-2
t_{H3}	PDEV hold time on DQA5..0 to SCK rising edge		5.5	—	ns	Figure 23-4, 33-2
t_{S4}	ROW2..0, COL4..0 setup time for quiet window Note6		–1	—	t_{CYCLE}	Figure 23-4
t_{H4}	ROW2..0, COL4..0 hold time for quiet window		5	—	t_{CYCLE}	Figure 23-4
$V_{IL, CMOS}$	CMOS input low voltage - over / undershoot voltage duration is less than or equal to 5 ns		–0.7	+(V_{CMOS}/2–0.6)	V	
$V_{IH, CMOS}$	CMOS input high voltage - over / undershoot voltage duration is less than or equal to 5ns		V_{CMOS}/2 + 0.6	V_{CMOS} + 0.7	V	
t_{NPQ}	Quiet on ROW / COL bits during NAP / PDN entry		4	—	t_{CYCLE}	Figure 23-3
$t_{READTOCC}$	Offset between read data and CC packets (same device)		12	—	t_{CYCLE}	Figure 25-1
$t_{CCSAMTOREAD}$	Offset between CC packet and read data (same device)		8	—	t_{CYCLE}	Figure 25-1
t_{CE}	CTM/CFM stable before NAP/PDN exit		2	—	t_{CYCLE}	Figure 23-4
t_{CD}	CTM/CFM stable after NAP/PDN entry		100	—	t_{CYCLE}	Figure 23-3
t_{FRM}	ROW packet to COL packet ATTN framing delay		7	—	t_{CYCLE}	Figure 23-2
t_{NLIMIT}	Maximum time in NAP mode		—	10	μs	Figure 23-1
t_{REF}	Refresh interval		—	32	ms	Figure 24-1
t_{CCTRL}	Current control interval		34 t_{CYCLE}	100 ms	—	Figure 25-1
t_{TEMP}	Temperature control interval		—	100	ms	Figure 25-2
t_{TCEN}	TCE command to TCAL command		150	—	t_{CYCLE}	Figure 25-2
t_{TCAL}	TCAL command to quiet window		2	2	t_{CYCLE}	Figure 25-2
$t_{TCQUIET}$	Quiet window (no read data)		140	—	t_{CYCLE}	Figure 25-2
t_{PAUSE}	RDRAM delay (no RSL operations allowed)		—	200	μs	Figure 22-1
t_{BURST}	Interval after PDN or NAP (with self-refresh) exit in which all banks of the RDRAM must be refreshed at least once.		—	200	μs	Figure 24-2

Notes 1. MSE/MS are fields of the SKIP register. For this combination (skip override) the t_{DCW} parameter range is effectively 0.0 to 0.0.

2. This parameter also applies to a -C80 or -C71 part when operated with t_{CYCLE} = 3.33 ns.

3. This parameter also applies to a -C80 part when operated with t_{CYCLE} = 2.81ns.

4. $t_{S,MIN}$ and $t_{H,MIN}$ for other t_{CYCLE} values can be interpolated between or extrapolated from the timings at the 3 specified t_{CYCLE} values.

5. With $V_{IL,CMOS} = 0.5\ V_{CMOS} - 0.6$ V and $V_{IH,CMOS} = 0.5\ V_{CMOS} + 0.6$ V

6. Effective hold becomes $t_{H4}' = t_{H4} + [PDNXA \bullet 64 \bullet t_{SCYCLE} + t_{PDNXB,MAX}] - [PDNX \bullet 256 \bullet t_{SCYCLE}]$ if $[PDNX \bullet 256 \bullet t_{SCYCLE}] < [PDNXA \bullet 64 \bullet t_{SCYCLE} + t_{PDNXB,MAX}]$. See **Figure 23-4**.

28. Electrical Characteristics

Electrical Characteristics

Symbol	Parameter and Conditions	MIN.	MAX.	Unit
Θ_{JC}	Junction-to-Case thermal resistance	—	0.5	°C/Watt
I_{REF}	V_{REF} current @ $V_{REF,MAX}$	–10	+10	μA
I_{OH}	RSL output high current @ ($0 \le V_{OUT} \le V_{DD}$)	–10	+10	μA
I_{ALL}	RSL I_{OL} current @ V_{OL}=0.9 V, $V_{DD,MIN}$, $T_{j,MAX}$ [Note]	30	90	mA
ΔI_{OL}	RSL I_{OL} current resolution step	—	2.0	mA
r_{OUT}	Dynamic output impedance	150	—	Ω
$I_{I,CMOS}$	CMOS input leakage current @ ($0 \le V_{I,CMOS} \le V_{CMOS}$)	–10.0	+10.0	μA
$V_{OL,CMOS}$	CMOS output low voltage @ $I_{OL,CMOS}$ = 1.0 mA	—	0.3	V
$V_{OH,CMOS}$	CMOS output high voltage @ $I_{OH,CMOS}$ = – 0.25 mA	V_{CMOS} – 0.3	—	V

Note This measurement is made in manual current control mode; i.e. with all output device legs sinking current.

29. Timing Characteristics

Timing Characteristics

Symbol	Parameter		MIN.	MAX.	Unit	Figure(s)
t_Q	CTM-to-DQA/DQB output time	t_{CYCLE} = 2.50 ns	–0.260 [Note3]	+0.260 [Note3]	ns	Figure 32-1
		t_{CYCLE} = 2.81 ns	–0.300 [Note2,3]	+0.300 [Note2,3]		
		t_{CYCLE} = 3.33 ns	–0.350 [Note1,3]	+0.350 [Note1,3]		
t_{QR}, t_{QF}	DQA/DQB output rise and fall times		0.2	0.45	ns	Figure 32-1
t_{Q1}	SCK-to-SIO0 delay @ $C_{LOAD,MAX}$ = 20 pF (SD read packet)		—	10	ns	Figure 34-1
t_{HR}	SCK(pos)-to-SIO0 delay @ $C_{LOAD,MAX}$ = 20pF (SD read data hold)		2	—	ns	Figure 34-1
t_{QR1}, t_{QF1}	SIO_{OUT} rise/fall @ $C_{LOAD,MAX}$ = 20 pF		—	5	ns	Figure 34-1
t_{PROP1}	SIO0-to-SIO1 or SIO1-to-SIO0 delay @ $C_{LOAD,MAX}$ = 20 pF		—	10	ns	Figure 34-1
t_{NAPXA}	NAP exit delay - phase A		—	50	ns	Figure 23-4
t_{NAPXB}	NAP exit delay - phase B		—	40	ns	Figure 23-4
t_{PDNXA}	PDN exit delay - phase A		—	4	μs	Figure 23-4
t_{PDNXB}	PDN exit delay - phase B		—	9,000	t_{CYCLE}	Figure 23-4
t_{AS}	ATTN-to-STBY power state delay		—	1	t_{CYCLE}	Figure 23-2
t_{SA}	STBY-to-ATTN power state delay		—	0	t_{CYCLE}	Figure 23-2
t_{ASN}	ATTN/STBY-to-NAP power state delay		—	8	t_{CYCLE}	Figure 23-3
t_{ASP}	ATTN/STBY-to-PDN power state delay		—	8	t_{CYCLE}	Figure 23-3

Notes **1**. This parameter also applies to a -C80 or -C71 part when operated with t_{CYCLE} =3.33 ns.

2. This parameter also applies to a -C80 part when operated with t_{CYCLE} =2.81 ns.

3. $t_{Q,MIN}$ and $t_{Q,MAX}$ for other t_{CYCLE} values can be interpolated between or extrapolated from the timings at the 3 specified t_{CYCLE} values.

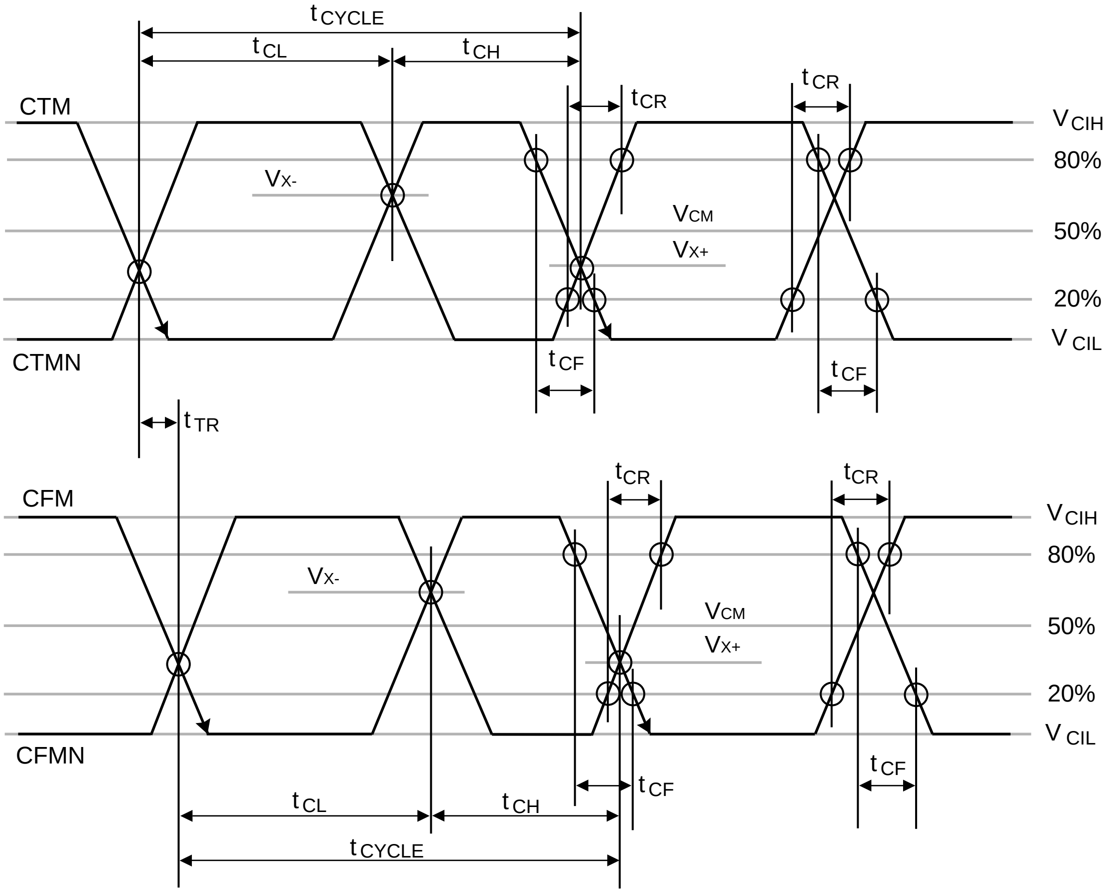
30. RSL Clocking

Figure 30-1 is a timing diagram which shows the detailed requirements for the RSL clock signals on the Channel.

The CTM and CTMN are differential clock inputs used for transmitting information on the DQA and DQB, outputs. Most timing is measured relative to the points where they cross. The t_{CYCLE} parameter is measured from the falling CTM edge to the falling CTM edge. The t_{CL} and t_{CH} parameters are measured from falling to rising and rising to falling edges of CTM. The t_{CR} and t_{CF} rise-and fall-time parameters are measured at the 20 % and 80 % points.

The CFM and CFMN are differential clock outputs used for receiving information on the DQA, DQB, ROW and COL outputs. Most timing is measured relative to the points where they cross. The t_{CYCLE} parameter is measured from the falling CFM edge to the falling CFM edge. The t_{CL} and t_{CH} parameters are measured from falling to rising and rising to falling edges of CFM. The t_{CR} and t_{CF} rise- and fall-time parameters are measured at the 20 % and 80 % points. The t_{TR} parameters specifies the phase difference that may be tolerated with respect to the CTM and CFM differential clock inputs (the CTM pair is always earlier).

Figure 30-1 RSL Timing - Clock Signals



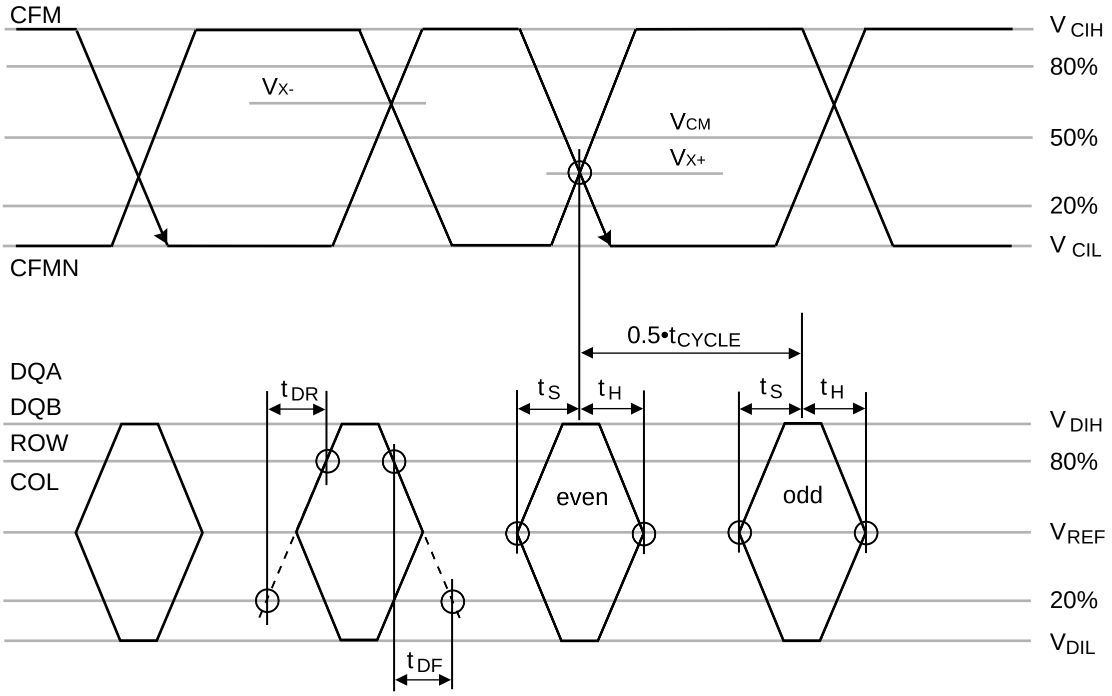
31. RSL - Receive Timing

Figure 31-1 is a timing diagram which shows the detailed requirements for the RSL input signals on the Channel.

The DQA, DQB, ROW, and COL signals are inputs which receive information transmitted by a Direct RAC on the Channel. Each signal is sampled twice per t_{CYCLE} interval. The set/hold window of the sample points is t_S/t_H. The sample points are centered at the 0 % and 50 % points of a cycle, measured relative to the crossing points of the falling CFM clock edge. The set and hold parameters are measured at the V_{REF} voltage point of the input transition.

The t_{DR} and t_{DF} rise- and fall-time parameters are measured at the 20 % and 80 % points of the input transition.

Figure 31-1 RSL Timing - Data Signals for Receive



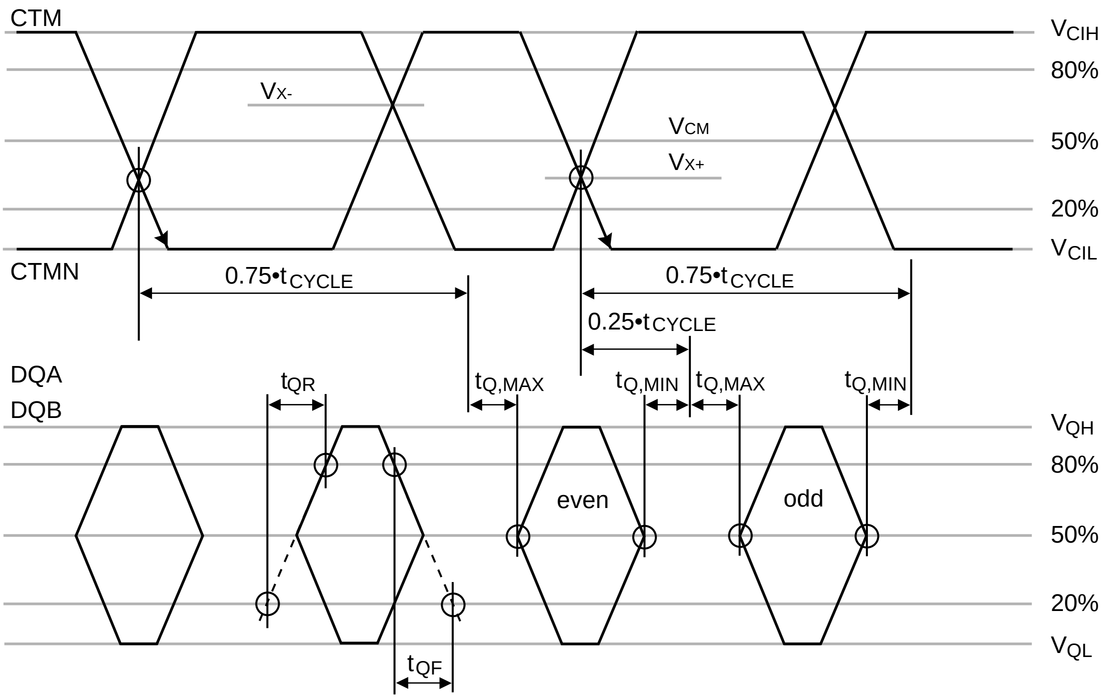
32. RSL - Transmit Timing

Figure 32-1 is a timing diagram which shows the detailed requirements for the RSL output signals on the Channel.

The DQA and DQB signals are outputs to transmit information that is received by a Direct RAC on the Channel. Each signal is driven twice per t_{CYCLE} interval. The beginning and end of the even transmit window is at the 75 % point of the previous cycle and at the 25 % point of the current cycle. The beginning and end of the odd transmit window is at the 25 % point and at the 75 % point of the current cycle. These transmit points are measured relative to the crossing points of the falling CTM clock edge. The size of the actual transmit window is less than the ideal $t_{CYCLE}/2$, as indicated by the non-zero valued of $t_{Q,MIN}$ and $t_{Q,MAX}$. The t_Q parameters are measured at the 50 % voltage point of the output transition.

The t_{QR} and t_{QF} rise- and fall-time parameters are measured at the 20 % and 80 % points of the output transition.

Figure 32-1 RSL Timing - Data Signals for Transmit



33. CMOS - Receive Timing

Figure 33-1 is a timing diagram which shows the detailed requirements for the CMOS input signals.

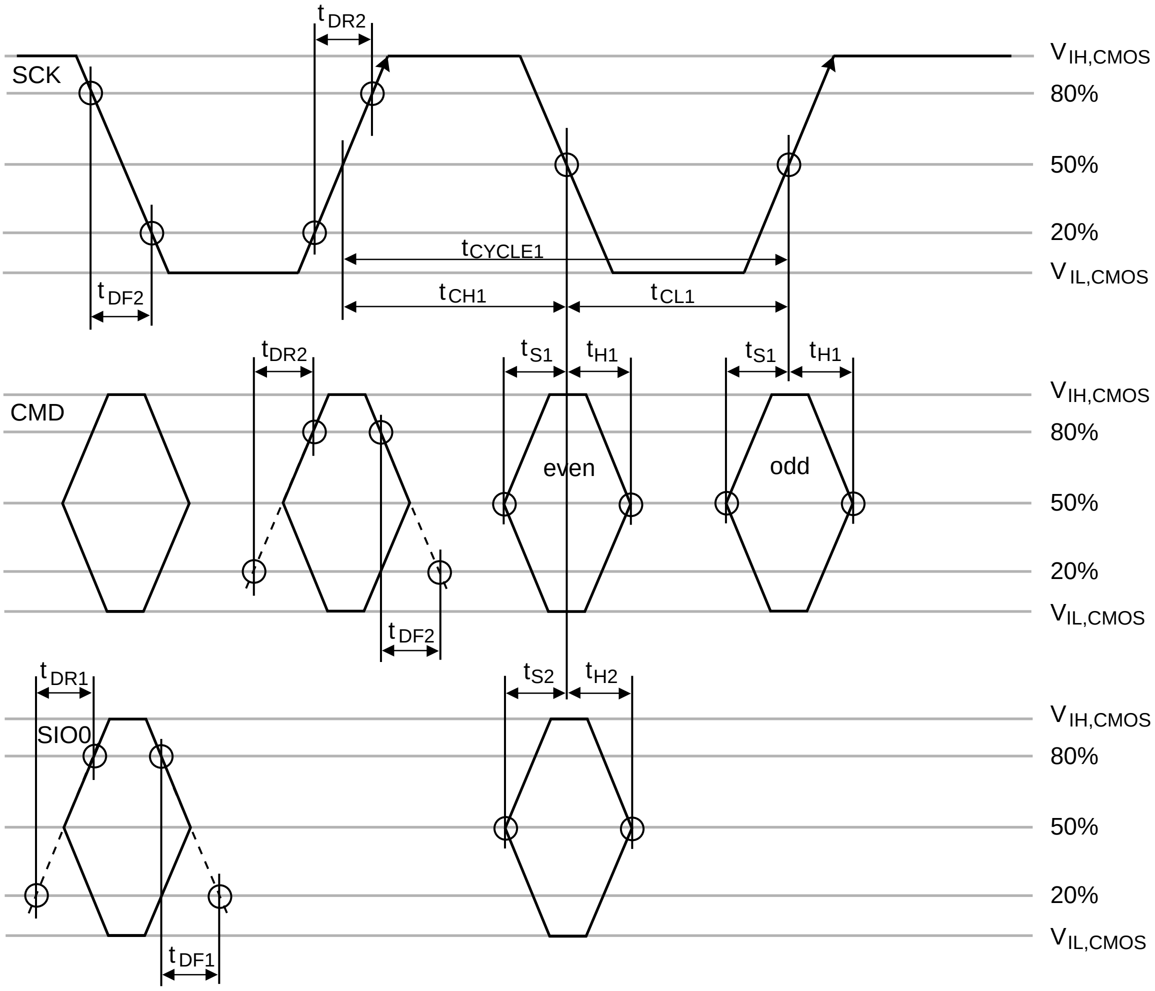
The CMD and SIO0 signals are inputs which receive information transmitted by a controller (or by another RDRAM's SIO1 output). SCK is the CMOS clock signal driven by the controller. All signals are high true.

The cycle time, high phase time, and low phase time of the SCK clock are t_{CYCLE1}, t_{CH1} and t_{CL1}, all measured at the 50 % level. The rise and fall times of SCK, CMD, and SIO0 are t_{DR1} and t_{DF1}, measured at the 20 % and 80 % levels.

The CMD signal is sampled twice per t_{CYCLE1} interval, on the rising edge (odd data) and the falling edge (even data). The set/hold window of the sample points is t_{S1}/t_{H1}. The SCK and CMD timing points are measured at the 50 % level.

The SIO0 signal is sampled once per t_{CYCLE1} interval on the falling edge. The set/hold window of the sample points is t_{S2}/t_{H2}. The SCK and SIO0 timing points are measured at the 50 % level.

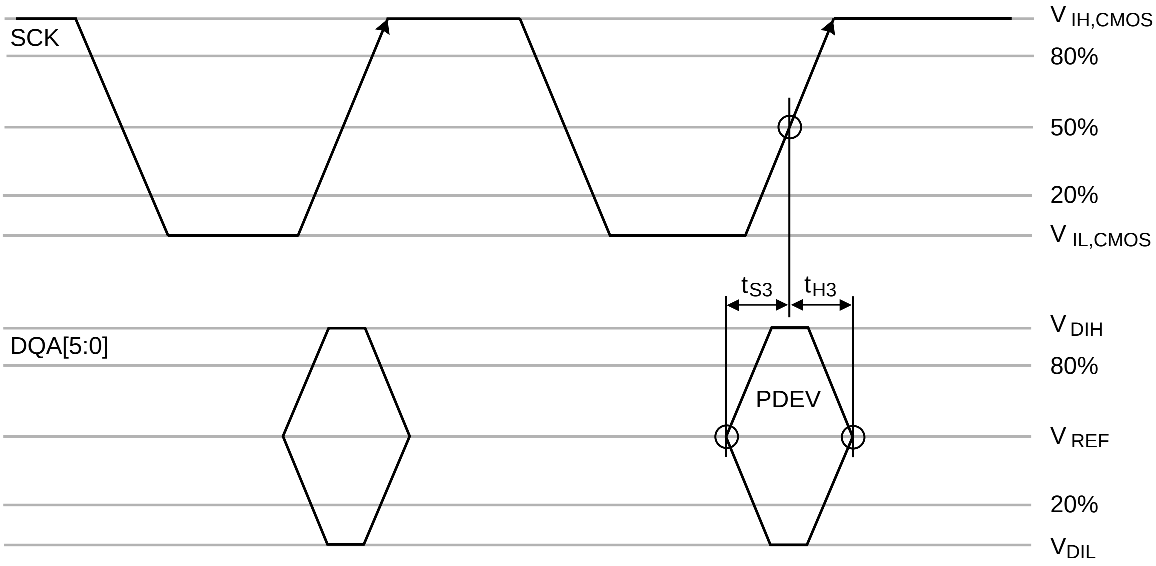
Figure 33-1 CMOS Timing - Data Signals for Receive



The SCK clock is also used for sampling data on RSL input in one situation. Figure23-4 shows the PDN and NAP exit sequences. If the PSX field of the INIT register is one (Figure 22-1 control registers (1/7) “INIT Register”), then the PDN and NAP exit sequences are broadcast; i.e. all RDRAMs that are in PDN or NAP will perform the exit sequence. If the PSX field of the INIT register is zero, then the PDN and NAP exit sequences are directed; i.e. only one RDRAM that is in PDN or NAP will perform the exit sequence.

The address of that RDRAM is specified on the DQA[5:0] bus in the set hold window t_{S3}/t_{H3} around the rising edge of SCK. This is shown Figure 33-2. The SCK timing point is measured at the 50 % level, and the DQA [5:0] bus signals are measured at the V_{REF} level.

Figure 33-2 CMOS Timing - Device Address for NAP or PDN Exit

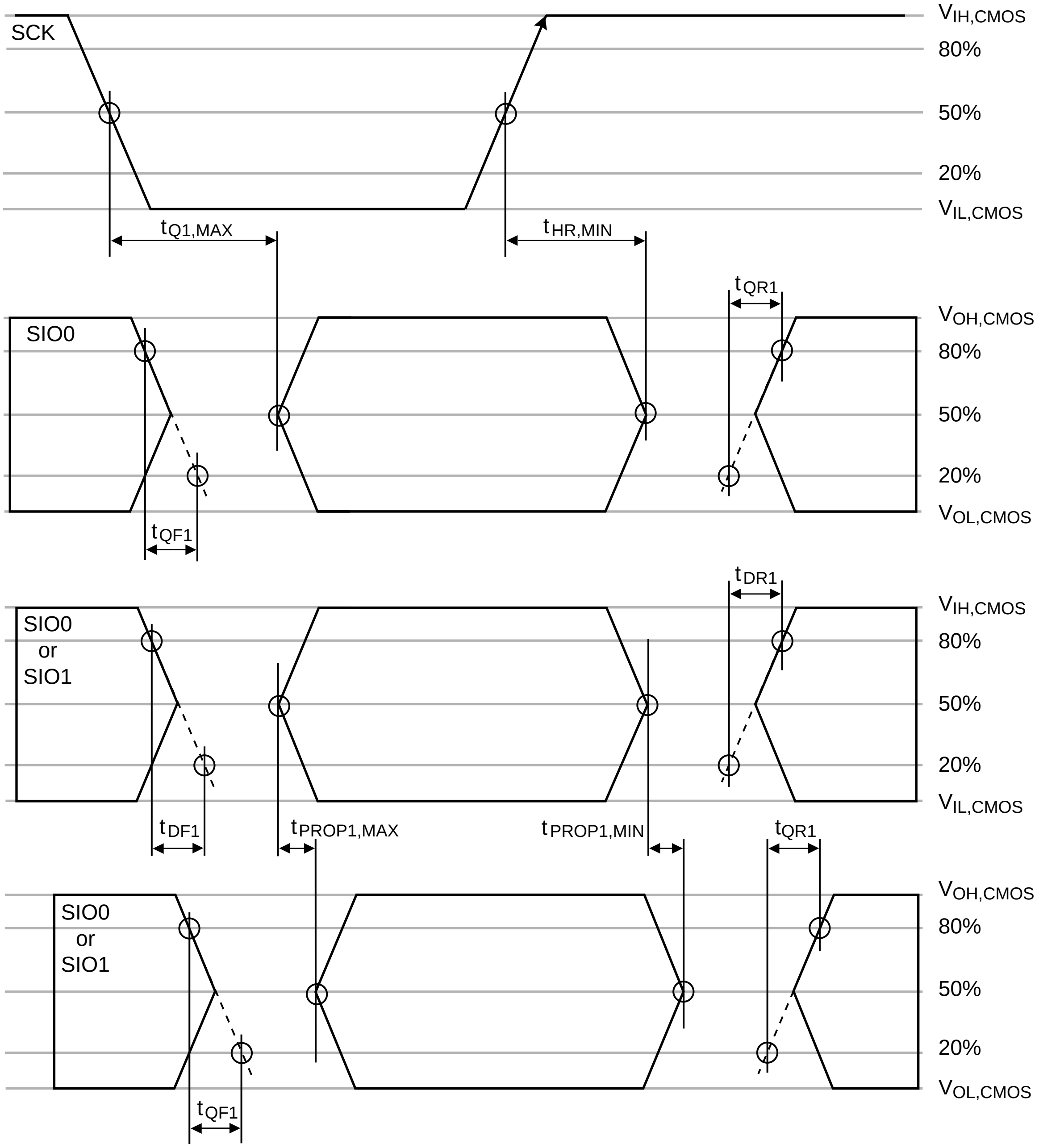


34. CMOS - Transmit Timing

Figure 34-1 is a timing diagram which shows the detailed requirements for the CMOS output signals. The SIO0 signal is driven once per t_{CYCLE1} interval on the falling edge. The clock-to-output window is $t_{Q1,MIN}$ /$t_{Q1,MAX}$. The SCK and SIO0 timing points are measured at the 50 % level. The rise and fall times of SIO0 are t_{QR1} and t_{QF1}, measured at the 20 % and 80 % levels.

Figure34-1 also shows the combinational path connecting SIO0 to SIO1 and the path connecting SIO1 to SIO0 (read data only). The t_{PROP1} parameter specified this propagation delay. The rise and fall times of SIO0 and SIO1 input must be t_{DR1} and t_{DF1}, measured at the 20 % and 80 % levels. The rise and fall times of SIO0 and SIO1 outputs are t_{QR1} and t_{QF1}, measured at the 20 % and 80 % levels.

Figure 34-1 CMOS Timing - Data Signals for Transmit

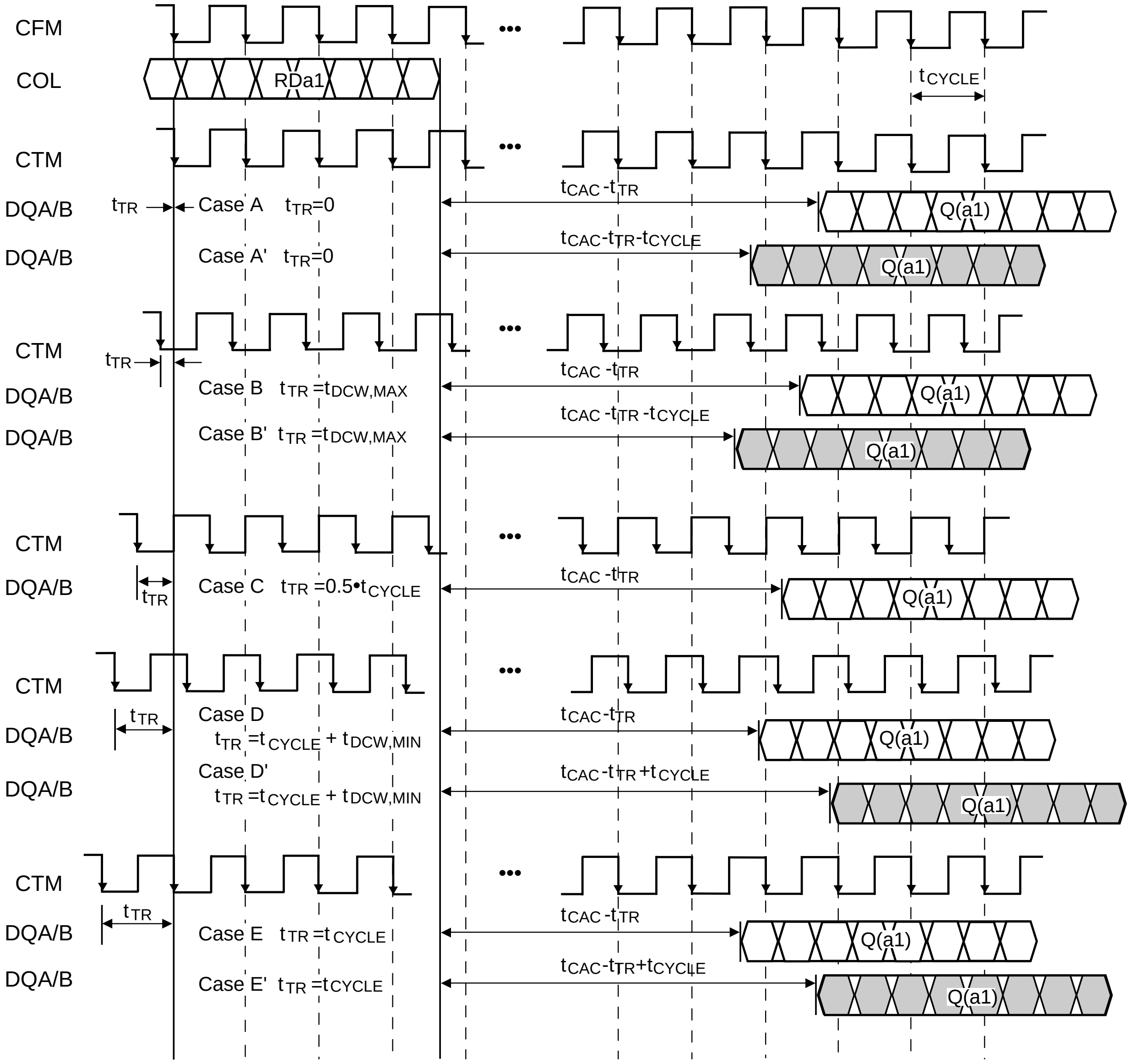


35. RSL - Domain Crossing Window

When read data is returned by the RDRAM, information must cross from the receive clock domain (CFM) to the transmit clock domain (CTM). The t_{TR} parameter permits the CFM to CTM phase to vary though an entire cycle ; i.e. there is no restriction on the alignment of these two clocks. A second parameter t_{DCW} is needed in order to describe how the delay between a RD command packet and read data packet varies as a function of the t_{TR} value.

Figure 35-1 shows this timing for five distinct values of t_{TR}. Case A ($t_{TR}=0$) is what has been used throughout this document. The delay between the RD command and read data is t_{CAC}. As t_{TR} varies from zero to t_{CYCLE} (cases A through E), the command to data delay is ($t_{CAC}-t_{TR}$). When the t_{TR} value is in the range 0 to $t_{DCW,MAX}$, the command to data delay can also be ($t_{CAC}-t_{TR}-t_{CYCLE}$). This is shown as cases A' and B' (the gray packets). Similarly, when the t_{TR} value is in the range ($t_{CYCLE}+t_{DCW,MIN}$) to t_{CYCLE}, the command to data delay can also be ($t_{CAC}-t_{TR}+t_{CYCLE}$). This is shown as cases D' and E' (the gray packets). The RDRAM will work reliably with either the white or gray packet timing. The delay value is selected at initialization, and remains fixed thereafter.

Figure 35-1 RSL Timing - Crossing Read Domains



36. Timing Parameters

Timing Parameters Summary

Parameter	Description	MIN.			MAX.	Units	Figures
		-C80	-C71	-C60			
		-45	-45	-53			
t_{RC}	Row Cycle time of RDRAM banks - the interval between ROWA packets with ACT commands to the same bank.	28	28	28	—	t_{CYCLE}	Figure13-1 Figure14-1
t_{RAS}	RAS-asserted time of RDRAM bank - the interval between ROWA packet with ACT command and next ROWR packet with PRER[Note 1] command to the same bank.	20	20	20	[Note 2] 64μs	t_{CYCLE}	Figure13-1 Figure14-1
t_{RP}	Row Precharge time of RDRAM banks - the interval between ROWR packet with PRER[Note 1] command and next ROWA packet with ACT command to the same bank.	8	8	8	—	t_{CYCLE}	Figure13-1 Figure14-1
t_{PP}	Precharge-to-precharge time of RDRAM device - the interval between successive ROWR packets with PRER[Note 1] commands to any banks of the same device.	8	8	8	—	t_{CYCLE}	Figure10-3
t_{RR}	RAS-to-RAS time of RDRAM device - the interval between successive ROWA packets with ACT commands to any banks of the same device.	8	8	8	—	t_{CYCLE}	Figure12-1
t_{RCD}	RAS-to-CAS Delay - the interval from ROWA packet with ACT command to COLC packet with RD or WR command. Note - the RAS-to-CAS delay seen by the RDRAM core (t_{RCD-C}) is equal to $t_{RCD-C} = 1 + t_{RCD}$ because of differences in the row and column paths through the RDRAM interface.	9	7	7	—	t_{CYCLE}	Figure13-1 Figure14-1
t_{CAC}	CAS Access delay - the interval from RD command to Q read data. The equation for t_{CAC} is given in the TPARM register in Figure 22-1(5/7).	8	8	8	12	t_{CYCLE}	Figure4-1
t_{CWD}	CAS Write Delay - interval from WR command to D write data.	6	6	6	6	t_{CYCLE}	Figure4-1
t_{CC}	CAS-to-CAS time of RDRAM bank - the interval between successive COLC commands.	4	4	4	—	t_{CYCLE}	Figure13-1 Figure14-1
t_{PACKET}	Length of ROWA, ROWR, COLC, COLM or COLX packet.	4	4	4	4	t_{CYCLE}	Figure2-1
t_{RTR}	Interval from COLC packet with WR command to COLC packet which causes retire, and to COLM packet with bytemask.	8	8	8	—	t_{CYCLE}	Figure15-1
t_{OFFP}	The interval (offset) from COLC packet with RDA command, or from COLC packet with retire command (after WRA automatic precharge), or from COLC packet with PREC command, or from COLX packet with PREX command to the equivalent ROWR packet with PRER. The equation for t_{OFFP} is given in the TPARM register in Figure 22-1(5/7).	4	4	4	4	t_{CYCLE}	Figure14-2
t_{RDP}	Interval from last COLC packet with RD command to ROWR packet with PRER.	4	4	4	—	t_{CYCLE}	Figure13-1
t_{RTP}	Interval from last COLC packet with automatic retire command to ROWR packet with PRER.	4	4	4	—	t_{CYCLE}	Figure14-1

Notes 1. Or equivalent PREC or PREX command. See Figure 12-2.

2. This is a constraint imposed by the core, and is therefore in units of ms rather than t_{CYCLE}.

37. Absolute Maximum Ratings

Absolute Maximum Ratings

Symbol	Parameter	MIN.	MAX.	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS pin with respect to GND	–0.3	V_{DD} +0.3	V
$V_{DD,ABS}$,$V_{DDa,ABS}$	Voltage on V_{DD} and V_{DDa} with respect to GND	–0.5	V_{DD} +1.0	V
T_{STORE}	Storage temperature	–50	+100	°C

Caution **Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

38. I_{DD} - Supply Current Profile

I_{DD} - Supply Current Profile

I_{DD} value	RDRAM blocks consuming power	@ t_{CYCLE} Note 1	MIN.	MAX.	Unit
$I_{DD,PDN}$	Self-refresh only for INIT.LSR=0		—	6.0	mA
$I_{DD,NAP}$	T/RCLK-Nap		—	4.2	mA
$I_{DD,STBY}$	T/RCLK,ROW-demux	2.50 ns	—	90	mA
		2.81 ns	—	80	
		3.33 ns	—	70	
		3.83 ns	—	65	
$I_{DD,ATTN}$	T/RCLK, ROW-demux, COL-demux	2.50 ns	—	135	mA
		2.81 ns	—	125	
		3.33 ns	—	115	
		3.83 ns	—	105	
$I_{DD,ATTN-W}$	T/RCLK, ROW-demux, COL-demux, DQ-demux, 1•WR-SenseAmp, 4•ACT-Bank	2.50 ns	—	720	mA
		2.81 ns	—	670	
		3.33 ns	—	620	
		3.83 ns	—	570	
$I_{DD,ATTN-R}$	T/RCLK, ROW-demux, COL-demux, DQ-mux, 1•RD-SenseAmp, 4•ACT-Bank Note 2	2.50 ns	—	630	mA
		2.81 ns	—	580	
		3.33 ns	—	520	
		3.83 ns	—	470	

Notes 1. The CMOS interface consumes power in all power states.

2. This does not include the I_{OL} sink current. The RDRAM dissipates I_{OL}•V_{OL} in each output driver when a logic one is driven.

39. Capacitance and Inductance

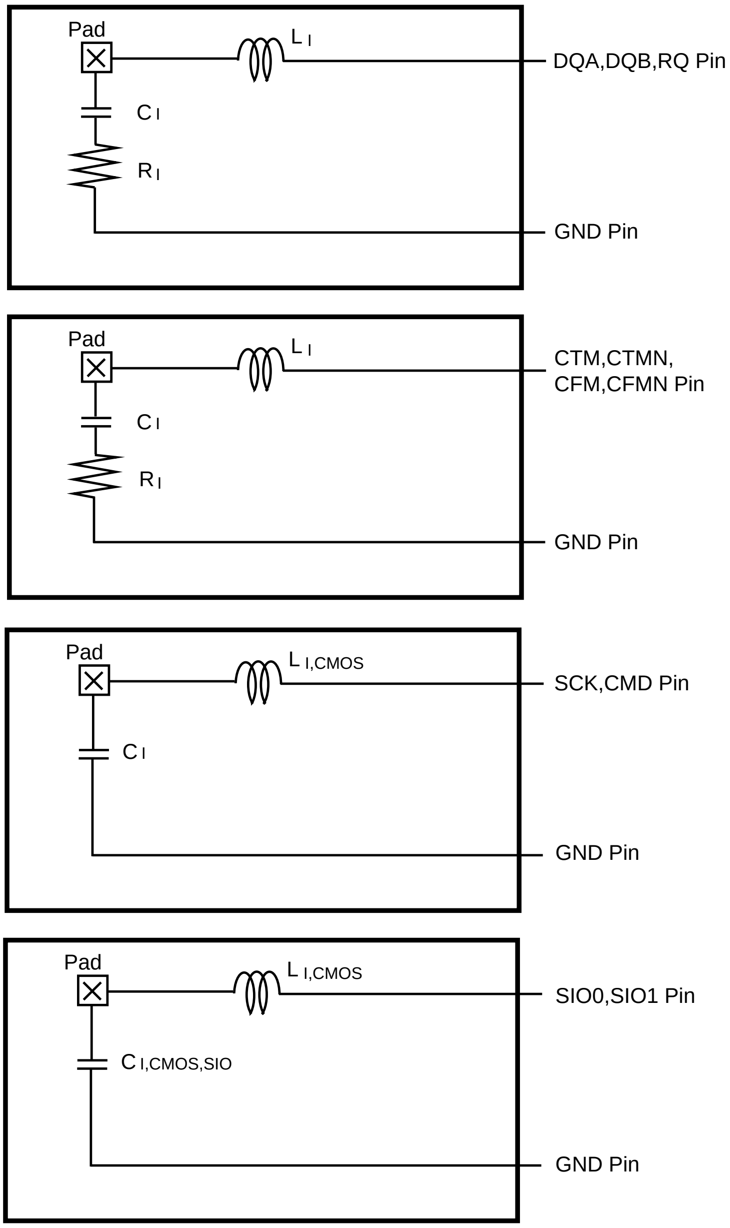
Figure 39-1 shows the equivalent load circuit of the RSL and CMOS pins. The circuit models the load that the device presents to the Channel.

This circuit does not include pin coupling effects that are often present in the packaged device. Because coupling effects make the effective single-pin inductance L_I, and capacitance C_I, a function of neighboring pins, these parameters are intrinsically data-dependent. For purposes of specifying the device electrical loading on the Channel, the effective L_I and C_I are defined as the worst-case values over all specified operating conditions.

L_I is defined as the effective pin inductance based on the device pin assignment. Because the pad assignment places each RSL signal adjacent to an AC ground (a GND or V_{DD} pin), the effective inductance must be defined based on this configuration. Therefore, L_I assumes a loop with the RSL pin adjacent to an AC ground.

C_I is defined as the effective pin capacitance based on the device pin assignment. It is the sum of the effective package pin capacitance and the IO pad capacitance.

Figure 39-1 Equivalent Load Circuit for RSL Pins



RSL Pin Parasitics

Symbol	Parameter and Conditions - RSL pins		MIN.	MAX.	Unit
L_I	RSL effective input inductance		–	4.0	nH
L_{12}	Mutual inductance between any DQA or DQB RSL signals.		–	0.2	nH
	Mutual inductance between any ROW or COL RSL signals.		–	0.6	nH
ΔL_I	Difference in L_I value between any RSL pins of a single device.		–	1.8	nH
C_I	RSL effective input capacitance Note	800 MHz	2.0	2.4	pF
		711 MHz	2.0	2.4	
		600 MHz	2.0	2.6	
C_{12}	Mutual capacitance between any RSL signals.		–	0.1	pF
ΔC_I	Difference in C_I value between any RSL pins of a single device.		–	0.06	pF
R_I	RSL effective input resistance		4	15	Ω

Note This value is a combination of the device IO circuitry and package capacitances.

CMOS Pin Parasitics

Symbol	Parameter and Conditions - CMOS pins	MIN.	MAX.	Unit
$L_{I,CMOS}$	CMOS effective input inductance	–	8.0	nH
$C_{I,CMOS}$	CMOS effective input capacitance (SCK,CMD) Note	1.7	2.1	pF
$C_{I,CMOS,SIO}$	CMOS effective input capacitance (SIO1,SIO0) Note	–	7.0	pF

Note This value is a combination of the device IO circuitry and package capacitances.

40. Interleaved Device Mode

Interleaved Device Mode permits a group of eight RDRAMs on the Channel to collectively respond to acommand. The purpose of this collective response is to limit the number of bits in each dualoct data packet which are read from or written to a single RDRAM device. This capability permits a memory controller to implement hardware for fault detection and correction that can tolerate the complete internal failure of one RDRAM device on a Channel.

The IDM bit of the INIT control register enables this fault tolerant operating mode. When it is set, the RDRAM will interpret the DR4..0 and DC4..0 fields of the ROW and COLC packets differently. Figure 40-1 shows the differences using an example system with eight RDRAMs.

The DEVID4..0 registers of these RDRAMs are initial-ized to “00000” through “00111’. However, when the IDM bit is set, only the upper two bits (DEVID4..3) will be compared to the DR4..3 and DC4..3 fields. This means that ROW and COLC packets will be executed by groups of eight RDRAMs, with a Channel containing from one to four of these groups. The low-order DR2..0 bits are not used when IDM is set, and the low-order DC2..0 bits have a modified function described below.

With IDM set, a directed ACT or PRE command in a ROW packet causes eight RDRAMs to perform the indicated operation. Likewise, when a RD or WR command is specified in a COLC command, the selected group of eight RDRAMs responds. When using IDM, devices must be added to the Channel in groups of eight. An application will typically make the IDM bit setting the same for all RDRAMs on a Channel.

The mechanism for indicating a broadcast ROW packet (DR4F and DR4T are both set to one) is not affected by the setting of the IDM bit; i.e. IDM mode does not change the broadcast ROW packet mechanism.

Likewise, the COLX fields (DX4..0, XOP4..0, and BX5..0) are not changed by IDM mode - all COLX packets are directed to a single device.

When the IDM bit is set, COLM packets should not be used (the M bit should be set to zero, selecting only COLX packets). This is because the mapping of bytes to RDRAM storage cells is changed by IDM mode.

Returning to Figure 40-1, the remaining fields of the ROW and COLC packets are interpreted in the same way regardless of the setting of the IDM bit – IDM mode does not affect these fields. Specifically, the BR5..0 and BC5..0 fields of the ROW and COLC packets are used to select one of the banks just as when IDM is not set. The R8..0 field of the ROW packet selects a row of the selected (BR5..0) bank to load into the bank’s sense amp. And the C6..0 field selects one dualoct of the selected (BC5..0) bank’s sense amp.

The IDM bit affects what is done with this selected dualoct. When IDM is not set, the dualoct is driven onto the Channel by the single selected RDRAM device. When IDM is set, the RDRAM of the eight device group selected by DC4..3 drives 16 or 24 bits (x18 device) of the 144-bit dualoct. The bits driven are a function of the DEVID2..0 RDRAM register field, the DC2..0 COLC packet field, and the device width (x18). Figure 40-1 shows the mapping that is appropriate for DC2..0=000.

Figure 40-2 and Figure 40-3 show the mapping for all eight values of DC2..0. There are eight mappings, which are rotated among the eight devices using the following equation:

$$\text{Pin} = 7 - 4 \bullet (\text{DEVID2}\wedge\text{DC2})$$

$$- 2 \bullet (\text{DEVID1}\wedge\text{DC1}) - 1 \bullet (\text{DEVID0}\wedge\text{DC0}) \quad \text{(Eq 1)}$$

where “^” is the exclusive-or function. “Pin” is the pin number that is driven by the RDRAM with the DEVID2..0 value. For example, Pin=0 means the RDRAM drives DQA0 and DQB0, and so forth. The DQA8 pin is always driven with DQA7, and DQB8 is always driven with DQB6 for x18 devices. For x16 devices, the DQA8 and DQB8 pins are not used. For each of the eight mappings, the eight-RDRAM group supplies a complete dualoct. As the application steps through eight values of DC2..0, all the bits of the eight underlying dualocts will be accessed. Thus, an eight-RDRAM group appears to be a single RDRAM with eight times the normal page size, with the DC2..0 field providing the extra column addressing informa-tion (beyond what C6..0 provides).

Figure 40-1 ACT, PRE, RD, and WR Commands for Eight RDRAM System with IDM = 1

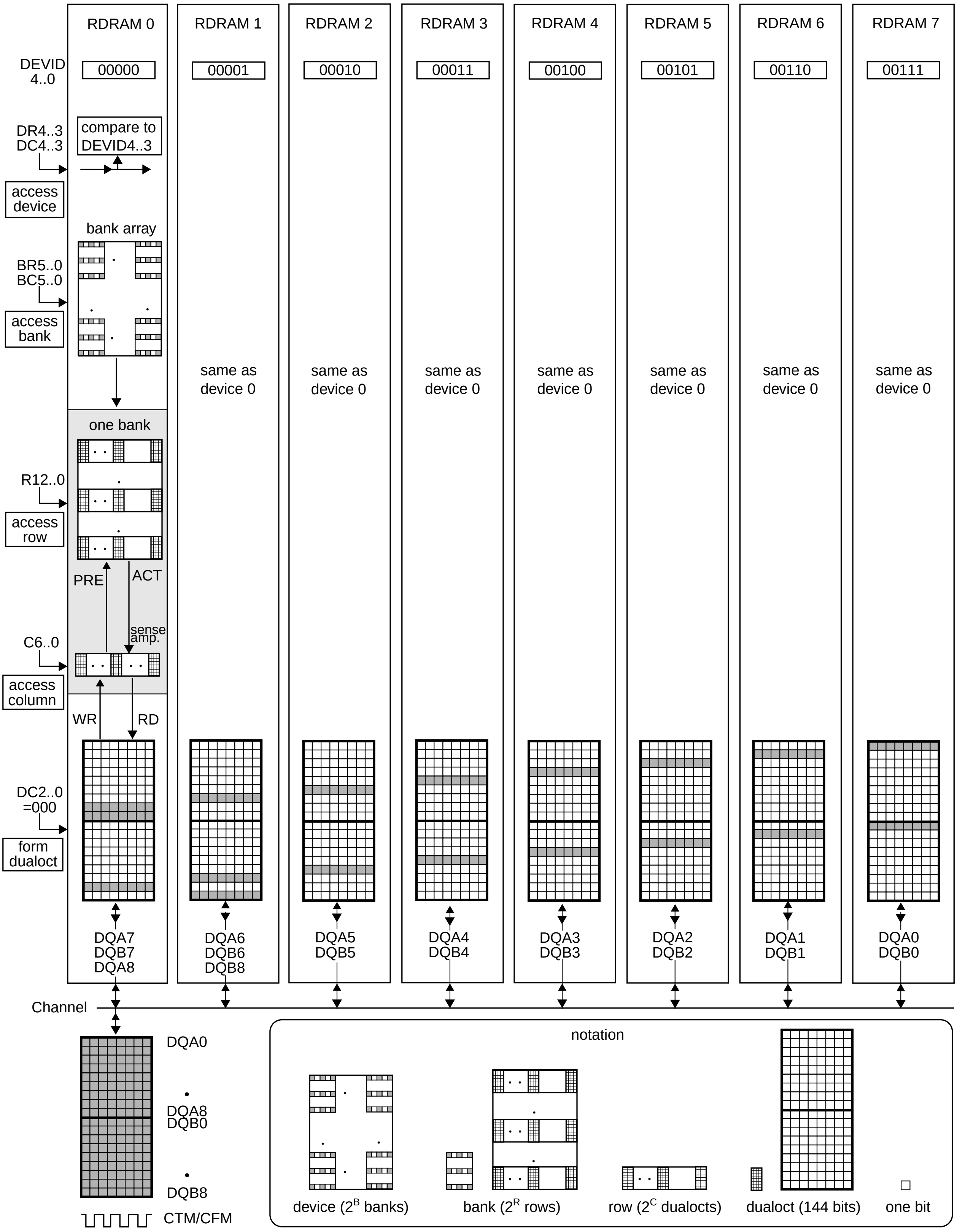


Figure 40-2 Mapping from DEVID2..0 and DC2..0 Fields to DQ Packet with IDM = 1

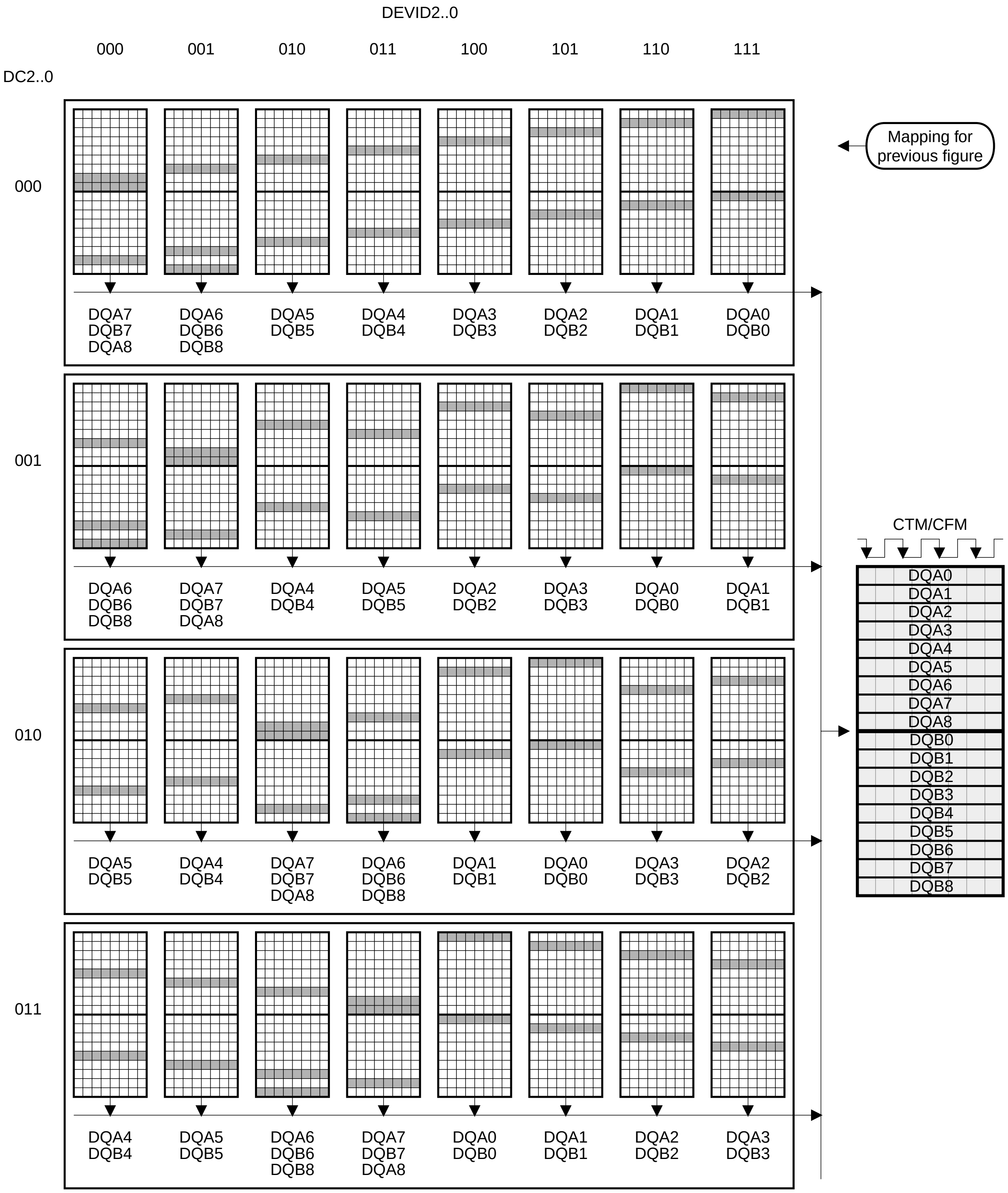
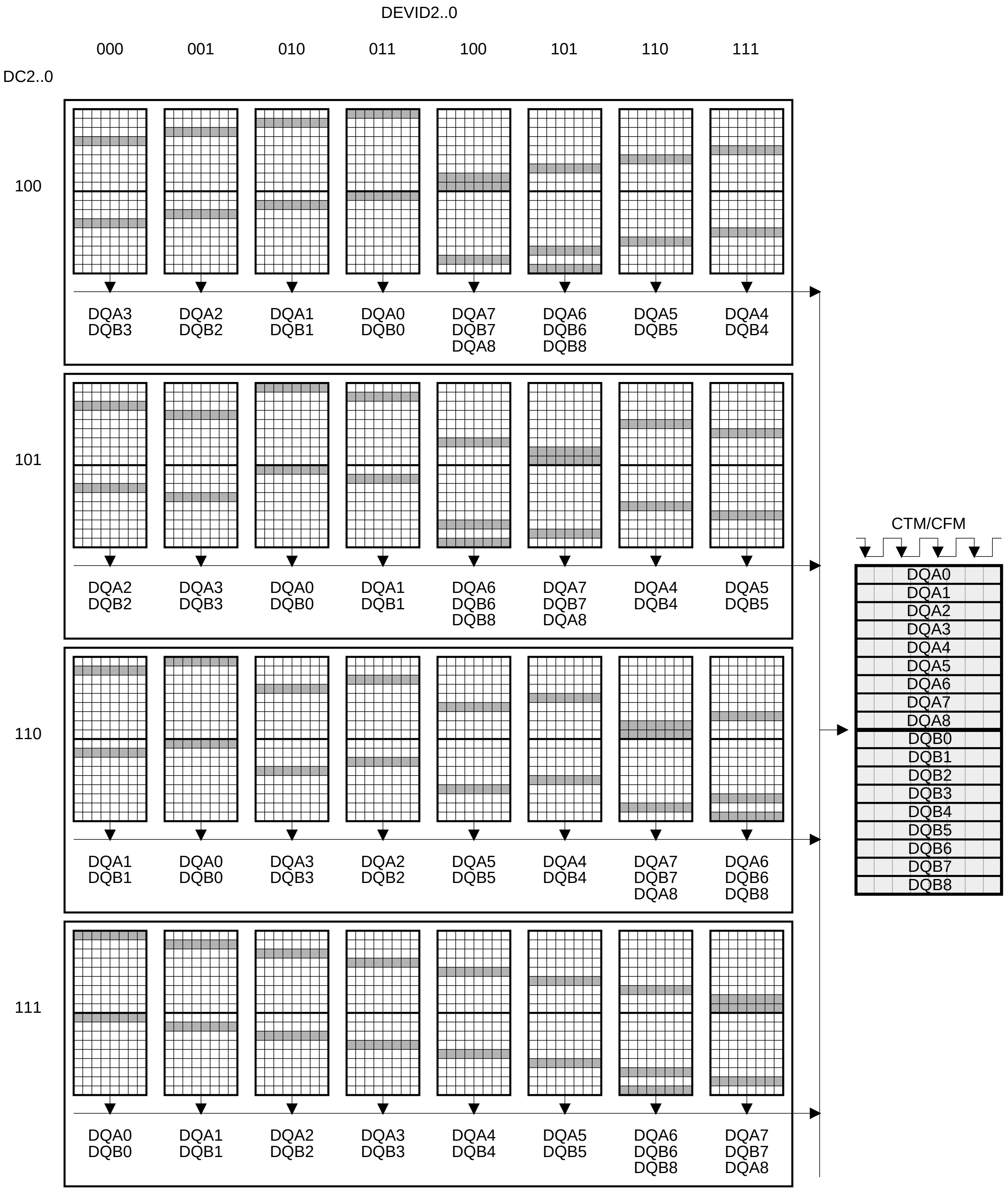


Figure 40-3 Mapping from DEVID2..0 and DC2..0 Fields to DQ Packet with IDM = 1 (continued)



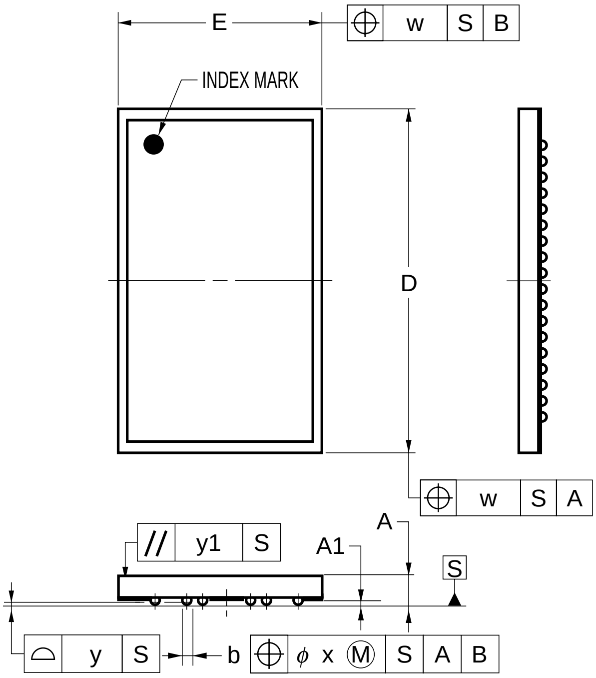
41. Glossary of Terms

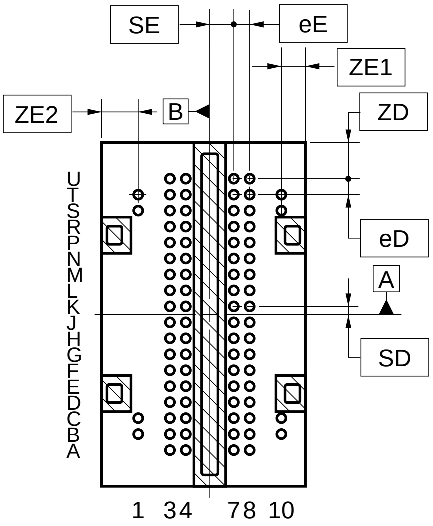
ACT	Activate command from AV field.
activate	To access a roe and place in sense amp.
activate	To access a row and place in sense amp.
adjacent	Two RDRAM banks which share sense amps (also called doubled banks).
ASYM	CCA register field for RSL V_{OL} / V_{OH}.
ATTN	Power state – ready for ROW / COL packets.
ATTNR	Power state – transmitting Q packets.
ATTNW	Power state – receiving D packets.
AV	Opcode field in ROW packets.
bank	A block of $2^{RBIT} \bullet 2^{CBIT}$ storage cells in the core of the RDRAM.
BC	Bank address field in CLC packet.
BBIT	CNFGA register field - # bank address bits.
broadcast	An operation executed by all RDRAMs.
BR	Bank address field in ROW packets.
bubble	Idle cycle(s) on RDRAM pins needed because of a resource constraint.
BYT	CNFGB register field – 9 bits per byte.
BX	Bank address field in COLX packet.
C	Column address field in COLC packet.
CAL	Calibrate (I_{OL}) command in XOP field.
CBIT	CNFGB register field - # column address bits.
CCA	Control register – current control A.
CCB	Control register – current control B.
CFM,CFMN	Clock pins for receiving packets.
Channel	ROW / COL / DQ pins and external wires.
CLRR	Clear reset command from SOP field.
CMD	CMOS pins for initialization / power control.
CNFGA	Control register with configuration fields.
CNFGB	Control register with configuration fields.
COL	Pins for column-access control.
COLC	Column operation packet on COL pins.
COLM	Write mask packet on COL pins.
column	Rows in a bank or activated in sense amps have 2^{CBTI} dualocts column storage.
Command	A decoded bit-combination from a field.
COLX	Extended operation packet on COL pins.
controller	A logic-device which drives the ROW / COL / DQ wires for a Channel of RDRAMs.
COP	Column opcode field in COLC packet.
core	The banks and sense amps of an RDRAM.
CTM, CTMN	Clock pins for transmitting packets.
Current control	Periodic operations to update the proper I_{OL} Value of RSL output drivers.
D	Write data packet on DQ pins.
DBL	CNFGB register field – doubled-bank.
DC	Device address field in COLC packet.
device	An RDRAM on a Channel.
DEVID	Control register with device address that is matched against DR, DC, and DX fields.
DM	Device match for ROW packet decode.
Doubled-bank	RDRAM with shared sense amp.
DQ	DQA and DQB pins.
DQA	Pins for data byte A.
DQB	Pins for data byte B.
DQS	NAPX register field – PDN/NAP exit.
DR,DR4T,DR4F	Device address field and packet framing fields in ROW and ROWE packets.
dualoct	16 bytes – the smallest addressable datum.
DX	Device address field in COLX packet.
field	A collection of bits in a packet.
INIT	Control register with initialization fields.
initialization	Configuring a Channel of RDRAMs so they are ready to respond to transactions.
LSR	CNFGA register field – low-power self-refresh.
M	Mask opcode field (COLM/COLX packet).
MA	Field in COLM packet for masking byte A.
MB	Field in COLM packet for masking byte B.
MSK	Mask command in M field.
MVER	Control register – manufacturer ID.
NAP	Power state – needs SCK/CMD wakeup.
NAPR	Nap command in ROP field.
NAPRC	Conditional nap command in ROP field.
NAPXA	NAPX register field – NAP exit delay A.
NAPXB	NAPX register field – NAP exit delay B.
NOCOP	No-operation command in COP field.
NOROP	No-operation command in ROP field.
NOXOP	No-operation command in XOP field.
NSR	INIT register field – NAP self-refresh.
packet	A collection of bits carried on the Channel.
PDN	Power state – needs SCK/CMD wakeup.
PDNR	Powerdown command in ROP field.
PDNXA	Control register – PDN exit delay A.
PDNXB	Control register – PDN exit delay B.
pin efficiency	The fraction of non-idle cycles on a pin.
PRE	PREC, PRER, PREX precharge commands.
PREC	Precharge command in COP field.
precharge	Prepares sense amp and bank for activate.
PRER	Precharge command in ROP field.

PREX	Precharge command in XOP field.
PSX	INIT register field – PDN/NAP exit.
PSR	INIT register field – PDN self-refresh.
PVER	CNFGB register field – protocol version.
Q	Read data packet on DQ pins.
R	Row address field of ROWA packet.
RBIT	CNFGB register field - #row address bits.
RD/RDA	Read (/precharge) command in COP field.
read	Operation of accessing sense amp data.
receive	Moving information from the Channel into the RDRAM (a serial stream is demuxed).
REFA	Refresh-activate command in ROP field.
REFB	Control register – next bank (self-refresh).
REFBIT	CNFGA register field – ignore bank bits (for REFA and self-refresh).
REFP	Refresh-precharge command in ROP field.
REFR	Control register – next row for REFA.
refresh	Periodic operations to restore storage cells.
retire	The automatic operation that stores write buffer into sense amp after WR command.
RLX	RLXC, RLXR, RLXX relax commands.
RLXC	Relax command in COP field.
RLXR	Relax command in ROP field.
RLXX	Relax command in XOP field.
ROP	Row-opcode field in ROWR packet.
row	2^{CBIT} dualocts of cells (bank/sense amp).
ROW	Pins for row-access control
ROW	ROWA or ROWR packets on ROW pins.
ROWA	Activate packet on ROW pins.
ROWR	Row operation packet on ROW pins.
RQ	Alternate name for ROW/COL pins.
RSL	Rambus Signal levels.
SAM	Sample (I_{OL}) command in XOP field.
SA	Serial address packet for control register transactions w/ SA address field.
SBC	Serial broadcast field in SRQ.
SCK	CMOS clock pin.
SD	Serial data packet for control register transactions w/ SD data field.
SDEV	Serial device address in SRQ packet.
SDEVID	INIT register field – Serial device ID.
self-refresh	Refresh mode for PDN and NAP.
sense amp	Fast storage that holds copy of bank’s row.
SETF	Set fast clock command from SOP field.
SETR	Set reset command from SOP field.
SINT	Serial interval packet for control register read/write transactions.
SIO0,SIO1	CMOS serial pins for control registers.
SOP	Serial opcode field in SRQ.
SRD	Serial read opcode command from SOP.
SRP	INIT register field – Serial repeat bit.
SRQ	Serial request packet for control register read/write transactions.
STBY	Power state – ready for ROW packets.
SVER	Control register – stepping version.
SWR	Serial write opcode command from SOP.
TCAS	TCLSCAS register field – t_{CAS} core delay.
TCLS	TCLSCAS register field – t_{CLS} core delay.
TCLSCAS	Control register – t_{CAS} and t_{CLS} delay.
TCYCLE	Control register – t_{CYCLE} delay.
TDAT	Control register – t_{DAC} delay.
TEST77	Control register – for test purposes.
TEST78	Control register – for test purposes.
TRDLY	Control register – t_{RDLY} delay.
transaction	ROW, COL, DQ packets for memory access.
transmit	Moving information from the RDRAM onto the Channel (parallel word is muxed).
WR/WRA	Write (/precharge) command in COP field.
write	Operation of modifying sense amp data.
XOP	Extended opcode field in COLX packet.

42. Package Drawing

80-ball FBGA (μBGA) (17.16 × 10.2)





ITEM	MILLIMETERS
D	17.16±0.10
E	10.2±0.1
w	0.2
A	0.96±0.10
A1	0.40±0.05
$\boxed{eD}$	0.8
$\boxed{eE}$	0.8
b	0.50±0.05
x	0.08
y	0.1
y1	0.2
$\boxed{SD}$	0.4
$\boxed{SE}$	1.2
$\boxed{ZD}$	1.78
$\boxed{ZE1}$	1.1
$\boxed{ZE2}$	1.9

ECA-TS2-0051-02

43. Recommended Soldering Conditions

Please consult our sales office for soldering conditions of the μPD488588.

Type of Surface Mount Device

μPD488588FF-DH1 : 80-ball FBGA (μBGA) (17.16 × 10.2)

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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