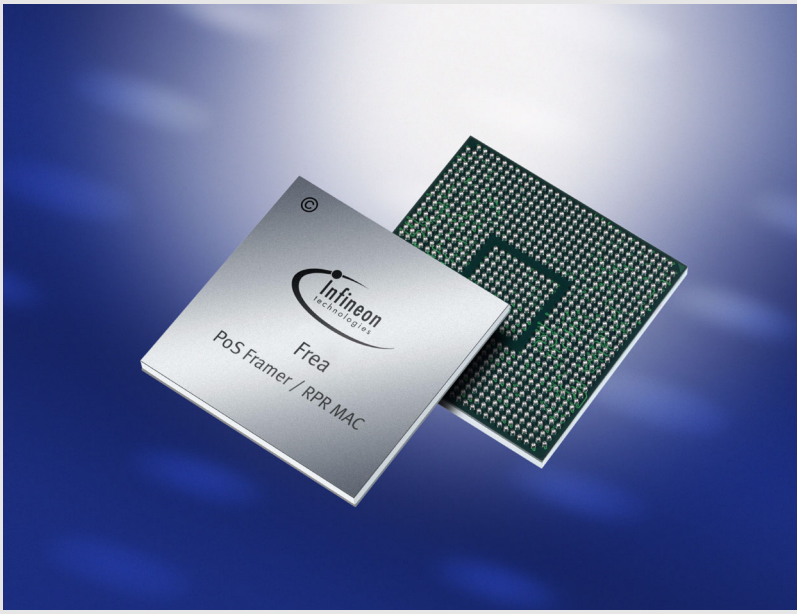
Semiconductor Solutions for High Speed Communications and Fiber Optic Applications

The Frea™ is a single-chip OC-192c/48c device that supports Resilient Packet Ring (RPR) protocol on both SONET/SDH and 10GbE PHYs.

RPR, a layer two Media Access Control (MAC) technology, significantly increases the bandwidth efficiency of service provider networks by utilizing twice the capacity of traditional SONET/SDH rings. RPR delivers dynamic bandwidth management while preserving the same kind of protection and resiliency found in SONET/SDH networks.

The Frea chip integrates RPR MAC, PoS (Packet-Over-SONET) framer and XAUI SerDes (Serializer/Deserializer) necessary to deploy RPR rings in Metropolitan Area Networks (MANs) and Wide Area Networks (WANs). It also eliminates external memory by including 1 MB of memory on-chip for RPR operation. The Frea chip supports both IEEE 802.17 RPR standard Draft 2.1, and RFC 2892 SRP protocol. It also operates in a PoS framer-only mode, which allows carriers unparalleled flexibility to build legacy PoS networks that can later be configured to RPR through a simple software upgrade.



Frea

High-level Features

- Supports RPR on SONET/SDH, RPR on 10 GbE, and POS only applications
- Maps RPR frames into PoS STS-192c/48c or STM-64c/16c
- Maps RPR frames into 10GbE
- 10GbE MAC processing, compliant with IEEE P802.3ae
- Integrated on-chip memory
- On-chip XAUI mate Serdes
- Provides built-in diagnostics - BERT, loopbacks

SONET/SDH Framer Features

- SONET/SDH STS-192c/48c with full duplex mapping of packets into SONET/SDH payloads
- Pointer and payload processing
- Full-duplex TOH add/drop
- Performs frame-synchronous scrambling and de-scrambling of SONET frame
- Processes section, line and path overhead bytes
- Hardware assistance for APS via K1 and K2 bytes
- Detects SEF, LOS, LOF, LOP, and LOC
- Monitors line AIS-L, RDI-L, and REI-L
- Handles J0 and J1 processing
- Calculates, monitors, and counts B1, B2, and B3 errors
- Supports SF/SD BER algorithm
- Supports REI-P error counting and RDI-P monitoring
- Supports path unequipped and payload label mismatch
- Meets ITU G.707, GR-253, T1.105 standards

PoS Features

- PoS on STS-192c/48c
- Option of CRC-16 or CRC-32
- HDLC/PPP over SONET/SDH *per* IETF RFC 2615, RFC 1662
- RPR Mac Features
- Map RPR frames into SONET/SDH STS-192c/48c and 10GbE
- Supports 802.17 RPR (Draft 2.1) and RFC-2892 SRP protocols
- 16 bit HEC with 16-octet RPR header
- Supports all traffic classes - A0/A1/B(EIR and CIR)/C
- Supports all fairness-control mechanisms - single and multi-choke fairness
- Supports all protection schemes - steering and wrapping
- On-chip low and high priority transit buffers
- PM counters
- On-chip CAM for address lookup

Applications

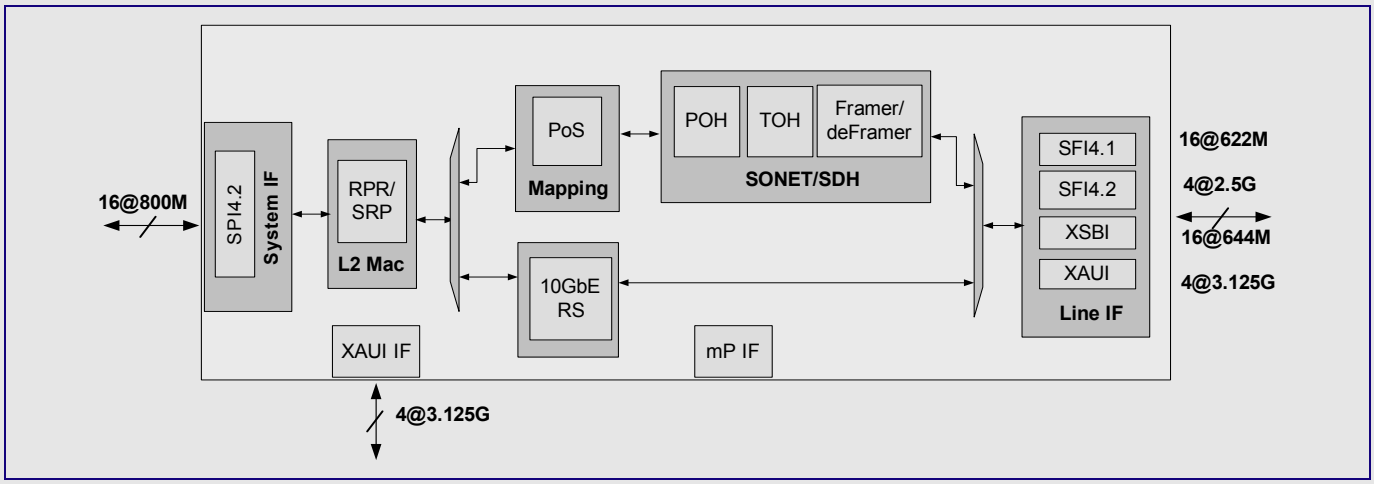
- Edge and core routers
- Multi-Service and LAN switches
- High-speed servers
- PoS and RPR test equipment

Frea™ PEB1755E

RPR on STS-192c/48c SONET/SDH application, RPR on 10GbE application, STS-192c/48c PoS only application

Infineon technologies

Never stop thinking.



Frea 10G Block Diagram

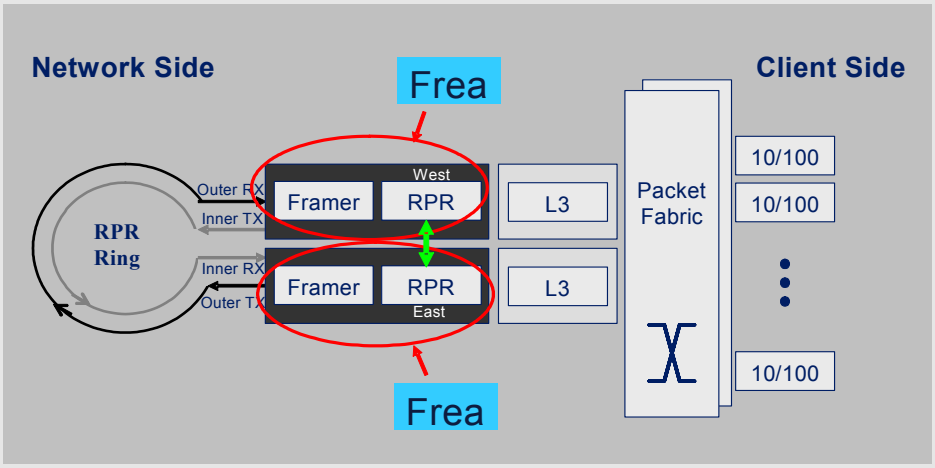
Interfaces

- 622.08 MHz 16-bit line interface (SFI-4.1)
- 2.5 GHz 4-bit line interface (SFI-4.2)
- 644 MHz 16-bit line interface (XSBI)
- 3.125 GHz 4-bit line interface (XAUI)
- 800 MHz 16-bit system interface (SPI-4.2)
- 3.125 GHz 4-bit mate interface (XAUI)
- 155 MHz 16-bit line interface for OC48
- TOH add/drop interface
- JTAG interface
- 16-bit processor interface for configuration, management, and statistics gathering

General Specifications

- 0.13 µm process
- Power: ~8 W
- Core Voltage: 1.3 V
- I/O Buffer Voltage: 3.3 V
- Operating temp. 0 °C to 70 °C
- Full Scan, JTAG, MemBIST
- Flipchip P-FCHBGA-979

Type	Sales Code	Package
OC192/OC48 PoS Framer and RPR Mac	PEB1755E	P-FCHBGA 979



How to reach us:
http://www.infineon.com

Published by
Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81669 München

Template: pb_tmplt.fm/2/2003-05-01

Attention please!

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide.

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Ordering No. B115-H8198-X-X-7600
Printed in Germany
PS 05032. R&L

Published by Infineon Technologies AG