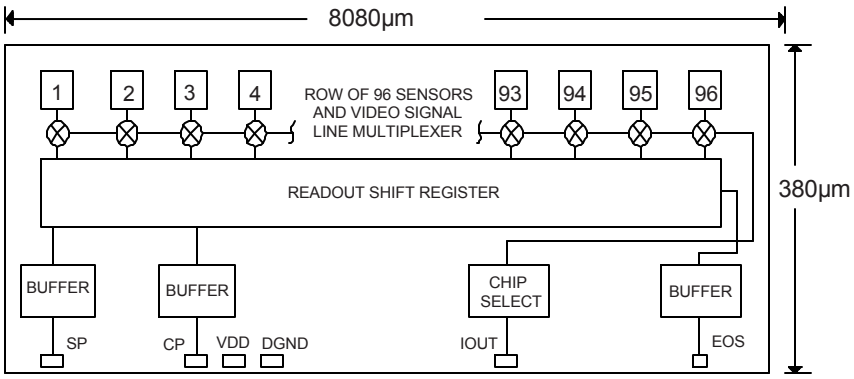
AMI SEMICONDUCTOR

Peripheral Imaging Corporation

PI3012A
300DPI CIS Sensor Chip
Engineering Data Sheet

Description:

Peripheral Imaging Corporation PI3012A CIS sensor chip is a 300 dot per inch resolution linear array image sensor chip which utilizes PIC's proprietary CMOS Image Sensing Technology. This image sensor is to be used for butting end-to-end on a printed circuit board (PCB) using chip-on-board technology to form a scanning array with various lengths. Applications for the sensor array are facsimile, scanner, check reader, and office automation equipment.
Figure 1 is a block diagram of the sensor chip. Each sensor chip consists of 96 detector elements,



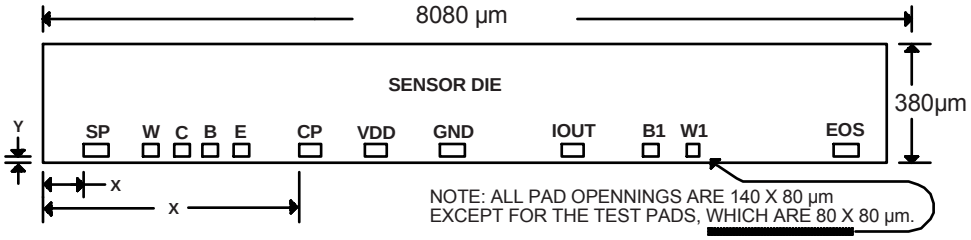
PI3012A SENSOR CHIP
FIGURE 1 BLOCK DIAGRAM

their associated multiplexing switches, buffers, and a chip selector. The detector element-to-element spacing is approximately 84.6 µm. The size of each chip without scribe lines is 8080 µm by 380 µm. Each sensor chip has 6 bonding pads. The pad symbols and functions are described in Table 1.

SYMBOL	FUNCTION
SP	Start Pulse: Input to start the line scan.
CP	Clock Pulse: Input to clock the Shift Register.
VDD	Positive Supply: +5 volt supply connected to substrate.
DGND	Digital Ground: Connection topside common.
IOUT	Signal Current Output: Output for video signal current
EOS	End of Scan Pulse: Output from the shift register at end of scan.

Table 1. Pad Symbols and Functions

Bonding pad layout diagram:



PAD	FUNCTION	Y	X
SP	START INPUT	30	742.5
CP	CLOCK INPUT	30	2767.0
VDD	+ 5 VOLT SUPPLY	30	3124.5
VSS	GROUND	30	3419.0
IOUT	VIDEO SIGNAL OUT	30	5095.5
EOS	SCAN OUTPUT	30	7000.1
W	TP	30	1162.5
C	TP	30	1312.5
B	TP	30	1658.0
E	TP	30	1807.0
B1	TP	30	5407.0
W1	TP	30	5672.0

NOTES:
1. THE DRAWING IS NOT TO SCALE.
2. THE DIE LENGTH AND WIDTH ARE GIVEN AS SHOWN.
3. THE PAD LOCATIONS ARE GIVEN IN THE TABLE.
4. THERE ARE TWO EXAMPLES OF THE X AND Y LOCATIONS SHOWN ON THE FIRST TWO PADS. THEY ARE MEASURED TO THE LEFT BOTTOM CORNER OF THE PAD OPENNING.
5. ALL DIMENSIONS ARE IN µm.
6. TP ARE TEST POINTS, THEY ARE NOT TO BE BONDED OUT.

FIGURE 2. PI3012A PAD LAYOUT AND DIE SIZE.

Figure 2 shows the bonding pad locations for PI3012A Sensor Chip relative to the lower left corner of the die. the die.

Electro-Optical Characteristics (25° C)

Table 2, below, lists the electro-optical characteristics of PI3012A sensor chip at 25° C.

Parameters	Symbols	Typical	Units	Notes
Number of Photo-elements		96	elements	
Pixel-to-pixel spacing		84.6	mm	
Line scanning rate	Tint * (1)	1.3	ms/line	
Clock frequency	f * (2)	2.0	MHz	
Output voltage	Vp*(3)	200	mV	Level is adjustable see (3) This measurement was directly taken on the video line without an amplifier.
Output voltage non-uniformity	Up *(4)	± 7.5	%	
Chip-to-chip non-uniformity	Ud	± 7.5	%	
Dark output voltage	Vd * (5)	10	mV	
Dark output non-uniformity	Ud * (6)	<15	mV	

Table 2. Electro-Optical Characteristic

Notes: (1) Tint stands for the line scanning rate or the integration time. It is determined by the time interval between two start pulses.

(2) f stands for the input clock frequency:
@ 1.0 MHz the total active line scan time for a A4 CIS module is 2.6 ms of the line integration time.
@ 2.0 MHz the total active line scan time for a A4 CIS module is 1.3 ms of the line integration time.

(3) Vp is a video output signal. It is converted from the signal current by charging the video line capacitance. An amplifier buffers the video line capacitance and allows line to charge, and the line is discharged through a shunting switch that shunts it to ground. This amplifier also provides a variable gain, typically 4 to 5 times the voltage that is measured on the video line. Hence, as indicated in the schematic, the video output level is adjustable.

(4) Up = [(Vpmax-Vp)/Vp]x100%
Or [(Vp-Vpmin)/Vp]x100%
Where Vp = (Vpmax+Vpmin)/2
Vpmax is the maximum pixel output voltage in the light.
Vpmin is the minimum pixel output voltage in the light.
Note: In the light means the sensor is exposed to the light.

(5) Vd = (Vdmax+Vdmin)/2
Vdmax is the maximum pixel output voltage in the dark.
Vdmin is the minimum pixel output voltage in the dark.
Note: In the dark means that sensor is light shielded and has no exposure to the light.

(5) Ud = [(Vdmax-Vdmin)/Vd]x100%

Absolute Maximum Ratings:

Parameters	Symbol	Maximum Rating	Units
Power Supply Voltage	VDD	10	Volts
Power Supply Current	IDD	<2.0	ma
Input clock pulse (high level)	Vih	Vdd + 0.5	Volts
Input clock pulse (low level)	Vil	-0.25	Volts
Operating Temperature	Top	0 to 50	°C
Operating Humidity	Hop	10 to 85	RH %
Storage Temperature	Tstg	-25 to 75	°C
Storage Humidity	Hstg	10 to 90	RH %

Recommended Operating Conditions at Room Temperature

Parameters	Symbol	Min.	Typical	Max.	Units	Notes
Power Supply	VDD	4.5	5.0	5.5	Volts	
Input clock pulses high level	Vih	2.8	5.0	VDD	Volts	1
Input clock pulse low level	Vil	0	0	0.8	Volts	1
Operating high level exposed output	Iout					2
Clock Frequency	f	0.1	2.0	5.0	MHz	3
Clock pulse duty cycle			25		%	4
Clock pulse high durations	tw		0.125		μsec	4
Integration time	Tint		1.3	10	ms	3
Operating Temperature	Top		25	50	°C	

Notes:

(1) Applies to both CP and SP.

(2) The output is a current that is proportional to the charges, which are integrated on the phototransistor's base via photon-to-electron conversion. Accordingly during read out, these charges are discharged from the base through the transistor's emitter proportionally to the Beta of the phototransistor. Hence, the emitter current, that flows to the output video line, is the signal that is proportional to the photon integrated charges. To gain the optimum performance, the signal interfacing circuits are designed consistently with this signal process. The video signal current is made to flow into a virtual ground, while the signal extraction circuit is made to integrate these charges that converts these charges into the output signal voltage. The circuit used for the converting the current charge to voltage is attached to this document as a separate sheet.

(3) Although the clock frequency will operate the device at less than 100KHz, it is recommended that the device be operated above 500KHz to maintain the devices performance characteristic.

(4) The clock duty cycle typically is 25 %. However, it can operate with duty cycle as large as 50 %. This specified duty cycle is suggested because the 25 % of clock time, or the positive time of the clock, is used in the reset process, while the remainder of the time is used inextracting the signal during each pixel. Accordingly at low clock frequencies, it would help the

operation if the duty cycle is less than 25 %. On the other hand, since the clock can operate with a 50% duty cycle the operator has additional timing flexibility if it desired.

Switching Characteristics @ 25 ° C.

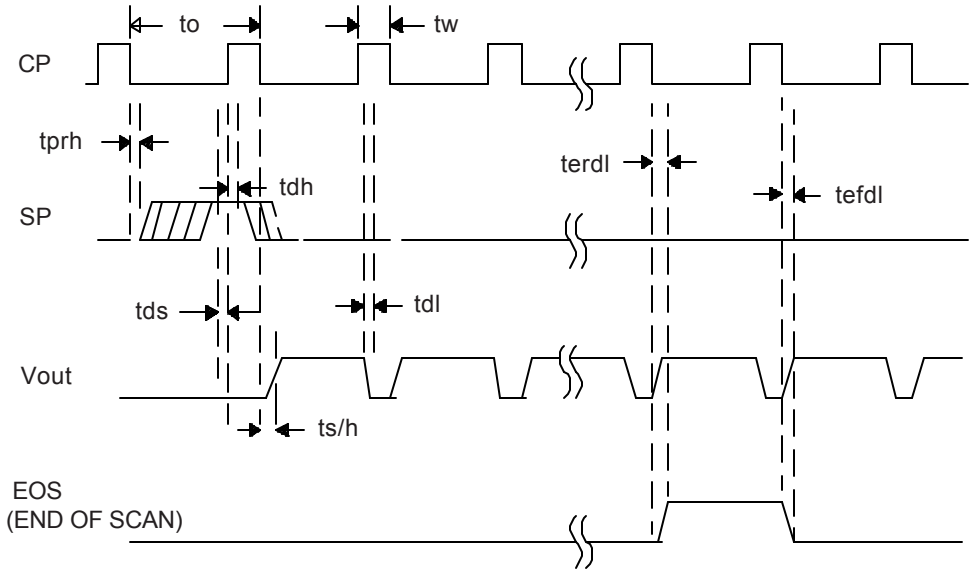


Figure 3. Timing Diagram of the PI3012 A Sensor

Item	Symbol	Minimum	Mean	Maximum	Units
Clock cycle time	to	200		10000	ns
Clock pulse width (1)	tw	50			ns
Clock duty cycle		25	50	75	%
Data setup time	tds	50			ns
Data hold time	tdh	20			ns
Prohibit crossing time (2)	tprh		20		ns
EOS rise delay	terdl		60		ns
EOS fall delay	tefdl		70		ns
Signal delay time (3)	tdl		20		ns
Signal settling time (3)	ts/h		90		ns

1. Clock pulse width varies with frequency, as it was explained foregoing paragraphs. The number given in table is the minimum value regardless of the clock frequency.
2. Prohibit crossing time to insure that two start pulses are not locked into the shift register in any single scan time.
3. Pixel delay times and settling time depend on the output amplifier, which is employed. The numbers, which are given, are measured with an EL2044 amplifier. Note the impulse signal current out of the device is within 10 ns. Hence, the faster the amplifier with a quick settling time and with a lower input capacitance will allow the signal to rise and settle quickly with speeds greater than those given above.

Output Circuits for Video Signal

The circuit, attached on this document as separate page, is a recommended module circuit for operating the sensors. It was also used in the forgoing characterization of the sensor's signal output. See page 7.

Optional Wafer Probe Classification

An optional wafer classification is available for users of the PI3012A devices. To achieve the highest degree of amplitude uniformity, the wafers are sorted and classified. The wafers are rank in accordance to their output amplitudes. Accordingly the users are assured of a greater uniform output from a CIS module when the sensors are selected from the same wafer.