AMI SEMICONDUCTOR

Peripheral Imaging Corporation

PI400M-A4
400DPI CIS Module
Engineering Data Sheet

Key Features

• Light source, lens, and sensor are integrated into a single module

• 15.7 dpm resolution, 216 mm scanning length

• 700µsec/line scanning speed @ 5.0 MHz Clock Rate

• Wide dynamic range

• Analog output

• Yellow-Green light source 575nm

•Compact size ≅14.6 mm x 19.5 mm x 232 mm

• Low power

• Light weight

General Description

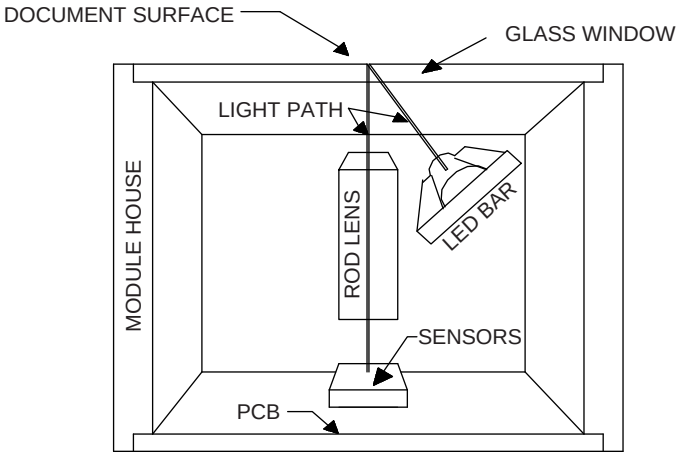
The PI400M-A4 is a CIS module. It is a long contact image sensor, using MOS image sensor technology for high-speed performance and high sensitivity. The PI400M-A4 is suitable for scanning A4 size (216 mm) documents with 15.7 dots per millimeter resolution. Applications include document scanning, mark readers, gaming and office automation equipment.

Functional Description

The PI400M-A4 imaging array consists of 27 sensors that are cascaded to provide 3456 photo-detectors with their associated multiplex switches, and a digital shift register that controls its sequential readout. Mounted in the module is one-to-one graded indexed micro lens array that focuses the scanned documents to image onto its sensing plane.

The on-board amplifier processes the video signal to produce a sequential stream of video at the video output pin of the PI400M-A4 module.

Illumination is by means of an integrated LED light source. All components are housed in a small plastic housing which has a cover glass which acts as the focal point for the object being scanned and protects the imaging array, micro lens assembly, and LED light source from dust. I/O to the module is the 10-pin connector located on one end of the module. See Figure 4, Mechanical Structure on the last page. The cross section of the PI400M-A4 is shown in Figure 1 and the block diagram in Figure 2.



INSIDE PICTORIAL OF MODULE

Figure 1. PI400M-A4 Cross Section

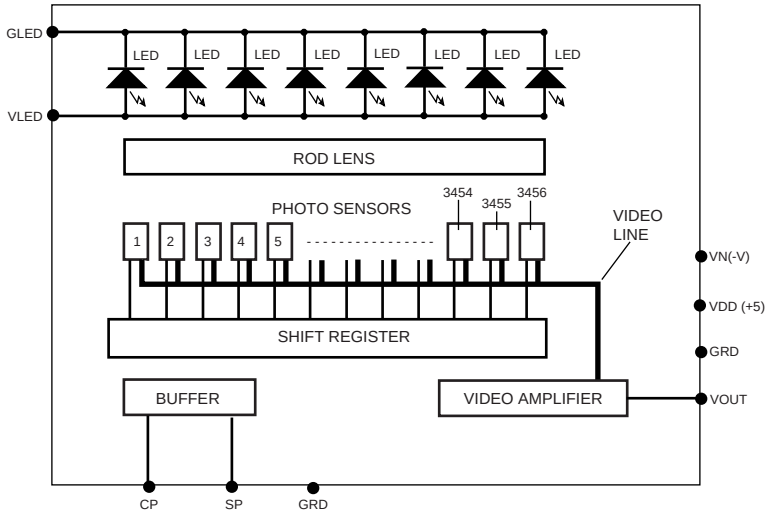


Figure 2. PI400M-A4 module block diagram.
(See Table 1 below for pin configuration)

Pin Number	Symbol	Names and Functions
1	Vout	Analog Video Output
2	Gnd	Ground; 0V
3	Vdd (+5V)	Positive power supply
4	Vn (-5V to –12V)	Negative power supply
5	Gnd	Ground; 0V
6	SP	Shift register start pulse
7	Gnd	Ground; 0V
8	CP	Sampling clock pulse
9	GLED	Ground for the light source; 0V
10	VLED	Supply for the light source

Table 1. Pin configuration

Absolute Maximum Rating:

Parameter	Symbols	Maximum Rating	Units
Power supply voltage	Vdd	10	V
	Idd	60	ma
	Vn	-15	V
	In	10	ma
	VLED	6V	V
	ILED(1)	250	ma
Input clock pulse (high level)	Vih	Vdd – 0.5V	V

Input clock pulse (low level)	Vil	-0.5	V

Table 2. Absolute Maximum Rating

Note (1) LED light source is for current controlled operation. The output video is adjusted to 1.0 Volt maximum, using standard white document - similar to white typing paper.

Environmental Specifications

Operating temperature(1)	Top	0 to 50 (TBD)	^{o}C
Operating humidity(1)	Hop	10 to 85 (TBD)	%
Storage temperature(1)	Tstg	-25 to+75 (TBD)	^{o}C
Storage humidity(1)	Hstg	5 to 95 (TBD)	%

Table 3. Operating and Storage Environment

Note (1) These are standard specifications for the CIS modules. The TBD is to shows that these parameters will be tested later and added to our data sheet.

Electro-Optical Characteristics (25°C)

Parameter	Symbol	Parameter	Units	Note
Number of photo detectors		3456	elements	
Pixel to pixel spacing		63.5	µm	
Line scanning rate	Tint(1)	864	µsec	@ 4.0 MHz clock frequency
Clock frequency(2)	f	4.0	MHz	
Bright output voltage(3)	Video Output	1.0	Volts	
Bright output nonuniformity(4)	Up	<50	%	
Dark nonuniformity(5)	Ud	150	mV	
Dark output voltage(6)	Dark Level	100	mV	
Modulation transfer function(7)	MTF	>30	%	

Table 4. Electro-optical characteristics at 25° C.

Definition:

(1) Tint: line scanning rate or integration time. Tint is determined by the interval between two start pulses (SP).

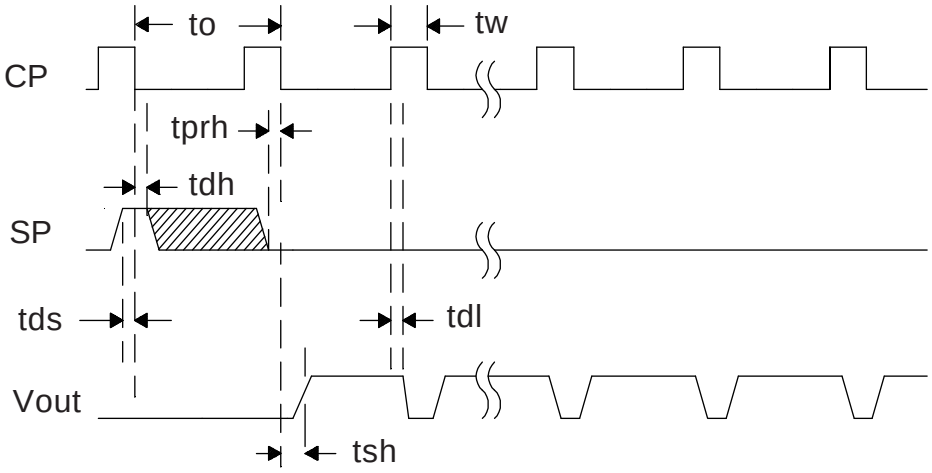
(2) f: main clock frequency also equals the video sampling frequency.
(3) Video output level is controlled with LED current source.
(4) Up = {[Vp(max) –Vp(min)]/Vp(max)}x100%
Where VP(max) = maximum peak pixel and VP(min) = minimum pixel.
(5) Ud = Vdmax – Vdmin
Vdmin is the minimum output voltage with LED off.
Vdmax: maximum output voltage with LED off
(6) This level is measured from the reset level that is located between the pixels, during the pixel reset duration. The reset level is at ground, 0V. It can be adjusted with offset potentiometer located on the module.
(7) MTF = [(Vp(n) – Vp(n+1)] / (Vp(n)+ Vp(n+1)] x 100 [%]
Vp(n): n^{th} maximum output pixel from a 8.0 lp/mm target.
$V(n+1)^{th}$: $(n+1)^{th}$ minimum output pixel from a 8.0 lp/mm target.
(8) lp / mm: line pair per mm

Recommended Operating Conditions (25 C)

Item	Symbol	Min	Typical	Max	Units
Power Supply	Vdd	4.5	5.0	5.5	V
	Vn.	-4.5	-5	-12	V
	Idd				ma
	ILED			250	ma
	VLED		+5.0		V
Input voltage at digital high	Vih	Vdd-1.0	Vdd-.5	Vdd	V
Input voltage at digital low	Vil	0		0.8	V
Clock frequency	f	0.5	4.0	5.0	MHz
Clock pulse high duty cycle			25		%
Clock pulse high duration			62.5		ns
Integration time	Tint		864		µs
Operating temperature(1)	Top		25	50	^{0}C

Table 5. Recommended Operating Condition (25 ^{0}C)
Note (1) see the note under the Table for Operating and Storage Environment.

Switching Characteristics (25°C)



MODULE TIMING DIAGRAM

Figure 3

The Switching Characteristics (25°C) for the I/O clocks are shown in the diagram below. For the timing symbol definitions see the following table below the timing diagram.

Item	Symbol	Min.	Typical	Max.	Units
Clock cycle time	to	0.20		2.0	µs
Clock pulse width	tw	50			ns
Clock duty cycle		25		75	%
Prohibit crossing time of Start Pulse(1)	tprh	0			ns
Data setup time	tds	20			ns
Data hold time	tdh	0			ns
Signal delay time	tdl	20			ns
Signal settling time	tsh	100			ns

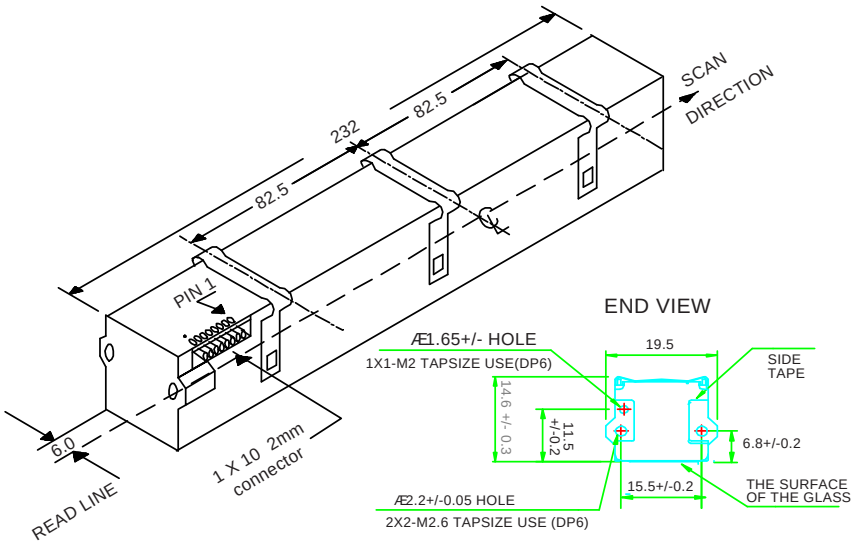
Table 6. Timing Symbol's Definition and Timing Values.

Note:

(1) "Prohibit crossing of start pulse" is to indicate that the start pulse should not be active high between any two consecutive high going clock pulse or two consecutive low going clock pulses. See the timing diagram. Only one high going clock under the active high start pulse initiates the internal shift register, and it must not be active over two high going clocks. All low going clock pulses will not initiate the shift register, but to ensure that the start pulse will not be actively high during two consecutive high going clocks, the circuit should be design to keep the start pulse active only for one low going clock cycle.

Mechanical Structure of the Module

For PI400M-A4 Module's dimensions see the Figure 4 Mechanical Structure.



MECHANICAL STRUCTURE
FIGURE 4