AMI SEMICONDUCTOR

Peripheral Imaging Corporation

PI404MC-A8
400DPI CIS Module
Engineering Data Sheet

Key Features

• Light source, lens, and sensor are integrated into a single module

• 15.7 dpm resolution, 57 mm scanning length

• 1.8 msec/line scanning speed @ 500KHz clock rate

• Wide dynamic range

• Analog output

• Yellow-Green light source 570nm

• Compact size ≅ 13 mm x 19 mm x 70 mm

• Low power

• Light weight

General Description

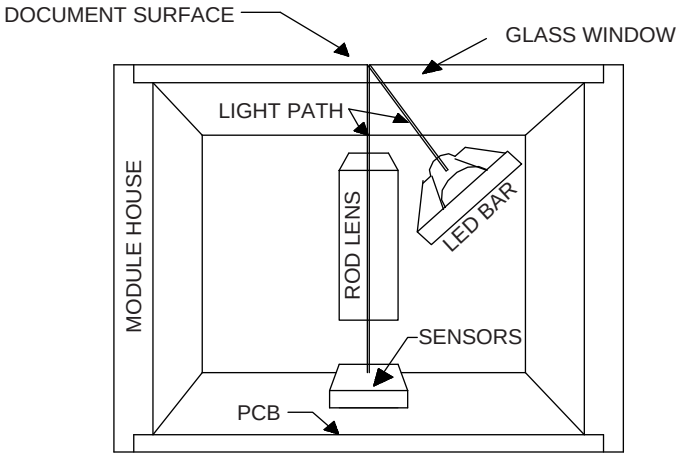
The PI404MC-A8 is a CIS module. It is a long contact image chips, using MOS image sensor technology for high-speed performance and high sensitivity. The PI404MC-A8 is suitable for scanning A8 size (57 mm) documents with 15.7 dots per millimeter resolution. Applications include document scanning, mark readers, gaming and office automation equipment.

Functional Description

The PI404MC-A8 imaging array consists of 7 sensors that are cascaded to provide 896 photo-detectors with their associated multiplex switches, and a digital shift register that controls its sequential readout. Mounted in the module is one-to-one graded indexed micro lens array that focuses the scanned documents to image onto its sensing plane.

The on-board amplifier processes the video signal to produce a sequential stream of video at the video output pin of the PI404MC-A8 module.

Illumination is by means of an integrated LED light source. All components are housed in a small plastic housing which has a cover glass which acts as the focal point for the object being scanned and protects the imaging array, micro lens assembly, and LED light source from dust. I/O to the module is the 10-pin connector located on one end of the module. See Figure 4, Mechanical Structure on the last page. The cross section of the PI404MC-A8 is shown in Figure 1 and the block diagram in Figure 2.



INSIDE PICTORIAL OF MODULE

Figure 1. PI404MC-A8 Cross Section

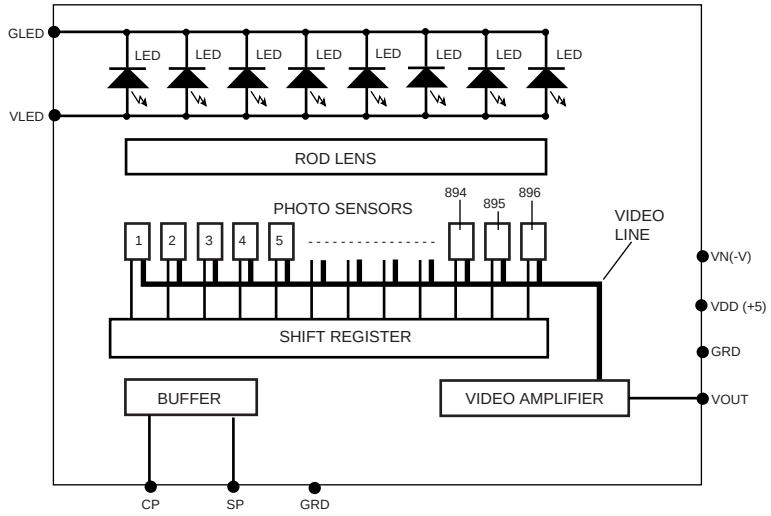


Figure 2. PI404MC-A8 module block diagram.
(See Table 1 below for pin configuration)

Pin Number	Symbol	Names and Functions
1	Vout	Analog Video Output
2	Gnd	Ground; 0V
3	Vdd (+5V)	Positive power supply
4	Vn (-5V to –12V)	Negative power supply
5	Gnd	Ground; 0V
6	SP	Shift register start pulse
7	Gnd	Ground; 0V
8	CP	Sampling clock pulse
9	GLED	Ground for the light source; 0V
10	VLED	Supply for the light source

Table 1. Pin configuration

Absolute Maximum Rating:

Parameter	Symbols	Maximum Rating	Units
Power supply voltage	Vdd	6	V
	Idd	40	ma
	Vn	-15	V
	In	10	ma
	VLED	5.5V	V
	ILED	300	ma
Input clock pulse (high level)	Vih	Vdd – 0.5V	V

Input clock pulse (low level)	Vil	-0.5	V

Table 2. Absolute Maximum Rating

Environmental Specifications

Operating temperature (1)	Top	0 to 50	^{0}C
Operating humidity (1)	Hop	10 to 90	%
Storage temperature (1)	Tstg	-20 to+75	^{0}C
Storage humidity (1)	Hstg	10 to 90	%

Table 3. Operating and Storage Environment
Note (1) These are standard specifications for the CIS modules.

Electro-Optical Characteristics (25℃)

Parameter	Symbol	Parameter	Units	Note
Number of photo detectors		896	elements	
Pixel-to-pixel spacing		63.5	μm	
Line scanning rate	Tint (1)	2.92	msec	@ 307 KHz clock frequency
Clock frequency (2)	f	307	KHz	
Bright output voltage (3)	Video Output	2.0 +/-0.2	Volt	
Bright output nonuniformity (4)	Up	+/- 30	%	
Dark nonuniformity (5)	Ud	<200	mV	
Dark output voltage (6)	Dark Level (DL)	-200<DL<200	mV	
Modulation transfer function (7)	MTF	>45	%	

Table 4. Electro-optical characteristics at 25° C.

Definition:
(1) Tint: line scanning rate or integration time. Tint is determined by the interval between two start pulses (SP).
(2) f: main clock frequency also equals the video sampling frequency.
(3) Video output level is controlled with an adjustment as well as Integration time
(4) Up = {[Vp(max) –Vp(min)]/Vp(max)}x100%
Where VP(max) = maximum peak pixel and VP(min) = minimum pixel.
(5) Ud = Vdmax – Vdmin

Vdmin is the minimum output voltage with LED off.
Vdmax is maximum output voltage with LED off
(6) This level is measured from the reset level that is located between the pixels, during the pixel reset duration. The reset level is at ground, 0V. It can be adjusted with offset potentiometer located on the module.
(7) MTF = [(Vp(n) – Vp(n+1)] / (Vp(n)+ Vp(n+1)] x 100 [%]
Vp(n): n^{th} maximum output pixel from a 8.0 lp/mm target.
V(n+1): $(n+1)^{th}$ minimum output pixel from a 8.0 lp/mm target.
(8) lp / mm: line pair per mm

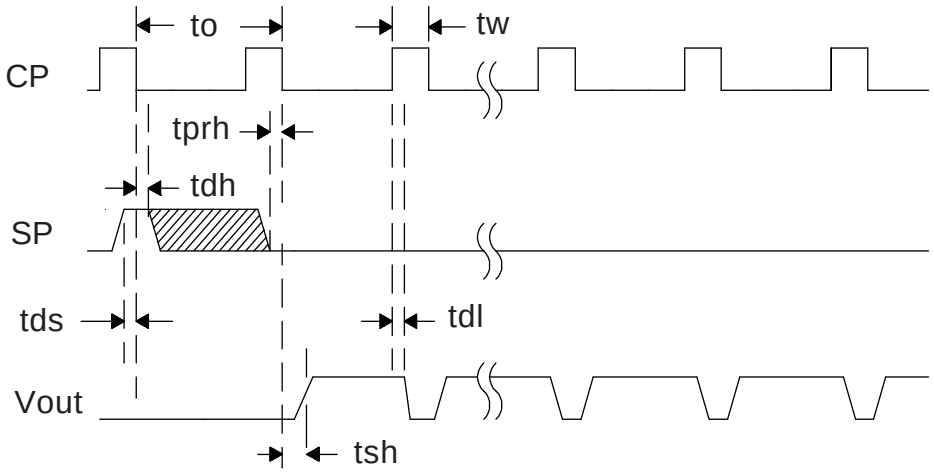
Recommended Operating Conditions (25°C)

Item	Symbol	Min	Typical	Max	Units
Power Supply	Vdd	4.5	5.0	5.5	V
	Vn.	-12	-5	-4.0	V
	Idd		30		ma
	In		8		ma
	ILED		250	300	ma
	VLED		+5		V
Input voltage at digital high	Vih	Vdd-1.0	Vdd-.5	Vdd	V
Input voltage at digital low	Vil	0		0.6	V
Clock frequency	f	0	0.30	1.0	MHz
Clock pulse high duty cycle			25		%
Clock pulse high duration			0.8		us
Integration time	Tint		3.0		ms
Operating temperature(1)	Top		25	50	^{o}C

Table 5. Recommended Operating Condition (25 ^{o}C)
Note (1) see the note under the Table for Operating and Storage Environment.

Switching Characteristics (25℃)

The Switching Characteristics (25℃) for the I/O clocks are shown in the diagram below. For the timing symbol definitions see the following table below the timing diagram.



MODULE TIMING DIAGRAM
FIGURE 3

Item	Symbol	Min.	Typical	Max.	Units
Clock cycle time	to	1.0		4.0	μs
Clock pulse width	tw	250			ns
Clock duty cycle		25		75	%
Prohibit crossing time of Start Pulse(1)	tprh	0			ns
Data setup time	tds	20			ns
Data hold time	tdh	0			ns
Signal delay time	tdl	20			ns
Signal settling time	tsh	100			ns

Table 6. Timing Symbol's Definition and Timing Values.

Note:

(1) "Prohibit crossing of start pulse" is to indicate that the start pulse should not be active high between any two consecutive high going clock pulse or two consecutive low going clock pulses. See the timing diagram. Only one high going clock under the active high start pulse initiates the internal shift register, and it must not be active over two high going clocks. All low going clock pulses will not initiate the shift register, but to ensure that the start pulse will not be actively high during two consecutive high going clocks, the circuit should be design to keep the start pulse active only for one low going clock cycle.

Mechanical Structure of the Module

An isometric overview drawing of the PI404MC-A8 Module's housing is shown in the Figure 4. Housing Outline. These modules is supplied with plastic end caps, how ever, for compactness in the installation of these module the end caps can be removed, providing internal to the housing the modules are kept dark with no external light leakage.

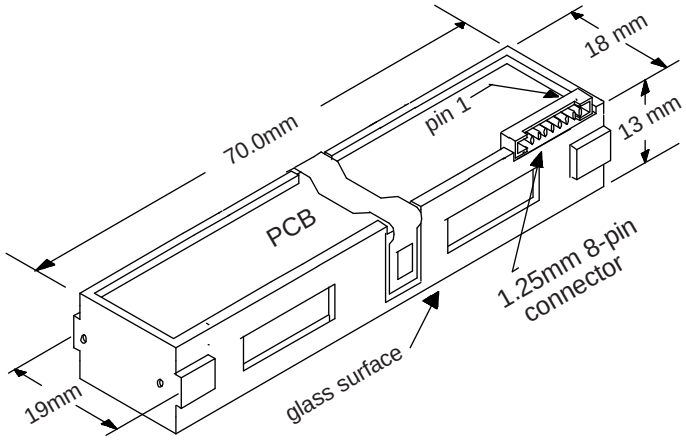


Figure 4. PI404MC-A8 Module Housing Module

Although the standard modules comes with connector pins extruding to the sides as shown, a straight pinned socket can be installed into the PCB with its pins extruding directly up from its mount PCB. However, it must be requested upon ordering of the modules, otherwise the standard configuration will be shipped.

For module design-in, a detail drawing is available upon request.