



## PI6C3Q991, PI6C3Q993

### 3.3V Programmable Skew PLL Clock Driver *SuperClock*<sup>®</sup>

#### Features

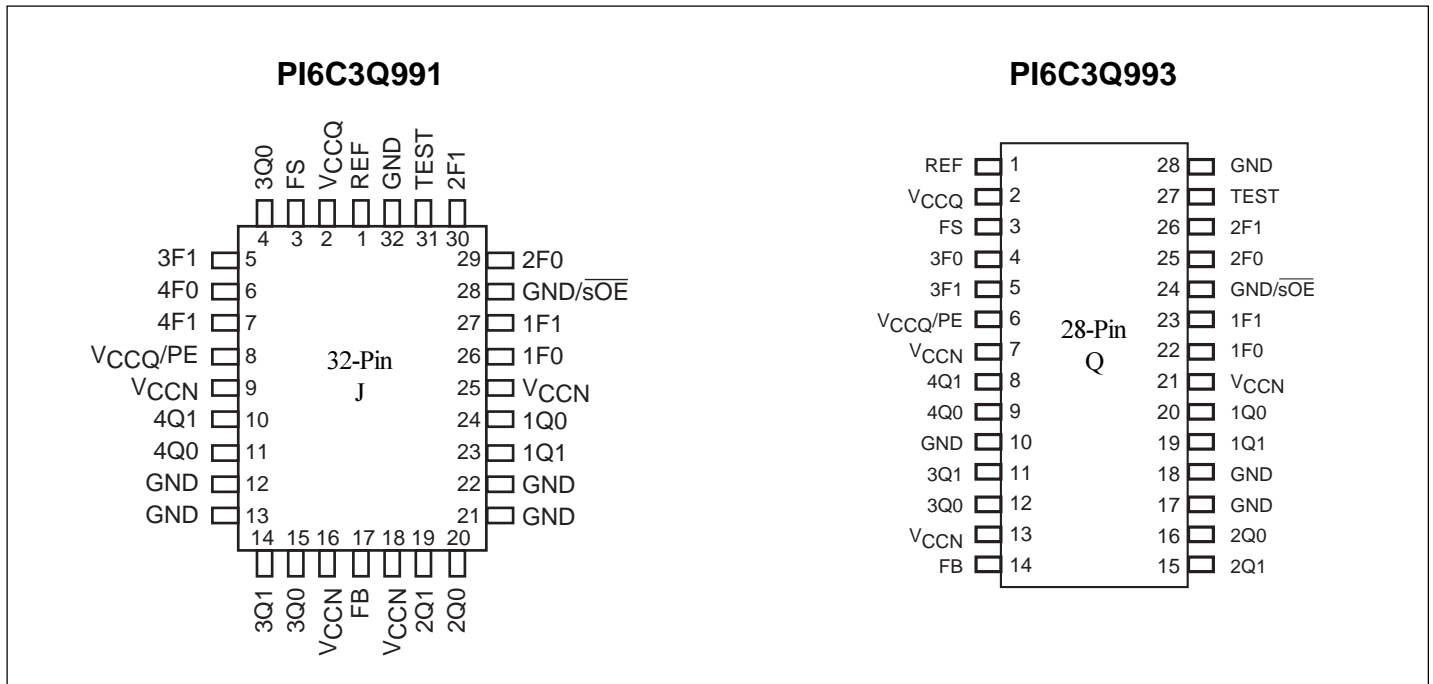
- PI6C3Q99X family provides following products:  
PI6C3Q991: 32-pin PLCC version  
PI6C3Q993: 28-pin QSOP version
- Inputs are 5V I/O Tolerant
- 4 pairs of programmable skew outputs
- Low skew: 200ps same pair; 250ps all outputs
- Selectable positive or negative edge synchronization:  
Excellent for DSP applications
- Synchronous output enable
- Output frequency: 3.75 MHz to 85 MHz
- 2x, 4x, 1/2, and 1/4 outputs
- 3 skew grades:
- 3-level inputs for skew and PLL range control
- PLL bypass for DC testing
- External feedback, internal loop filter
- 12mA balanced drive outputs
- Low Jitter: <200ps peak-to-peak
- Industrial temperature range
- Pin-to-pin compatible with IDT QS5V991 and QS5V993
- Available in 32-pin PLCC and 28-pin QSOP

#### Description

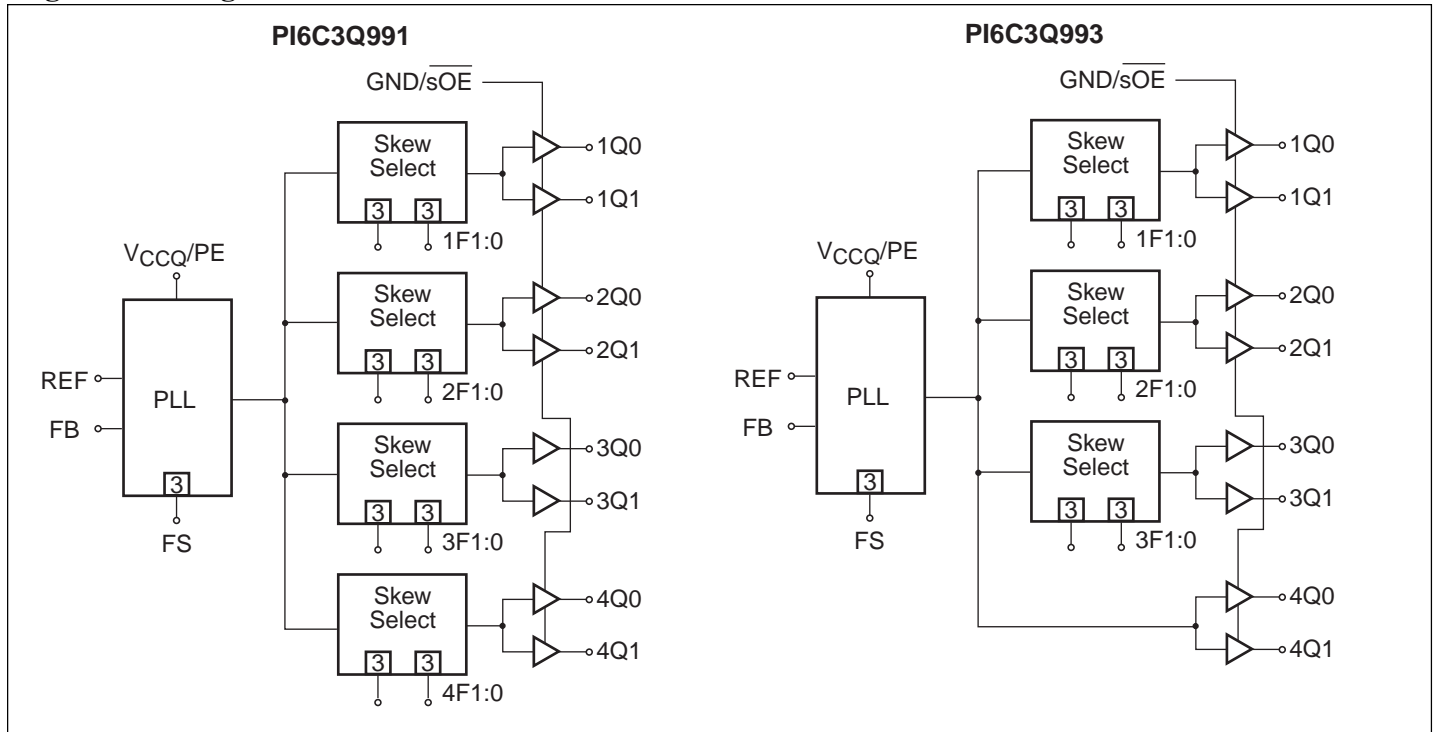
The PI6C3Q99X family is a high fanout 3.3V PLL-based clock driver intended for high performance computing and data-communications applications. A key feature of the programmable skew is the ability of outputs to lead or lag the REF input signal. The PI6C3Q991 has 8 programmable skew outputs in 4 banks of 2, while the PI6C3Q993 has 6 programmable skew outputs and 2 zero skew outputs. Skew is controlled by 3-level input signals that may be hard-wired to appropriate HIGH-MID-LOW levels.

When the GND/ $\overline{sOE}$  pin is held low, all the outputs are synchronously enabled. However, if GND/ $\overline{sOE}$  is held high, all the outputs except 3Q0 and 3Q1 are synchronously disabled. Furthermore, when the V<sub>CCQ</sub>/PE is held high, all the outputs are synchronized with the positive edge of the REF clock input. When V<sub>CCQ</sub>/PE is held low, all the outputs are synchronized with the negative edge of REF. Both devices have LVTTTL outputs with 12mA balanced drive outputs.

#### Pin Configurations



### Logic Block Diagrams



### Pin Descriptions

Pin Name	Type	Functional Description
REF	IN	Reference Clock input
FB	IN	Feedback Input
TEST <sup>(1)</sup>	IN	When MID or HIGH, disables PLL (except for conditions of Note 1). REF goes to all outputs. Skew selections (see table 3) remain in effect. Set LOW for normal operation.
GND/ $\overline{\text{sOE}}$ <sup>(1)</sup>	IN	Synchronous Output Enable. When HIGH, it stops clock outputs (except 3Q0 and 3Q1) in a LOW state - 3Q0 or 3Q1 may be used as the feedback signal to maintain phase lock. When TEST is held at MID level and GND/ $\overline{\text{sOE}}$ is HIGH, the nF [1:0] pins act as output disable controls for individual banks when nF [1:0] = LL. Set GND/ $\overline{\text{sOE}}$ LOW for normal operation.
VCCQ/PE	IN	Selectable positive or negative edge control. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock.
nF [1:0]	IN	3-level inputs for selecting 1 of 9 skew taps or frequency range.
FS	IN	Selects appropriate oscillator circuit based on anticipated frequency range. See table 2
nQ [1:0]	OUT	4 output banks of 2 outputs, with programmable skew. On the PI6C3Q993 4Q1:0 are fixed zero skew outputs.
VCCN	PWR	Power supply for output buffers
VCCQ	PWR	Power supply for phase locked loop and other internal circuitry
GND	PWR	Ground

**Note:**

1. When TEST = MID and GND/ $\overline{\text{sOE}}$  = HIGH, PLL remains active with nF[1:0] = LL functioning as an output disable control for individual output banks. Skew selections (see Table 3) remain in effect unless nF[1:0] = LL.

### Programmable Skew

Output skew with respect to the REF input is adjustable to compensate for PCB trace delays, backplane propagation delays or to accommodate requirements for special timing relationships between clocked components. Skew is selectable as a multiple of a time unit  $t_U$  which is of the order of a nanosecond (see Table 2). There are 9 skew configurations available for each output pair. These configurations are chosen by the nF1:0 control pins. In order to minimize the number of control pins, 3-level inputs (HIGH-MID-LOW) are used, they are intended for but not restricted to hard-wiring. Undriven 3-level inputs default to the MID level. Where programmable skew is not a requirement, the control pins can be left open for the zero skew default setting. The Skew Selection Table (Table 3) shows how to select specific skew taps by using the nF1:0 control pins.

### External Feedback

By providing external feedback, the PI6C3Q99X family gives users flexibility with regard to skew adjustment. The FB signal is compared with the input REF signal at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly. An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

**Table 2. PLL Programmable Skew Range and Resolution Table**

	FS = LOW	FS = MID	FS = HIGH	Comments
Timing unit calculation ( $t_U$ )	$1/(44 \times F_{NOM})$	$1/(26 \times F_{NOM})$	$1/(16 \times F_{NOM})$	
VCO frequency range ( $F_{NOM}$ ) <sup>(1,2)</sup>	15 to 35 MHz	25 to 60 MHz	40 to 85 MHz	
Skew adjustment range <sup>(3)</sup> Max. adjustment	$\pm 9.09\text{ns}$ $\pm 49^\circ$ $\pm 14\%$	$\pm 9.23\text{ns}$ $\pm 83^\circ$ $\pm 23\%$	$\pm 9.38\text{ns}$ $\pm 135^\circ$ $\pm 37\%$	ns Phase degrees % of cycle time
Example 1, $F_{NOM} = 15$ MHz	$t_U = 1.52\text{ns}$			
Example 2, $F_{NOM} = 25$ MHz	$t_U = 0.91\text{ns}$	$t_U = 1.54\text{ns}$		
Example 3, $F_{NOM} = 30$ MHz	$t_U = 0.76\text{ns}$	$t_U = 1.28\text{ns}$		
Example 4, $F_{NOM} = 40$ MHz		$t_U = 0.96\text{ns}$	$t_U = 1.56\text{ns}$	
Example 5, $F_{NOM} = 50$ MHz		$t_U = 0.77\text{ns}$	$t_U = 1.25\text{ns}$	
Example 6, $F_{NOM} = 80$ MHz			$t_U = 0.78\text{ns}$	

**Notes:**

1. The device may be operated outside recommended frequency ranges without damage, but functional operation is not guaranteed. Selecting the appropriate FS value based on input frequency range allows the PLL to operate in its ‘sweet spot’ where jitter is lowest.
2. The level to be set on FS is determined by the nominal operating frequency of the VCO and Time Unit Generator. The VCO frequency always appears at 1Q1:0, 2Q1:0, and the higher outputs when they are operated in their undivided modes. The frequency appearing at the REF and FB inputs will be the same as the VCO when the output connected to FB is undivided. The frequency of the REF and FB inputs will be 1/2 or 1/4 the VCO frequency when the part is configured for a frequency multiplication by using a divided output as the FB input.
3. Skew adjustment range assumes that a zero skew output is used for feedback. If a skewed Q output is used for feedback, then adjustment range will be greater. For example if a  $4t_U$  skewed output is used for feedback, all other outputs will be skewed  $-4t_U$  in addition to whatever skew value is programmed for those outputs. ‘Max adjustment’ range applies to output pairs 3 and 4 where  $\pm 6 t_U$  skew adjustment is possible and at the lowest  $F_{NOM}$  value.



**Table 6. DC Characteristics Over Operating Range**

Symbol	Parameter	Test Condition	Min.	Max.	Units
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Logic HIGH (REF, FB inputs only)	2.0		V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Logic LOW (REF, FB inputs only)		0.8	
V <sub>IHH</sub>	Input HIGH Voltage <sup>(1)</sup>	3-Level Inputs Only	V <sub>CC</sub> - 0.6		
V <sub>IMM</sub>	Input MID Voltage <sup>(1)</sup>	3-Level Inputs Only	V <sub>CC</sub> /2 - 0.3	V <sub>CC</sub> /2 + 0.3	
V <sub>ILL</sub>	Input LOW Voltage <sup>(1)</sup>	3-Level Inputs Only		0.6	
I <sub>IN</sub>	Input Leakage Current (REF, FB inputs only)	V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>CC</sub> = Max.		5	μA
I <sub>3</sub>	3-Level Input DC Current (TEST, FS, nF1:0)	V <sub>IN</sub> = V <sub>CC</sub> HIGH Level V <sub>IN</sub> = V <sub>CC</sub> /2 MID Level V <sub>IN</sub> = GND LOW Level		200 50 200	
I <sub>PU</sub>	Input Pull-Up Current (V <sub>CCQ</sub> /PE)	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND		100	
I <sub>PD</sub>	Input Pull-Down Current (GND/sOE)	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>		100	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -12mA	2.2		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 12mA		0.55	

**Note:**

1. These inputs are normally wired to V<sub>CC</sub>, GND, or unconnected. Internal termination resistors bias unconnected inputs to V<sub>CC</sub>/2. If these inputs are switched, the function and timing of the outputs may glitched, and the PLL may require an additional t<sub>LOCK</sub> time before all datasheet limits are achieved.

**Table 7. Power Supply Characteristics**

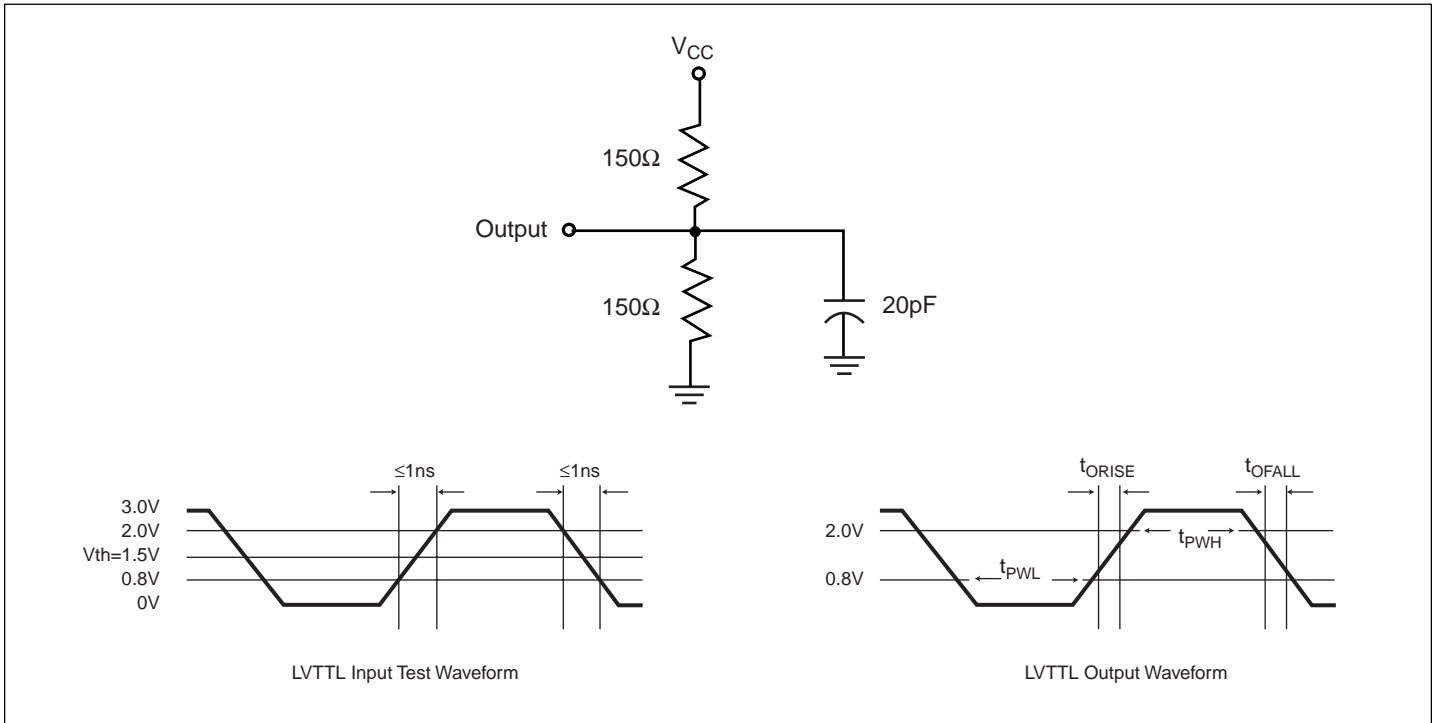
Symbol	Parameter	Test Condition	Typ.	Max.	Units
I <sub>CCQ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max., TEST = Mid., REF = LOW, GND/sOE = LOW, All outputs unloaded	8.0	15	mA
ΔI <sub>CC</sub>	Power Supply Current per Input HIGH <sup>(1)</sup>	V <sub>CC</sub> = Max., V <sub>IN</sub> = 3.0V	1.0	30	μA
I <sub>CCD</sub>	Dynamic Power Supply Current per Output <sup>(1)</sup>	V <sub>CC</sub> = Max., C <sub>L</sub> = 0pF	55	90	μA/MHz
I <sub>C</sub>	Total Power Supply Current <sup>(1)</sup>	V <sub>CC</sub> = 3.3V, F <sub>REF</sub> = 20 MHz, C <sub>L</sub> = 160pF <sup>(2)</sup>	29		mA
I <sub>C</sub>	Total Power Supply Current <sup>(1)</sup>	V <sub>CC</sub> = 3.3V, F <sub>REF</sub> = 33 MHz, C <sub>L</sub> = 160pF <sup>(2)</sup>	42		
I <sub>C</sub>	Total Power Supply Current <sup>(1)</sup>	V <sub>CC</sub> = 3.3V, F <sub>REF</sub> = 66 MHz, C <sub>L</sub> = 160pF <sup>(2)</sup>	76		

**Notes:**

1. Guaranteed by characterization but not production tested.
2. For 8 outputs each loaded with 20pF.

**Table 8. Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{IN} = 0\text{V}$ )

	QSOP		PLCC		Units
	Typ.	Max.	Typ.	Max.	
$C_{IN}$	4	6	5	7	pF


**AC Test Loads and Waveforms**

**Table 9. Switching Characteristics Over Operating Range**

Symbol	Description	PI6C3Q991-2 PI6C3Q993-2			PI6C3Q991-5 PI6C3Q993-5			PI6C3Q991 PI6C3Q993			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
F <sub>NOM</sub>	VCO frequency range	see Table 2			see Table 2			see Table 2			
t <sub>RPWH</sub>	REF pulse width HIGH <sup>(11)</sup>	3.0			3.0			3.0			ns
t <sub>RPWL</sub>	REF pulse width LOW <sup>(11)</sup>	3.0			3.0			3.0			
t <sub>U</sub>	Programmable skew time unit	see Table 3			see Table 3			see Table 3			
t <sub>SKEWPR</sub>	Zero output matched-pair skew (xQ0, xQ1) <sup>(1,2,3)</sup>		0.05	0.20		0.1	0.25		0.1	0.25	ns
t <sub>SKEW0</sub>	Zero output skew (all outputs) C <sub>L</sub> = 0pF <sup>(1,4)</sup>		0.1	0.25		0.25	0.5		0.3	0.75	
t <sub>SKEW1</sub>	Output skew (rise-rise, fall-fall, same class outputs) <sup>(1,5)</sup>		0.25	0.50		0.6	0.7		0.6	1.0	
t <sub>SKEW2</sub>	Output skew (rise-fall, nominal-inverted, divided-divided) <sup>(1,5)</sup>		0.30	1.2		0.5	1.2		1.0	1.5	
t <sub>SKEW3</sub>	Output skew (rise-rise, fall-fall, different class outputs) <sup>(1,5)</sup>		0.25	0.50		0.5	0.7		0.7	1.2	
t <sub>SKEW4</sub>	Output skew (rise-fall, nominal-divided, divided-inverted) <sup>(1,5)</sup>		0.50	0.90		0.5	1.0		1.2	1.7	
t <sub>DEV</sub>	Device-to-device skew <sup>(1,2,6)</sup>			0.75			1.25			1.65	
t <sub>PD</sub>	REF input to FB propagation delay <sup>(1,8)</sup>	-0.25	0	0.25	-0.5	0	0.5	-0.7	0	0.7	
t <sub>ODCV</sub>	Output duty cycle variation from 50% <sup>(1)</sup>	-1.2	0	1.2	-1.2	0	1.2	-1.2	0	1.2	
t <sub>PWH</sub>	Output HIGH time deviation from 50% <sup>(1,9)</sup>			2.0			2.5			3.0	
t <sub>PWL</sub>	Output LOW time deviation from 50% <sup>(1,10)</sup>			2.5			3.0			3.5	
t <sub>ORISE</sub>	Output rise time <sup>(1)</sup>	0.15	1.0	1.8	0.15	1.0	1.8	0.15	1.5	2.5	
t <sub>OFALL</sub>	Output fall time <sup>(1)</sup>	0.15	1.0	1.8	0.15	1.0	1.8	0.15	1.5	2.5	
t <sub>LOCK</sub>	PLL lock time <sup>(1,7)</sup>			0.5			0.5			0.5	ms
t <sub>JR</sub>	Cycle-to-cycle output jitter <sup>(1)</sup>	RMS				25		40		40	ps
		Peak-to-peak				200		200		200	

**Notes:**

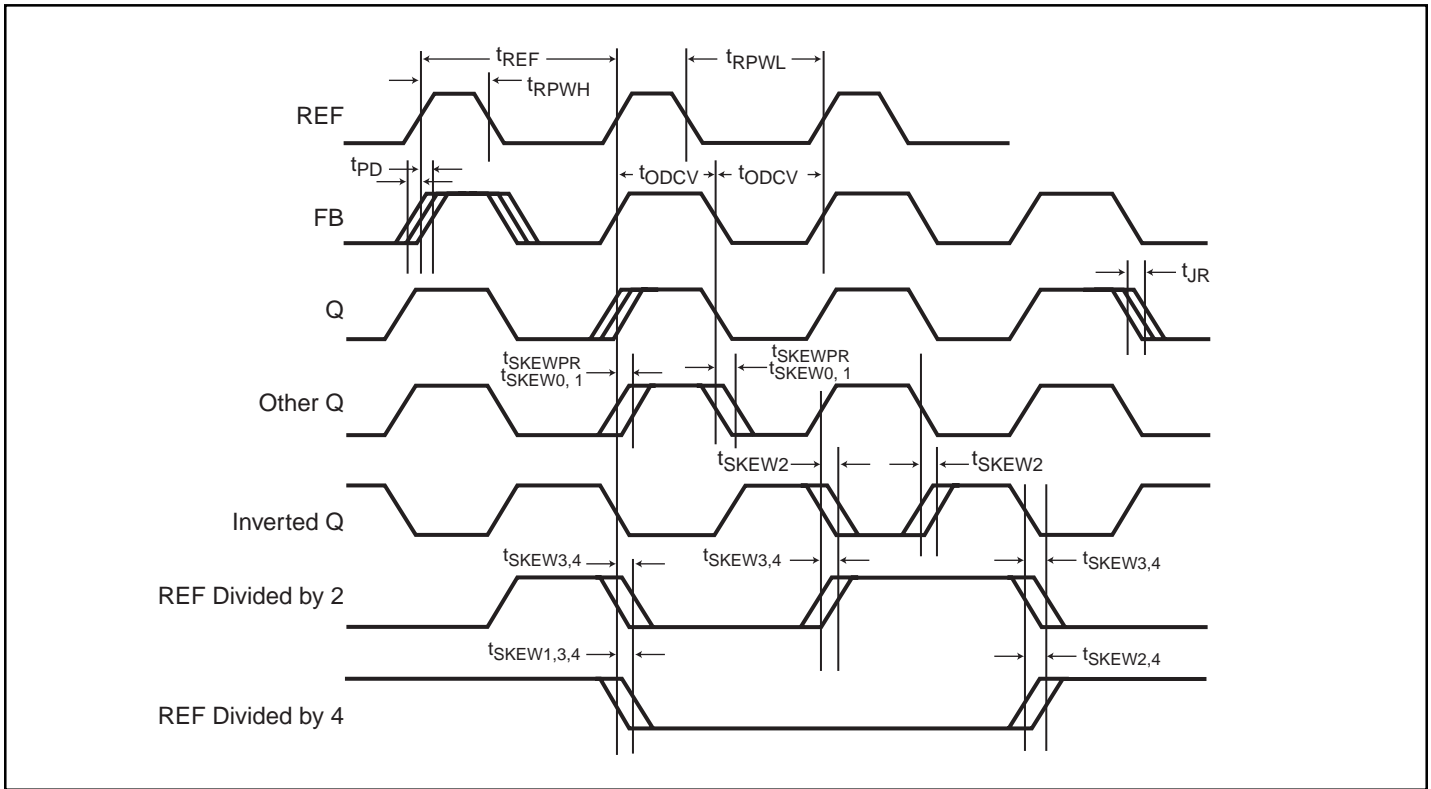
1. All timing tolerances apply for F<sub>NOM</sub> ≥ 25MHz. Guaranteed by design and characterization, not subject to 100% production testing.
2. Skew is the time between the earliest and the latest output transition among all outputs for which the same t<sub>U</sub> delay has been selected when all are loaded with the specified load.
3. t<sub>SKEWPR</sub> is the skew between a pair of outputs (xQ0 and xQ1) when all eight outputs are selected for 0t<sub>U</sub>.
4. t<sub>SKEW0</sub> is the skew between outputs when they are selected for 0t<sub>U</sub>.
5. There are 3 classes of outputs: Nominal (multiple of t<sub>U</sub> delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
6. t<sub>DEV</sub> is the output-to-output skew between any two devices operating under the same conditions (V<sub>CC</sub>, ambient temperature, air flow, etc.)
7. t<sub>LOCK</sub> is the time that is required before synchronization is achieved. This specification is valid only after V<sub>CC</sub> is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t<sub>PD</sub> is within specified limits.
8. t<sub>PD</sub> is measured with REF input rise and fall times (from 0.8V to 2.0V) of 1.0ns.
9. Measured at 2.0V.
10. Measured at 0.8V.
11. Refer to Table 12 for more detail.

**Table 12. Input Timing Requirements**

Symbol	Description	Min.	Max.	Units
$t_R, t_F$	Maximum input rise and fall times, 0.8V to 2.0V		10	ns/V
$t_{PWC}$	Input clock pulse, HIGH or LOW	3		ns
$D_H$	Input duty cycle	10	90	%

**Notes:**

1. Input timing requirements are guaranteed by design but not tested. Where pulse width implied by  $D_H$  is less than  $t_{PWC}$  limit,  $t_{PWC}$  limit applies.



**AC Timing Diagram**

**Notes:**

$V_{CCQ}/PE$ : The AC timing diagram above applies to  $V_{CCQ}/PE=V_{CC}$ . For  $V_{CCQ}/PE=GND$ , the negative edge of FB aligns with the negative edge of REF, divided outputs change on the negative edge of REF, and the positive edges of the divide-by-2 and the divide-by-4 signals align.

Skew: The time between the earliest and the latest output transition among all outputs for which the same  $t_U$  delay has been selected when all are loaded with 20pF and terminated with 75Ohm to  $V_{CC}/2$ .

$t_{SKEWPR}$ : The skew between a pair of outputs (xQ0 and xQ1) when all eight outputs are selected for  $0t_U$ .

$t_{SKEW0}$ : The skew between outputs when they are selected for  $0t_U$ .

$t_{DEV}$ : The output-to-output skew between any two devices operating under the same conditions ( $V_{CC}$ , ambient temperature, air flow, etc.)

$t_{ODCV}$ : The deviation of the output from a 50% duty cycle. Output pulse width variations are included in  $t_{SKEW2}$  and  $t_{SKEW4}$  specifications.

$t_{LOCK}$ : The time that is required before synchronization is achieved. This specification is valid only after  $V_{CC}$  is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until  $t_{PD}$  is within specified limits.

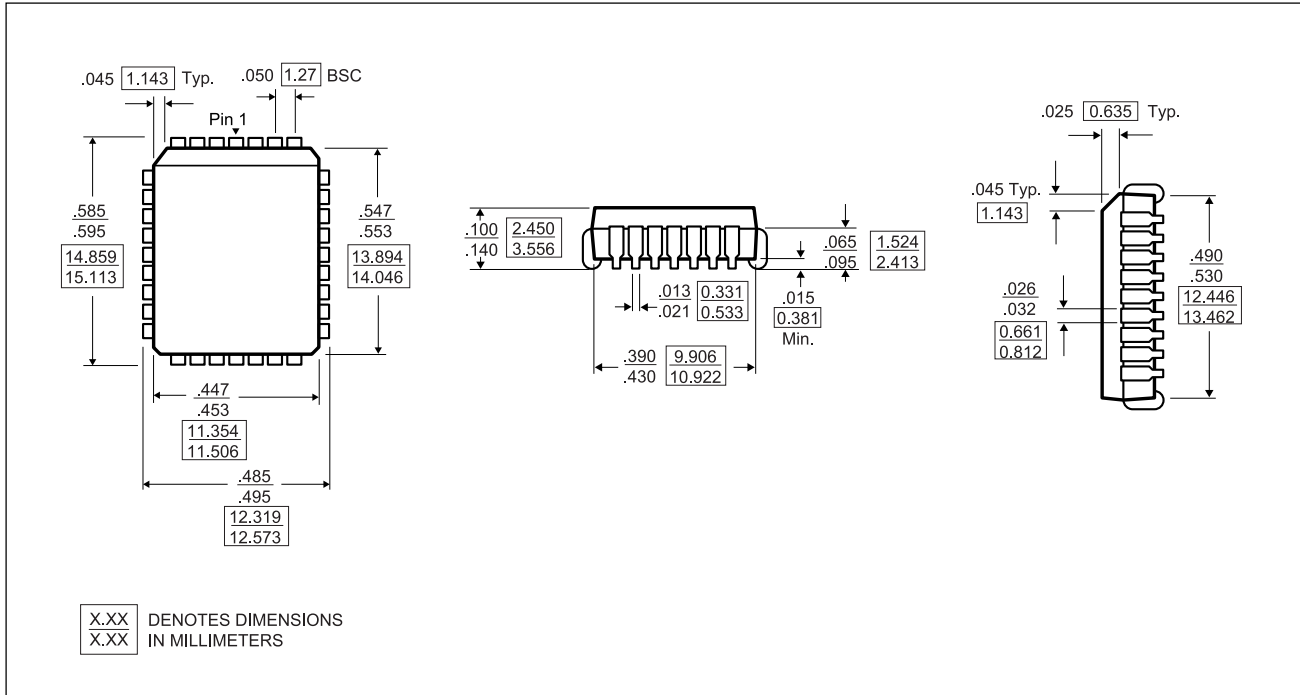
$t_{PWH}$  is measured at 2.0V.

$t_{PWL}$  is measured at 0.8V.

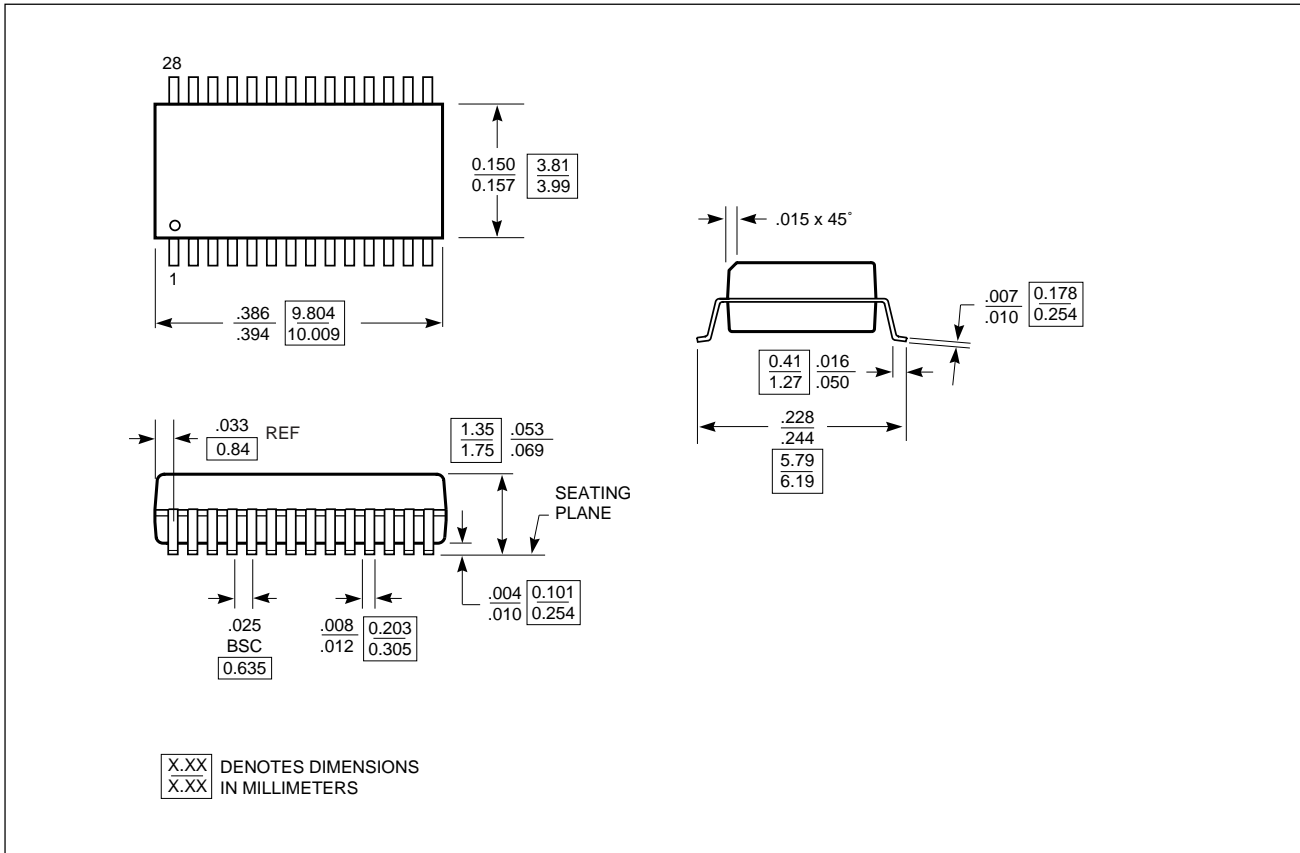
$t_{ORISE}$  and  $t_{OFALL}$  are measured between 0.8V and 2.0V.



### 32-Pin PLCC Package Diagram



### 28-Pin QSOP Package Diagram





### Ordering Information

Ordering Code	Package Code	Package Type	Operating Range
PI6C3Q991J	J32	32-Pin PLCC	Commercial
PI6C3Q991-2J	J32	32-Pin PLCC	
PI6C3Q991-5J	J32	32-Pin PLCC	
PI6C3Q991-IJ	J32	32-Pin PLCC	Industrial
PI6C3Q991-5IJ	J32	32-Pin PLCC	
PI6C3Q993Q	Q28	28-Pin QSOP	Commercial
PI6C3Q993-2Q	Q28	28-Pin QSOP	
PI6C3Q993-5Q	Q28	28-Pin QSOP	
PI6C3Q993-IQ	Q28	28-Pin QSOP	Industrial
PI6C3Q993-5IQ	Q28	28-Pin QSOP	