Low Skew, 1-to-16
LVCMOS / LVTTL Clock Driver

Product Features

- 16 LVCMOS/LVTTL outputs (4 banks of 4 outputs)
- Selectable differential or single-ended clock inputs
- CLK1, nCLK1 pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- CLK0 supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Independent bank control for ÷1 or ÷2 operation
- Independent output bank voltage settings for 3.3V, 2.5V, or 1.8V operations
- Output skew: 170ps (max)
- Bank skew: 50ps (max)
- Part-to-part skew: 800ps (max)
- 3.3V core, 3.3V, 2.5V, or 1.8V output operating supply
- -40° to +85°C ambient operating temperature
- Available packages:
  -Pb-free & green 48-pin LQFP(FB)

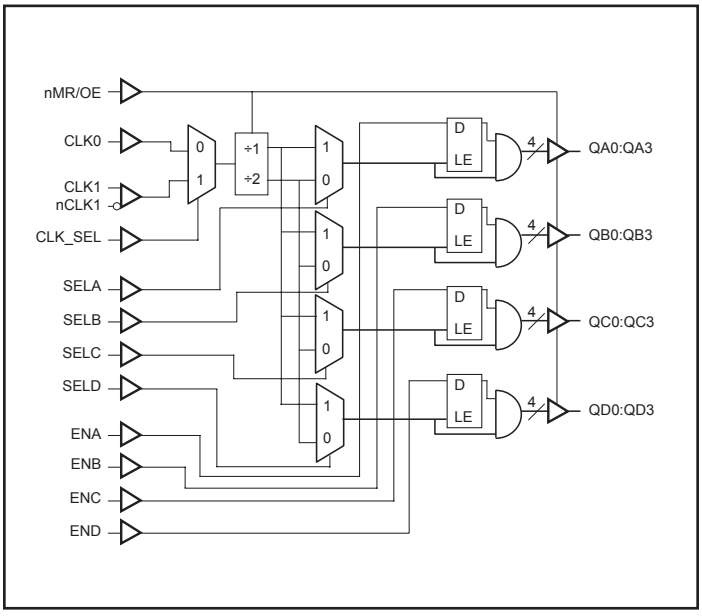
Product Description

The PI6C487016 is a low skew. 1:16 LVCMOS/LVTTL Clock Driver. The device has 4 banks of 4 outputs and each bank can be independently selected for ÷1 or ÷2 frequency operation. Each bank also has its own power supply pins so that the banks can operate at the following different voltage levels: 3.3V, 2.5V, and 1.8V. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines.

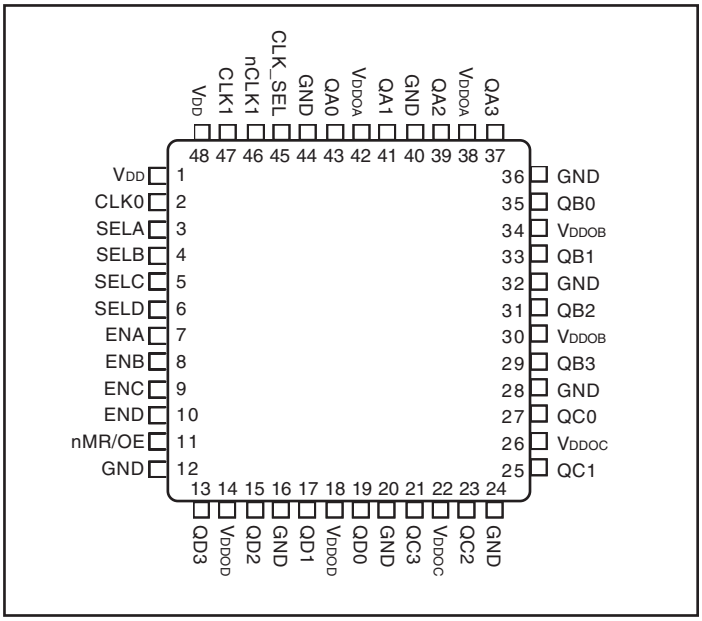
The divide select inputs, SELA:SELD, control the output frequency of each bank with either ÷1 or ÷2 frequency operation. The bank enable inputs, ENA:END, support enabling and disabling each bank of outputs individually. The outputs synchronized when enabling or disabling the clock outputs. The master reset input nMR/OE, resets the ÷1/÷2 flip flops and also controls the active and high impedance states of all outputs.

The PI6C487016 is characterized to operate with the core at 3.3V and the output banks at 3.3V, 2.5V or 1.8V.

Block Diagram



Pin Description



Pin Descriptions

Number	Name	Type		Description
1, 48	V_{DD}	Power		Core supply pins (3.3V)
2	CLK0	Input	Pulldown	LVCMOS / LVTTL clock input
3, 4, 5, 6	SELA : SELD	Input	Pullup	Controls frequency division for outputs. LVCMOS / LVTTL interface levels. QAx:QDx
7, 8, 9, 10	ENA : END	Input	Pullup	Output enable for QAx : QDx Outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS / LVTTL interface levels.
11	nMR/OE	Input	Pullup	Master reset. When LOW, resets the ÷1/÷2 flip flops and sets the outputs to high impedance. LVCMOS / LVTTL interface levels.
12, 16, 20, 24, 28, 32, 36, 40, 44	GND	Power		Supply Ground
13, 15, 17, 19	QD0 : QD3	Output		Bank D Outputs, LVCMOS / LVTTL interface levels.
14, 18	V_{DDOD}	Power		Voltage supply for QD0 : QD3
21, 23, 25, 27	QC0 : QC3	Output		Bank C outputs, LVCMOS / LVTTL interface levels.
22, 26	V_{DDOC}	Power		Voltage supply for QC0 : QC3
29, 31, 33, 35	QB0 : QB3	Output		Bank B outputs, LVCMOS / LVTTL interface levels.
30, 34	V_{DDOB}	Power		Voltage supply for QB0 : QB3
37, 39, 41, 43	QA0 : QA3	Output		Bank A outputs, LVCMOS / LVTTL interface levels.
38, 42	V_{DDOA}	Power		Voltage supply for QA0 : QA3
45	CLK_SEL	Input	Pulldown	Clock select input, when HIGH, selecs CLK1, nCLK1 inputs. When LOW, selects CLK0 input. LVCMOS / LVTTL interface levels.
46	nCLK1	Input	Pullup	inverting differential clock input
47	CLK1	input	Pulldown	Non-inverting differential clock input

Notes:
1. Pullup and Pulldown refer to internal input resistors. See Table 2, Pin characteristics, for typical values.

Function Table

Inputs			Outputs	
nMR/OE	**ENx**	**SELx**	**Bank X**	**Qx Frequency**
0	X	X	Hi Z	N/A
1	1	0	Active	$F_{IN}/2$
1	1	1	Active	F_{IN}
1	0	X	Low	N/A

Absolute Maxium Ratings

Supply Voltage, VDD 4.6V
Inputs, V_I ..... -0.5V to V_{DD} +0.5V
Outputs, V_0 ..... -0.5V to V_{DDO} +0.5V
Package Thermal Impedance, $Ø_{JA}$ ..... 47.9º C/W (0lfpm)
Storage Temperature, T_{STG} ..... -65ºC to +150ºC

Notes:

1. Stresses byond those listed under Absolute Maximun Ratings may caouse permanent damage to the device. These ratings are stress specifcations only. Functional operation of products at these conditions or any conditions beyond those listed in the DC Characteristics or AC characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Pin Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		
CPD	Power Dissaipation Capacitance (per output)	V_{DD}, V_{DDOX} = 3.465V			18	pf
		V_{DD} = 3.465, V_{DDOX} = 2.625V			20	
		V_{DD} = 3.465, V_{DDOX} = 1.895V			30	
R_{OUT}	Output Impedance		5	7	12	Ω

Power Supply DC Characteristics, (V_{DD} = 3.3V ±5%, T_A = -40º to +85ºC)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDOX}	Output Supply Voltage	3.135	3.3	3.465	
		2.375	2.5	2.625	
		1.71	1.8	1.89	
I_{DD}	Core Supply Current			100	mA
I_{DDOX}	Output Supply Current(1)			15	

Note:

1. Measured with all outputs disabled (ENx=0, nMR=1)

LVCMOS/LVTTL DC Characteristics, (V_{DD} = 3.3V ±5%, T_A = -40º to +85ºC)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	SELx, ENX, nMR/OE, CLK_SEL		2		V_{DD} + 0.3	V
		CLK0		2		V_{DD} + 0.3	
V_{IL}	Input Low Voltage	SELx, ENx, nMR/OE, CLK_SEL		-0.3		0.8	
		CLK0		-0.3		1.3	
I_{IH}	Input High Current	ENx, SELx, nMR/OE	V_{DD} = V_{IN} = 3..465V			5	µA
		CLK0, CLK_SEL				150	
I_{IL}	Input Low Current	ENx, SELx, nMR/OE	V_{DD} = 3.465, V_{IN} = 0V	-150			
		CLK0, CLK_SEL		-5			
V_{OH}	Output High Voltage(1)		V_{DDOX} = 3.3 ± 5%	2.6			V
			V_{DDOX} = 2.5 ± 5%	1.8			
			V_{DDOX} = 1.8 ± 5% I_{OH} = -2mA	V_{DD} - 0.45			
V_{OL}	Output Low Voltage(1)		V_{DDOX} = 3.3 ± 5%			0.5	
			V_{DDOX} = 2.5 ± 5%			0.5	
			V_{DDOX} = 1.8 ± 5% I_{OH} = -2mA			0.45	
I_{OZL}	Output Tristate Current Low			-5			µA
I_{OZH}	Output Tristate Curretn High					5	

Notes:

1. Outputs terminate with 50Ω to V_{DDOX}/2. See Parameter Measurement information, Output Load Test Circut

Differential DC Characteristics, (V_{DD} = 3.3V ±5%, T_A = -40º to +85ºC)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	nCLK1	V_{IN} = V_{DD} = 3.465V			5	µA
		CLK1	V_{IN} = V_{DD} = 3.465V			150	
I_{IL}	Input Low Current	nCLK1	V_{IN} = 0V, V_{DD} = 3.465V	-150			
		CLK1	V_{IN} = 0V, V_{DD} = 3.465V	-5			
V_{PP}	Peak-to-peak Input Voltage			0.15		1.3	V
V_{CMR}	Common mode input voltage(1,2)			GND + 0.5		V_{DD} -0.85	

Notes:

1. For single ended application, the maximum input voltage for CLK1, nCLK1 is V_{DD} + 0.3V.
2. Common mode voltage is definded as V_{IH}.

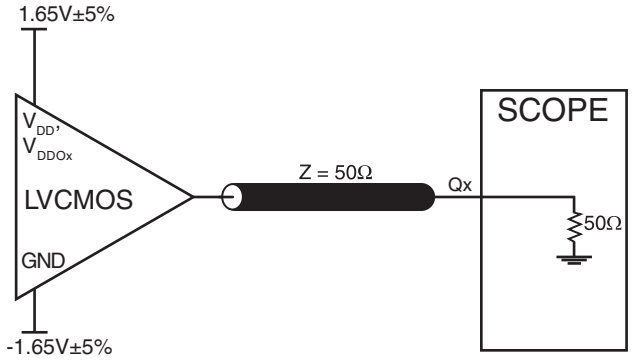
AC Characteristics, (V_{DD} = 3.3V ±5%, V_{DDOX} = 1.8V ±5% to 3.3V ±5%, T_A = -40º to +85ºC)[7]

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Units
f_{MAX}	Output Frequency					250	MHz
Tp_{LH}	Propagation Delay, Low to High	CLK0[1]	V_{DDOX} = 3.3V	2.3	3.4	3.9	ns
		CLK1, nCLK1[2]		2.5	3.4	3.9	
		CLK0[1]	V_{DDOX} = 2.5V	2.3	3.5	4.0	
		CLK1, nCLK1[2]		2.5	3.5	4.0	
		CLK0[1]	V_{DDOX} = 1.8V	2.4	3.9	4.7	
		CLK1, nCLK1[2]		2.6	3.9	4.7	
tsk(b)	Bank skew[3]		Measured on the rising edge			50	ps
tsk(o)	Output skew[4]		Measured on the rising edge			170	
tsk(pp)	Part-to-Part skew[5]					800	
t_R/t_F	Output Rise/Fall Time[5]		20% to 80%	200		700	
odc	Output duty cycle			40		60	%
t_{EN}	Output enable time[6]					10	ns
t_{DIS}	Output Disable Time[6]					10	

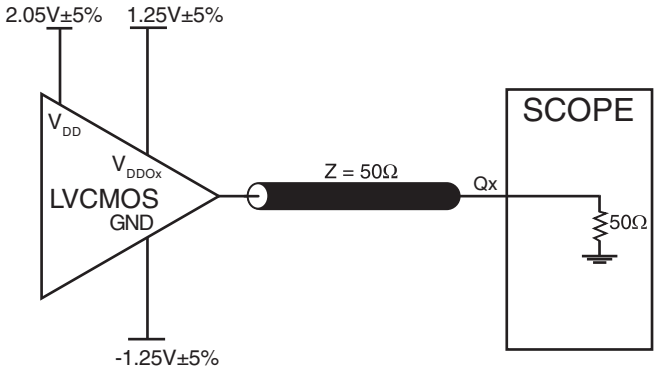
Notes:

1. Measured from the V_{DD}/2 of the input to V_{DDOX}/2 of the output
2. Measured from the differential input crossing point to V_{DDOX}/2 of the output
3. Defined as a skew within a bankwith equal load conditions
4. Defined as a skew between outputs at the same supply voltage, same frequency, and with equal load conditions. Measured at V_{DDOX}/2
5. Defined as a skew between outputs on a different devices operation at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDOX}/2.
6. These parameters are guaranteed by characterizatoin. Not tested in prodution.
7. All parameters are measured at 250MHz with SEL [A:D] = 1 unless noted otherwise.

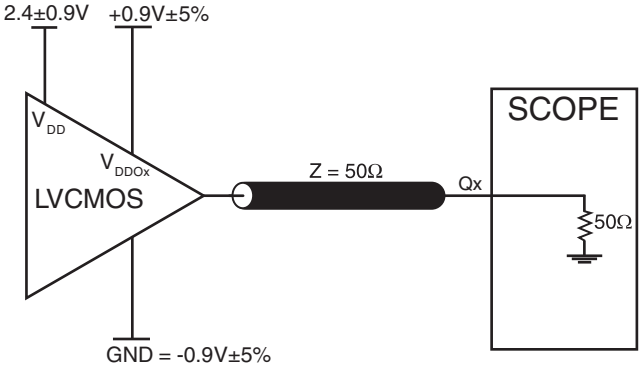
Parameter Measurement Information



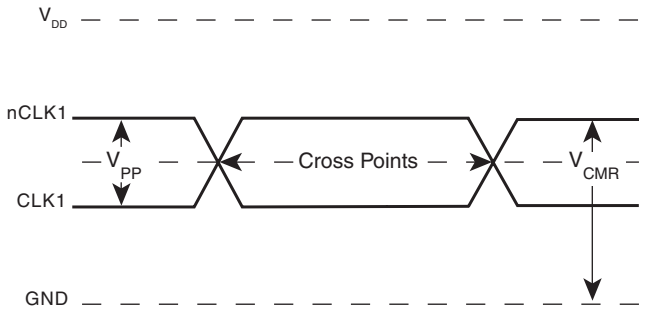
3.3V Core/3.3V Output Load AC Test Circuit



3.3V Core/2.5V Output Load AC Circuit



3.3V Core/1.8V Output Load AC Test Circuit



Differential Input Level

Application Information

Wiring the differenctial input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = VDD/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 adn R2 might need to be adjusted to postion the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R1/R2 = 0.609.

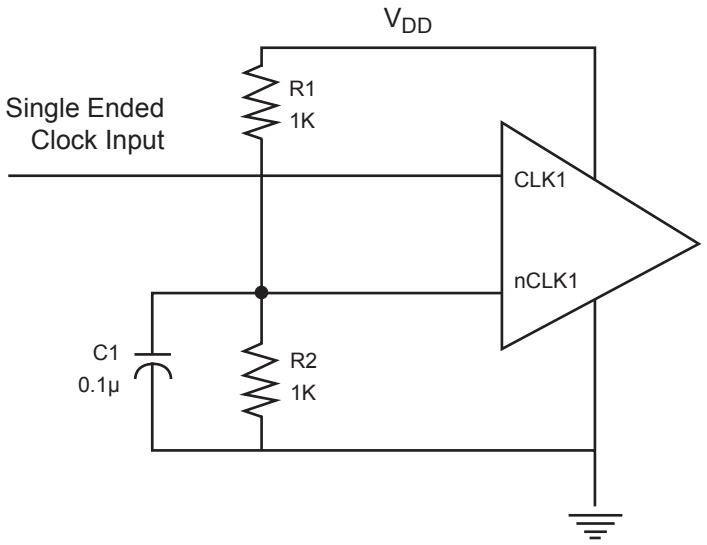
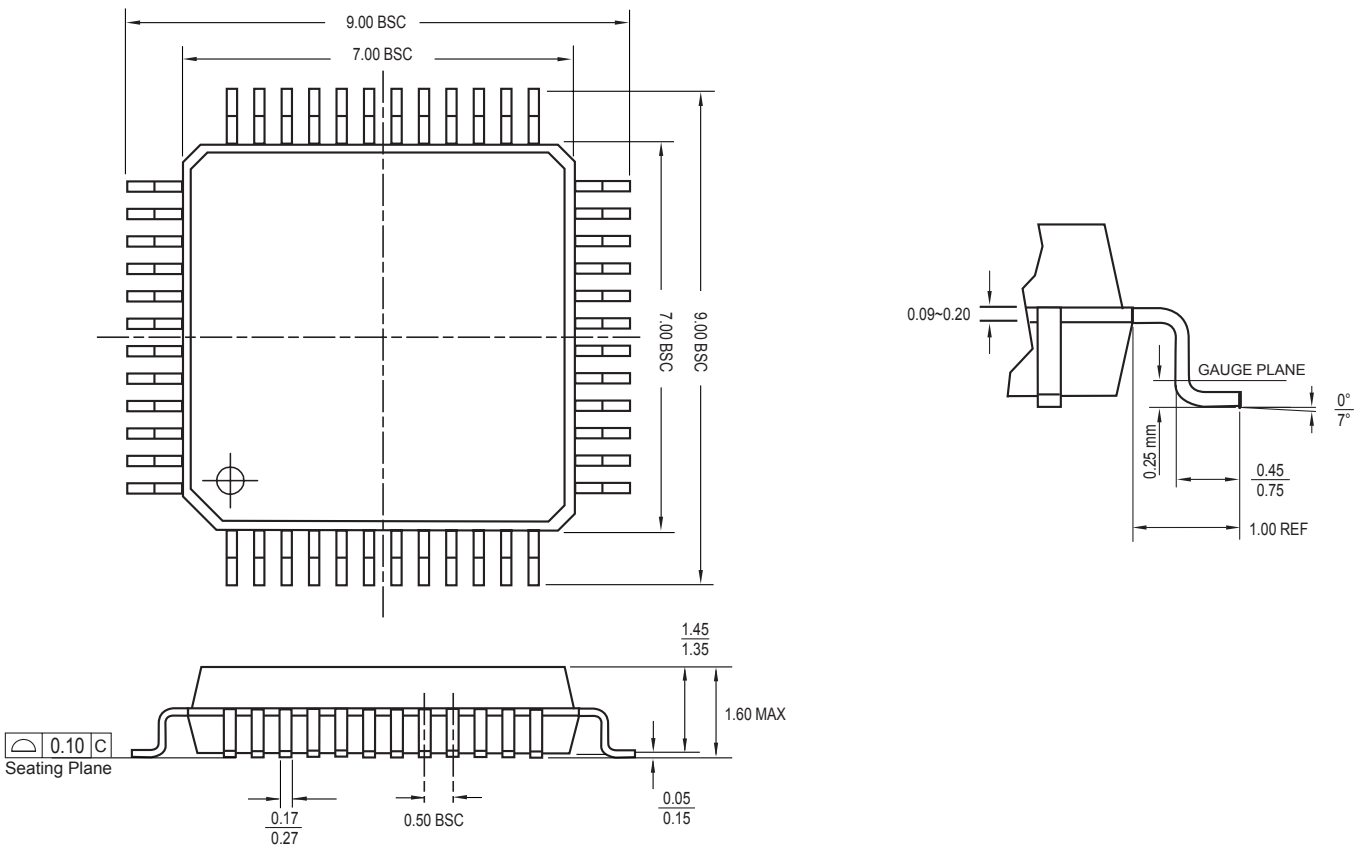


Figure 1: Single-ended Signal Driving Differential Input

Package Mechanical: 48-pin LQFP (FB)



Ordering Information

Ordering Code	Package Code	Package Type
PI6C487016FBE	FB	Pb-free & Green, 48-pin LQFP

Notes:

1. Thermal characteristics can be found on the company web site at http://www.pericom.com/packaging/
2. Number of Transistors = TBD