Data Sheet, DS 1, December 2001

ABM 3G
ATM Buffer Manager

PXF 4333 Version 1.1

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Edition 2001-12-17

**Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany**

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ABM-3G Data Sheet

Revision History:	**2001-12-17**	DS 1
Previous Version:	none	

Page	Subjects (major changes since last revision)
	Reworked from preliminary to first finalized status

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Table of Contents **Page**

Table of Contents **Page**

Table of Contents | Page

Table of Contents **Page**

Table of Contents **Page**

List of Figures

List of Figures **Page**

List of Tables **Page**

List of Tables **Page**

List of Registers **Page**

List of Registers **Page**

List of Registers **Page**

Preface

The purpose of this Data Sheet is to provide comprehensive information about the ABM-3G device regarding system-level integration, hardware/board design, and software driver aspects.

Organization of this Document

This Data Sheet is divided into 13 chapters and two appendices. It is organized as follows:

- **Chapter 1, Overview**
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.

- **Chapter 2, Pin Descriptions**
  Lists pin locations with associated signals, categorizes signals according to function, and describes the signals.

- **Chapter 3, Functional Description**
  Gives descriptions of major functional blocks, configuration tables, and global device functions.

- **Chapter 4, Operational Description**
  Describes basic initialization and operation procedures.

- **Chapter 5, Interface Description**
  Gives a functional description of all interfaces.

- **Chapter 6, Memory Structure**

- **Chapter 7, Register Description**
  Lists all registers and tables with functional description.

- **Chapter 8, Electrical Characteristics**
  Provides detailed information about electrical characteristics and interface timings.

- **Chapter 9, Test Mode**

- **Chapter 10, Package Outlines**

- **Chapter 11, Glossary**

Related Documentation

[1] ITU-T Recommendation I.371, Traffic Control and Congestion Control in B-ISDN, 2nd Release, March 1996.
[2] ATMF, Traffic Management Specification 4.1, March 1999.
[3] ATMF, UTOPIA Level 1 Specification Version 2.01, March 1994.
[4] ATMF, UTOPIA Level 2 Specification Version 1, June 1995.

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Please provide in the subject of your e-mail:
device name (ABM-3G), device part number (PXF 4333), device version (Version 1.1),

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document type (Data Sheet), issue date (2001-12-17) and document revision number (DS 1).

1 Overview

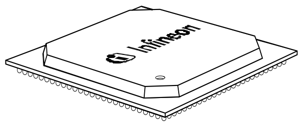
The ABM-3G PXF 4333 Version 1.1 is Infineon’s new generation ATM Buffer Manager device. It addresses the performance needs of new multi-service platforms with combined ATM cell and packet-handling applications. The ABM-3G manages ATM traffic flowing through multi-service platforms in which voice, video, and data traffic converge. The optimizes the interworking of ATM and higher-layer traffic-management and flow-control schemes. Optional “leaky bucket” shaping per queue provides full VBR support. The ABM-3G is useful in applications where extensive ATM traffic management capabilities are required. This includes either distributed or centralized system architectures that cover enterprise and Central Office switches, DSLAMs, and ATM line cards for routers and switches.

ATM Buffer Manager
ABM-3G

ABM-3G

PXF 4333 V1.1

1.1 Features



P-BGA-456

- ATM Traffic Management processing support up to STM-4/OC-12 equivalent bandwidth
- Throughput at UTOPIA Interface up to 687 Mbit/s transmit, 795 Mbit/s receive
- Speed-up factor relative to STM-4/OC12: 1.32
- Uni-directional mode with combined resources of both directions (optional)
- 256K cells buffer per direction (configurable in guaranteed and shared buffer)
- Up to 16384 connections arbitrarily assignable to queues for sharing connections and saving resources
- Up to 8192 queues per direction, individually assignable to schedulers and to traffic classes
- Up to 128 Scheduler Blocks (SB) per direction with programmable service rates, individually assignable to UTOPIA ports
- The ABM-3G is cascadable to provide up to 512 schedulers, 32K queues, and 1M cell memories per direction
- Up to 16 traffic classes with individually-selectable thresholds for highest service differentiation
- Up to 48 ports per UTOPIA Interface
- Standards-compliant support for the following ATM Forum service categories: CBR, rt-VBR, nrt-VBR, GFR, UBR, UBR+
- Generic PHB (Per Hop Behavior) characteristics are configurable (PHB traffic class is not standardized)
- Configurable cell-address translation modes

1.1.1 Queueing Functions

- Per-VC queueing for up to 8192 connections per direction for optimal connection isolation

Type	Package
ABM-3G PXF 4333 V1.1	BGA-456

- Optional queue sharing
- Guaranteed per-queue minimum buffer reservation
- Cell acceptance based on programmable threshold sets with hysteresis evaluation
- Threshold sets for individual queues, traffic classes, schedulers, and global buffer for optimized buffer sharing
- Per VC Packet Discard, including Early Packet Discard (EPD) & Partial Packet Discard (PPD) thresholds for Guaranteed Frame Rate (GFR) support
- Cell Loss Priority (CLP) aware selective discard thresholds
- UTOPIA input port backpressure thresholds without head-of-line-blocking

1.1.2 Scheduling Functions

- Multistage scheduling units with
  - Work conservative Weighted Round Robin (WRR) scheduling stage for 128 Scheduler Blocks
  - Each Scheduler Block comprising of
    - a Weighted Fair Queueing (WFQ) scheduler with 16320 programmable weight factors for each queue, providing rate guarantees and fairness in bandwidth allocation
    - a high priority Round Robin (RR) scheduler for real-time traffic
    - a low priority RR scheduler for best effort traffic
- Additional common real-time bypass queue for each direction, for cascading multiple ABM-3Gs
- Selectable Peak Cell Rate (PCR) shaping for each queue with minimum 2.62 Kbps and maximum 343 Mbit/s at 52 MHz clock (65472 programmable rates)
- Selectable Variable Bit Rate (VBR.1.2.3) leaky bucket shaping for up to 2046 queues
- VC merge function for up to 128 merge groups (arbitrary queues per merge group) for Multi Protocol Label Switching (MPLS) applications
- SB scheduler overbooking possibility

1.1.3 Interfaces

- Two external SDRAM Interfaces for cell storage, one for upstream and one for downstream direction (up to 256 K cell buffer per direction)
- One common cell pointer SSRAM Interface
- Multiport UTOPIA Level 2 Interface in up- and downstream direction conforming to the specifications of the ATM Forum [4]
  - 4-cell FIFO buffer at UTOPIA receive interfaces for clock synchronization (head-of-line blocking-free)
  - 64-cell buffer logical queueing for up to 48 PHYs at UTOPIA transmit interfaces (head-of-line blocking-free)
- 16-bit Microprocessor Interface, configurable as Intel or Motorola type (with AAL5 packet insertion/extraction support)

- Queue Congestion Indication Interface
- JTAG Boundary Scan Interface

1.1.4 Supervision Functions

- Internal pointer supervision
- Cell-header protection function

1.1.5 Technology

- Supply voltages 1.8 V (core) and 3.3 V (I/Os)
- Ball Grid Array BGA-456 package (Plastic BGA $(35\ mm)^2$)
- Temperature range -40°C to 85°C
- Power dissipation 2.0 W (typical)

1.2 Logic Symbol

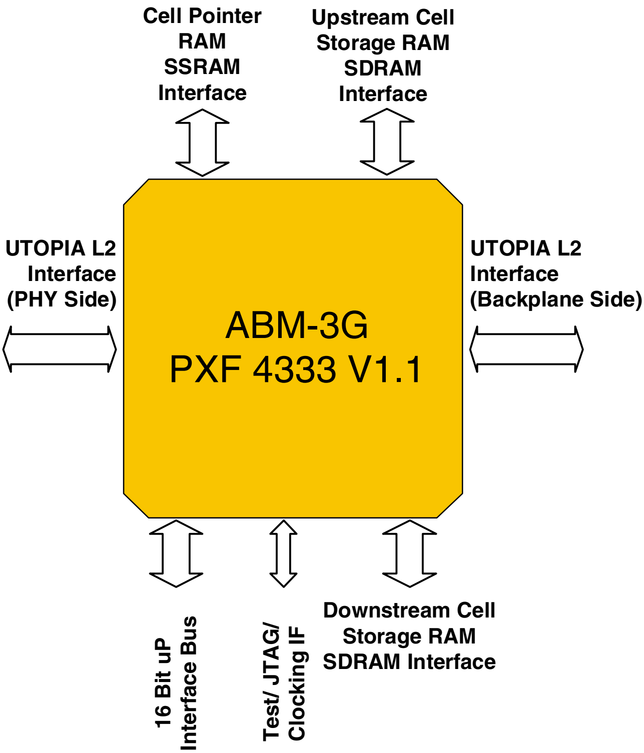


Figure 1-1 Logic Symbol

1.3 Typical Applications

The ABM-3G device is designed for traffic management on line cards and trunk cards such as are used in:

- ATM Switches
- DSLAMs, DLCs
- Multi-Service Access Switches
- 3G Wireless Infrastructure

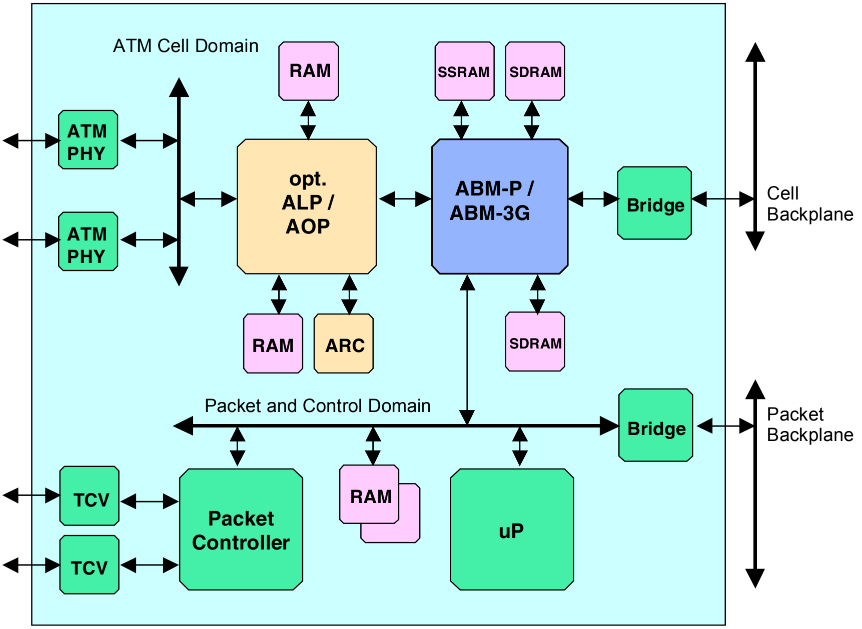


Figure 1-2 General System Integration

2 Pin Descriptions

2.1 Pin Diagram

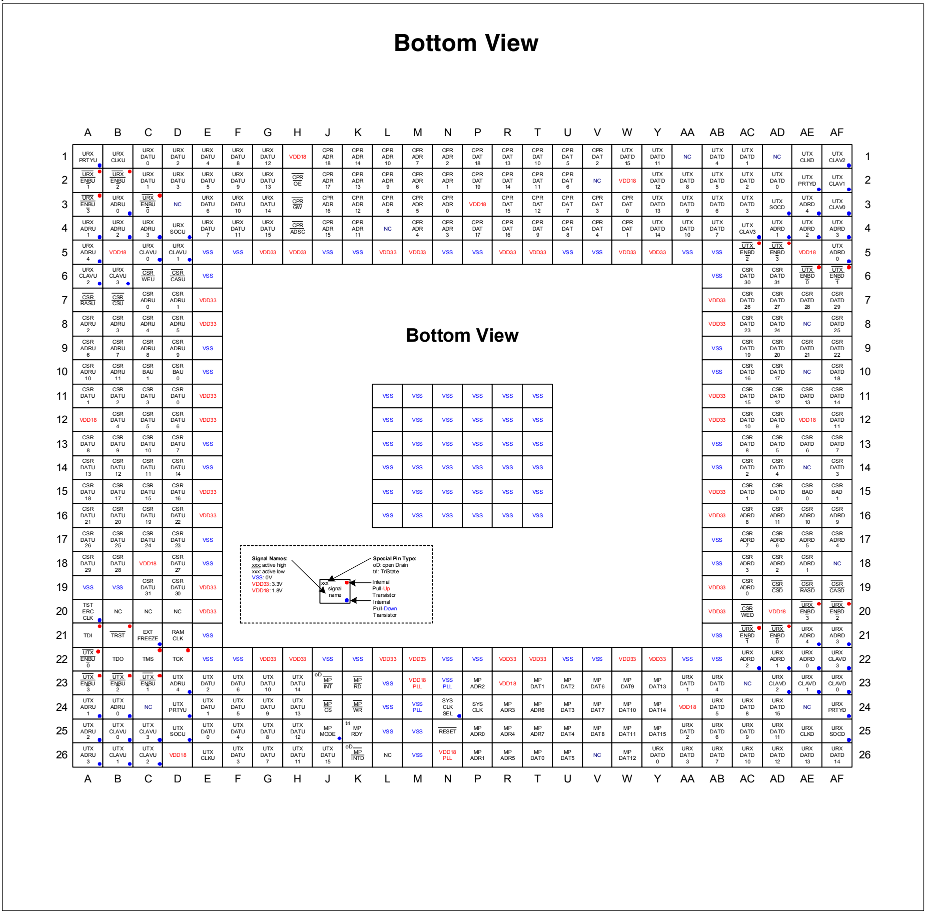


Figure 2-1 Pin Configuration (Bottom View)

2.2 Pin Diagram with Functional Groupings

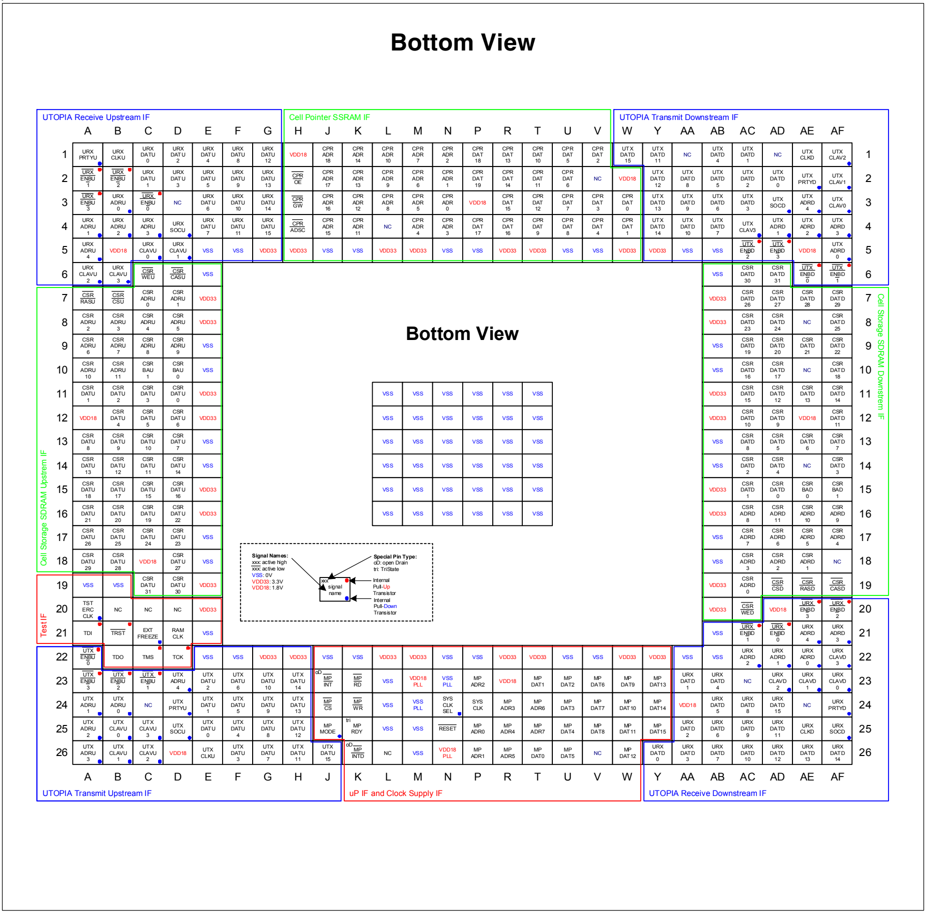


Figure 2-2 Pin Configuration (Bottom View)

2.3 Pin Definitions and Functions

Table 2-1 lists and explains all pins/balls organized into functional groups. Table 2-1 uses the following naming conventions:

Ball No. Ball Number with respect to package outline (see Figure 2-1)

Symbol Signal Name

Type Type of pin/ball:

I	Input pin
I_{PD}	Input pin (Internal Pull-Down Transistor)
I^{PU}	Input pin (Internal Pull-Up Transistor)
O	Output pin (Push/Pull)
O (oD)	Output pin (Open Drain)
O (tri)	Output pin (TriState)

Function Functional pin/ball description

Note: The ABM-3G signal pins are not 5 V I/O tolerant. For further details refer to "DC Characteristics" on Page 337.

Table 2-1 Ball Definitions and Functions

Ball No.	Symbol	Type	Function
2.3.1 Common System Clock Supply (3 pins)			
P24	SYSCLK	I	System Clock This clock signal feeds DPLL1 and DPLL2 and the internal ABM-3G Core Clock, depending on signal SYSCLKSEL.
N24	SYSCLKSEL	I_{PD}	Internal ABM-3G Core Clock Source Select: 'H': Internal Core Clock is supplied by signal SYSCLK 'L': Internal Core Clock is supplied by DPLL1

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol	Type	Function
D21	RAMCLK	O	Reference clock for external RAM (CSRU, CSRD and CPR)

2.3.2 UTOPIA Receive Interface Upstream (Master/Slave) (32 pins)

Ball No.	Symbol		Type	Function
G4, G3, G2, G1, F4, F3, F2, F1, E4, E3, E2, E1, D2, D1, C2, C1	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	URXDATU(15:0)	I	UTOPIA Receive Data Bus Upstream (from PHY)
A1	URXPRTYU		I_{PD}	UTOPIA Receive Odd Parity of URXDATU(15:0) (PHY side)
A5, C4, B4, A4, B3	4, 3, 2, 1, 0	URXADRU(4:0)	I/O_{PD}	UTOPIA Receive Address Bus (PHY side) Master Mode: output Slave Mode: input
A3, B2, A2, C3	3, 2, 1, 0	$\overline{URXENBU(3:0)}$	I/O^{PU}	UTOPIA Receive Enable Bus (PHY side) Master Mode: output Slave Mode: input

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol		Type	Function
B6, A6, D5, C5	3, 2, 1, 0	URXCLAVU(3:0)	I/O$_{PD}$	UTOPIA Receive CLAV Bus (PHY side) Master Mode: input Slave Mode: output
D4	URXSOCU		I$_{PD}$	UTOPIA Receive Start of Cell signal (PHY side)
B1	URXCLKU		I	UTOPIA Receive Clock signal (PHY side)

2.3.3 UTOPIA Transmit Interface Downstream (Master/Slave) (32 pins)

Ball No.	Symbol		Type	Function
W1, Y4, Y3, Y2, Y1, AA4, AA3, AA2, AB4, AB3, AB2, AB1, AC3, AC2, AC1, AD2	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	UTXDATD(15:0)	O	UTOPIA Transmit Data Bus Downstream (to PHY)
AE2	UTXPRTYD		O$_{PD}$	UTOPIA Transmit Odd Parity of UTXDATD(15:0) (PHY side)

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol		Type	Function
AE3, AF4, AE4, AD4, AF5	4, 3, 2, 1, 0	UTXADRD(4:0)	I/O_{PD}	UTOPIA Transmit Address Bus (PHY side) Master Mode: output Slave Mode: input
AD5, AC5, AF6, AE6	3, 2, 1, 0	$\overline{\text{UTXENBD(3:0)}}$	I/O^{PU}	UTOPIA Transmit Enable Bus (PHY side) Master Mode: output Slave Mode: input
AC4, AF1, AF2, AF3	3, 2, 1, 0	UTXCLAVD(3:0)	I/O_{PD}	UTOPIA Transmit CLAV Bus (PHY side) Master Mode: input Slave Mode: output
AD3	UTXSOCD		O_{PD}	UTOPIA Transmit Start of Cell signal (PHY side)
AE1	UTXCLKD		I	UTOPIA Transmit Clock signal (PHY side)

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol	Type	Function
2.3.4 UTOPIA Receive Interface Downstream (Master/Slave) (32 pins)			
AD24, AF26, AE26, AD26, AD25, AC26, AC25, AC24, AB26, AB25, AB24, AB23, AA26, AA25, AA23, Y26	URXDATD(15:0): 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	I	UTOPIA Receive Data Bus Downstream (from Backplane)
AF24	URXPRTYD	I_{PD}	UTOPIA Receive Odd Parity of URXDATD(15:0) (Backplane side)
AE21, AF21, AC22, AD22, AE22	URXADRD(4:0): 4, 3, 2, 1, 0	I/O_{PD}	UTOPIA Receive Address Bus (Backplane side) Master Mode: output Slave Mode: input
AE20, AF20, AC21, AD21	$\overline{\text{URXENBD(3:0)}}$: 3, 2, 1, 0	I/O^{PU}	UTOPIA Receive Enable Bus (Backplane side) Master Mode: output Slave Mode: input

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol		Type	Function
AF22, AD23, AE23, AF23	3, 2, 1, 0	URXCLAVD(3:0)	I/O_{PD}	UTOPIA Receive CLAV Bus (Backplane side) Master Mode: input Slave Mode: output
AF25	URXSOCD		I_{PD}	UTOPIA Receive Start of Cell signal (Backplane side)
AE25	URXCLKD		I	UTOPIA Receive Clock signal (Backplane side)

2.3.5 UTOPIA Transmit Interface Upstream (Master/Slave) (32 pins)

Ball No.	Symbol		Type	Function
J26, H23, H24, H25, H26, G23, G24, G25, G26, F23, F24, F25, F26, E23, E24, E25	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	UTXDATU(15:0)	O	UTOPIA Transmit Data Bus Upstream (to Backplane)
D24	UTXPRTYU		O_{PD}	UTOPIA Transmit Odd Parity of UTXDATU(15:0) (Backplane side)

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol		Type	Function
D23, A26, A25, A24, B24	4, 3, 2, 1, 0	UTXADRU(4:0)	I/O_{PD}	UTOPIA Transmit Address Bus (Backplane side) Master Mode: output Slave Mode: input
A23, B23, C23, A22	3, 2, 1, 0	$\overline{\text{UTXENBU(3:0)}}$	I/O^{PU}	UTOPIA Transmit Enable Bus (Backplane side) Master Mode: output Slave Mode: input
C25, C26, B26, B25	3, 2, 1, 0	UTXCLAVU(3:0)	I/O_{PD}	UTOPIA Transmit CLAV Bus (Backplane side) Master Mode: input Slave Mode: output
D25	UTXSOCU		O_{PD}	UTOPIA Transmit Start of Cell signal (Backplane side)
E26	UTXCLKU		I	UTOPIA Transmit Clock signal (Backplane side)

2.3.6 Microprocessor Interface (32 pins)

N25	$\overline{\text{RESET}}$	I	ABM-3G Reset

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol		Type	Function
Y25, Y24, Y23, W26, W25, W24, W23, V25, V24, V23, U26, U25, U24, U23, T23, T26	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	MPDAT(15:0)	I/O	Microprocessor Data Bus
T25, T24, R26, R25, R24, P23, P26, P25	7, 6, 5, 4, 3, 2, 1, 0	MPADR(7:0)	I	Microprocessor Address Bus
K24	$\overline{\text{MPWR}}$		I	$\overline{\text{WR}}$ when MPMOD=0 (Intel Mode) R/$\overline{\text{W}}$ when MPMOD=1 (Motorola Mode).
K23	$\overline{\text{MPRD}}$		I	$\overline{\text{RD}}$ when MPMOD=0 (Intel Mode) $\overline{\text{DS}}$ when MPMOD=1 (Motorola Mode).
J24	$\overline{\text{MPCS}}$		I	Chip Select from Microprocessor.
J23	$\overline{\text{MPINT}}$		O(oD)	Interrupt Request to Microprocessor. Open drain, needs external pull-up resistor. Interrupt pins of several devices can be wired-or together.
K25	MPRDY		O(tri)	Ready Output to Microprocessor for read and write accesses.

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol	Type	Function
J25	MPMODE	I_{PD}	Intel/Motorola select: 'L' Intel type processor 'H' Motorola type processor

2.3.7 Cell Storage RAM Upstream (50 pins)

C19,	31,	CSRDATU(31:0)	I/O	Data Bus to Cell Storage RAM Upstream
D19,	30,			
A18,	29,			
B18,	28,			
D18,	27,			
A17,	26,			
B17,	25,			
C17,	24,			
D17,	23,			
D16,	22,			
A16,	21,			
B16,	20,			
C16,	19,			
A15,	18,			
B15,	17,			
D15,	16,			
C15,	15,			
D14,	14,			
A14,	13,			
B14,	12,			
C14,	11,			
C13,	10,			
B13,	9,			
A13,	8,			
D13,	7,			
D12,	6,			
C12,	5,			
B12,	4,			
C11,	3,			
B11,	2,			
A11,	1,			
D11	0			

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol	Type	Function
D10	CSRBAU0	O	Cell Storage RAM Bank Address 0 Upstream
C10	CSRBAU1	O	Cell Storage RAM Bank Address 1 Upstream
B10, A10, D9, C9, B9, A9, D8, C8, B8, A8, D7, C7	CSRADRU(11:0) 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	O	Address Bus of Cell Storage RAM Upstream
B7	$\overline{\text{CSRCSU}}$	O	Cell Storage RAM Upstream Chip Select
A7	$\overline{\text{CSRRASU}}$	O	Cell Storage RAM Upstream Row Address Strobe
D6	$\overline{\text{CSRCASU}}$	O	Cell Storage RAM Upstream Column Address Strobe
C6	$\overline{\text{CSRWEU}}$	O	Cell Storage RAM Upstream Write Enable

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol		Type	Function
2.3.8	**Cell Storage RAM Downstream (50 pins)**			
AD6,	31,	CSRDATD(31:0)	I/O	Data Bus to Cell Storage RAM Downstream
AC6,	30,			
AF7,	29,			
AE7,	28,			
AD7,	27,			
AC7,	26,			
AF8,	25,			
AD8,	24,			
AC8,	23,			
AF9,	22,			
AE9,	21,			
AD9,	20,			
AC9,	19,			
AF10,	18,			
AD10,	17,			
AC10,	16,			
AC11,	15,			
AF11,	14,			
AE11,	13,			
AD11,	12,			
AF12,	11,			
AC12,	10,			
AD12,	9,			
AC13,	8,			
AF13,	7,			
AE13,	6,			
AD13,	5,			
AD14,	4,			
AF14,	3,			
AC14,	2,			
AC15,	1,			
AD15	0			
AE15	CSRBAD0		O	Cell Storage RAM Bank Address 0 Downstream

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol	Type	Function
AF15	CSRBAD1	O	Cell Storage RAM Bank Address 1 Downstream
AD16, AE16, AF16, AC16, AC17, AD17, AE17, AF17, AC18, AD18, AE18, AC19	CSRADRD(11:0) 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	O	Address Bus of Cell Storage RAM Downstream
AD19	$\overline{\text{CSRCSD}}$	O	Cell Storage RAM Downstream Chip Select
AE19	$\overline{\text{CSRRASD}}$	O	Cell Storage RAM Downstream Row Address Strobe
AF19	$\overline{\text{CSRCASD}}$	O	Cell Storage RAM Downstream Column Address Strobe
AC20	$\overline{\text{CSRWED}}$	O	Cell Storage RAM Downstream Write Enable

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol		Type	Function

2.3.9 Common Up- and Downstream Cell Pointer RAM (42 pins)

Ball No.	Symbol		Type	Function
P2, P1, P4, R4, R3, R2, R1, T3, T2, T1, T4, U4, U3, U2, U1, V4, V3, V1, W4, W3	19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	CPRDAT(19:0)	I/O	Data Bus to Cell Pointer RAM

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol		Type	Function
J1, J2, J3, J4, K1, K2, K3, K4, L1, L2, L3, M1, M2, M3, M4, N4, N1, N2, N3	18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	CPRADR(18:0)	O	Address Bus of Cell Pointer RAM
H4	$\overline{\text{CPRADSC}}$		O	Cell Pointer RAM Chip Select
H3	$\overline{\text{CPRGW}}$		O	Cell Pointer RAM Write Enable
H2	$\overline{\text{CPROE}}$		O	Cell Pointer RAM Output Enable

2.3.10 JTAG Boundary Scan (5 pins)

A21	TDI	I^{PU}	Test Data Input.
D22	TCK	I^{PU}	Test Clock.
C22	TMS	I^{PU}	Test Mode Select.
B21	$\overline{\text{TRST}}$	I^{PU}	Test Data Reset
B22	TDO	O	Test Data Output In normal operation, must not be connected.

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol	Type	Function

2.3.11 Production Test (2 pin)

A20	TSTERCCLK	I_{PD}	For device test only, do not connect. Must not be connected in normal operation.
C21	EXTFREEZ	I_{PD}	For device test only, do not connect. Must not be connected in normal operation.

2.3.12 Supply (74 VSS, 32 VDD33 and 14 VDD18 pins)

A19, B19, E5, E6, E9, E10, E13, E14, E17, E18, E21, E22, F5, F22, J5, J22, K5, K22, L11, L12, L13, L14, L15, L16, L23, L24, L25, M11, M12, M13, M14, M15, M16, M25, M26, N5, N11, N12, N13, N14, N15, N16, N22, P5, P11, P12, P13, P14, P15, P16, P22, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, U5, U22, V5, V22, AA5, AA22, AB5, AB6, AB9, AB10, AB13, AB14, AB17, AB18, AB21, AB22	VSS, Chip GND Supply (All pins should be connected to the same level)
E7, E8, E11, E12, E15, E16, E19, E20, G5, G22, H5, H22, L5, L22, M5, M22, R5, R22, T5, T22, W5, W22, Y5, Y22, AB7, AB8, AB11, AB12, AB15, AB16, AB19, AB20	VDD33, Chip 3.3 V Supply (All pins should be connected to the same level)
B5, A12, C18, D26, R23, AA24, AD20, AE12, AE5, W2, P3, H1	VDD18, Chip 1.8 V Supply (All pins should be connected to the same level)
N23, M24	VSS PLL, Chip GND Supply (All pins should be connected to the same level)
N26, M23	VDD18 PLL, Chip 1.8 V Supply (All pins should be connected to the same level)

Table 2-1 Ball Definitions and Functions (cont'd)

Ball No.	Symbol	Type	Function

2.3.13 Unconnected (13 pins)

B20, C20, D20, L26, K26, D3, L4, V2, AA1, AD1, AE8, AE10, AE14, AF18, AE24, AC23, V26, C24	Unconnected pins. It is recommended to leave these pins unconnected on the board to guarantee board compatibility to future device versions.

Note: Total signal pins: 323; total power supply pins: 120.

3 Functional Description

3.1 Block Diagrams

Figure 3-1 shows a typical sub-system integration scenario using the ABM-3G. The memory configurations are examples and depend on the ABM-3G operation modes and required queueing resources.

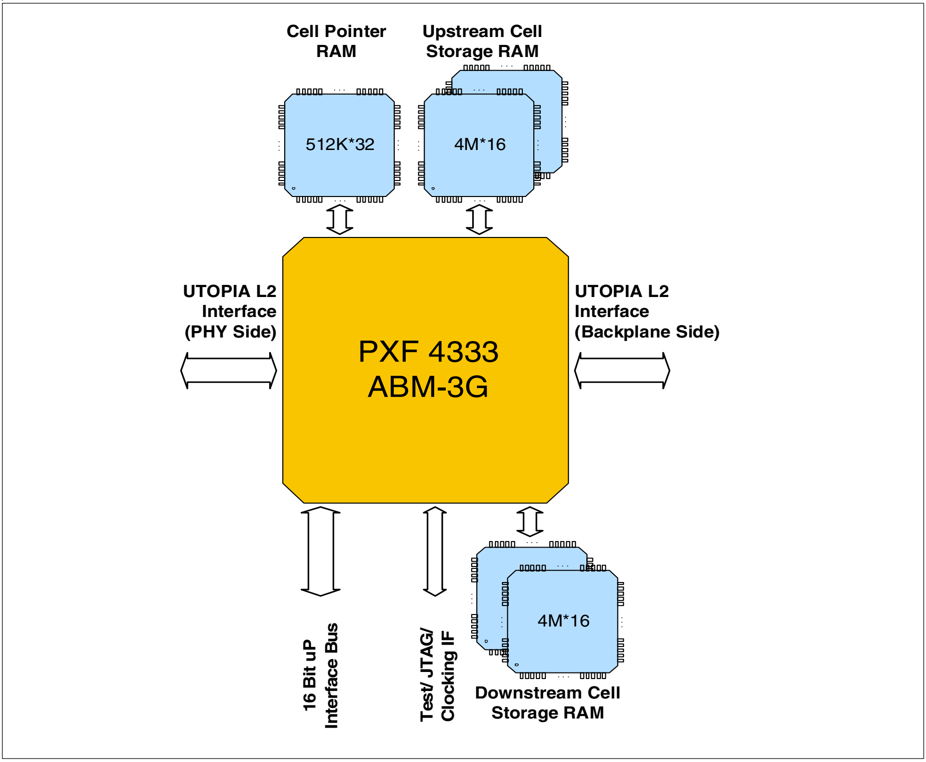


Figure 3-1 Sub-System Integration Diagram

Figure 3-2 shows a functional block diagram of the ABM-3G. The function blocks are referenced and described in more detail in subsequent chapters.

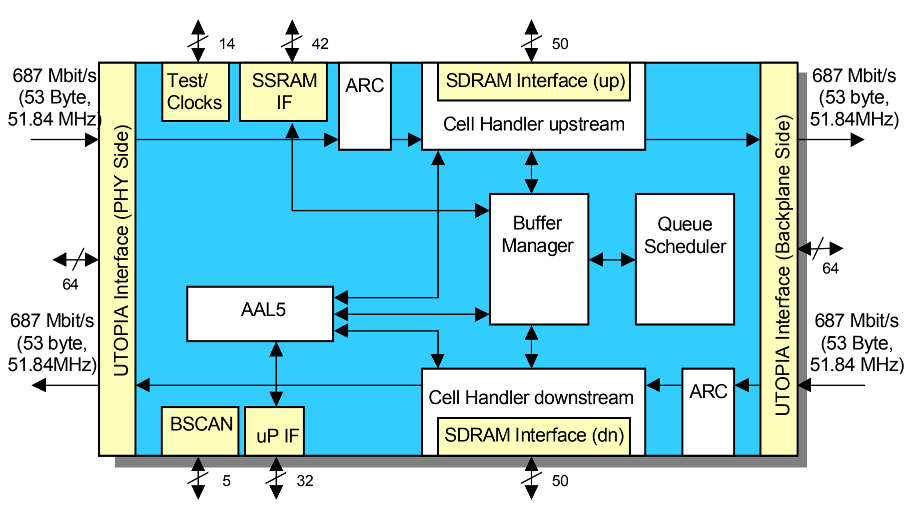


Figure 3-2 Functional Block Diagram

Figure 3-3 shows a logical illustration of the ATM Buffer Manager (ABM-3G) core for one direction.

Cells are assigned to queues in the Buffer Manager unit. The cell acceptance algorithm verifies that no thresholds are exceeded that are provided for queues, schedulers, traffic classes, as well as for the global buffer. Once accepted, a cell cannot be lost, but will be emitted at the respective UTOPIA Interface after some time (exception: queue has been disabled while cells are stored). Alternatively, cells can be received from the Microprocessor Interface via the AAL5 unit. The demultiplexer forwards the cells to the respective queue associated with a scheduler which sorts them for transmission according to the programmed configuration. As part of the scheduling function, an optional Peak Rate Limiter and a Leaky-Bucket shaper are provided for the shaping of individual queues (connections).

The Queue Scheduler and the Buffer Manager are the key units for QoS provisioning in the ABM-3G. The behavior of both units is described in subsequent chapters. The output multiplexer recombines the cell streams of all schedulers. Emitted cells are either forwarded to the UTOPIA Transmit Interface or to the AAL5 unit for extraction.

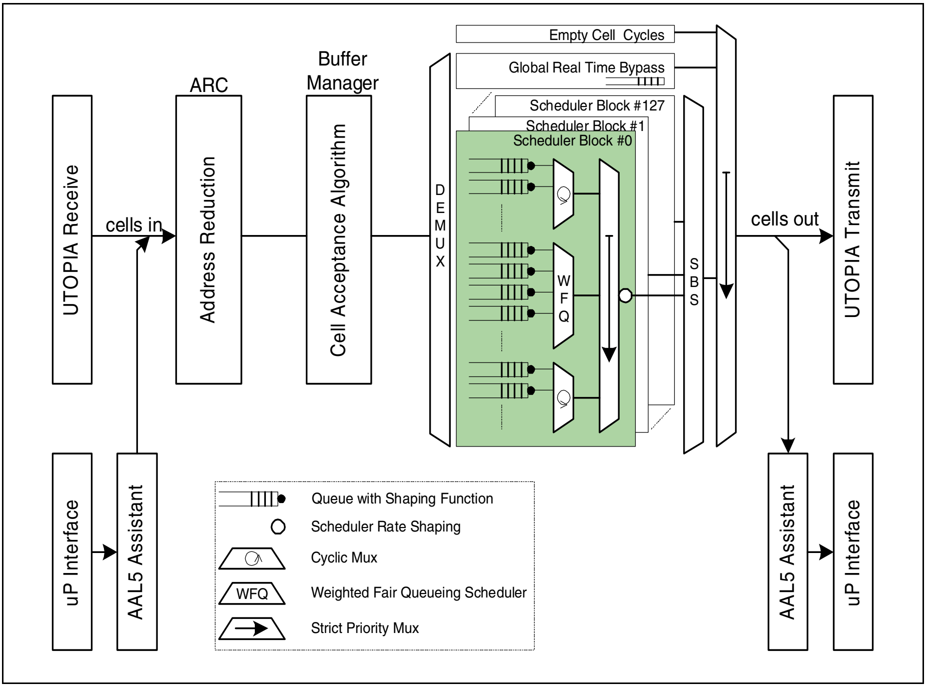


Figure 3-3 Logical Block Diagram (One Direction)

3.1.1 Throughput and Speedup

At a given clock frequency, applied to the ABM-3G UTOPIA interfaces and the ABM-3G core, the core is the limiting factor for throughput because it needs 32 clock cycles per cell as opposed to UTOPIA, which needs only 27+2. The available speedup in the ABM-3G relative to STM-4/OC12 transmission rates is shown in Table 3-4.

Table 3-4 Maximum ABM-3G Throughput and Speedup

Clock Frequency	ABM-3G core Throughput [Mbit/s] (53 Byte Cells)	Speedup relative to STM-4/OC12 (599.04 Mbit/s)
51.84	686.88	1.146

3.2 Functional Block Description

3.2.1 Cell Handler (Upstream/Downstream)

The Cell Handler (CH) units are responsible for the physical data flow of storing and retrieving cells to/from the respective Cell Storage RAM or insertion and extraction of Resource Management (RM) cells. Updates to the cell header section or to the cell contents in case of OAM-RM cells are also performed by the Cell Handler units.

3.2.2 Buffer Manager and Queue Scheduler (Overview)

The Buffer Manager (BM) unit is the central function of the ABM-3G device and handles the logical data flows for upstream and downstream direction. It utilizes the Queue Scheduler to coordinate cell emission and a common Cell Pointer RAM (SSRAM) to administrate cell storage.

Any cell entering the CH unit is reported to the BM unit running the cell acceptance algorithm. In a first step a cell is classified and associated to the logical resource entities connection, queue, traffic class and scheduler. Once all associated resources are determined, the BM runs the cell acceptance algorithm based on the current parameter sets. As a result of all threshold evaluations the cell is either discarded or accepted and related counters are updated accordingly. Non-empty queues are reported to the Queue Scheduler (QS) unit to be scheduled by the associated calendar. In return the QS unit reports queues to the Buffer Manager that are due for cell transmission in the current cell slot. Upon a cell emit request for a specific queue the BM requests the Cell Handler to retrieve and transmit the next cell.

Since the BM and QS units are the central functions of the ABM-3G device they are described in more detail in chapter **"Buffer Manager and Queue Scheduler Details" on Page 60**.

3.2.3 AAL5 Assistant

The AAL5 Assistant unit allows insertion and extraction of AAL5 segmented packets from and towards the Microprocessor Interface. Supported by the corresponding software driver, the unit implements an "in-line" SAR function, i.e. one packet is processed at any time by an SAR function. However, upstream and downstream flow as well as extraction and insertion are independent functions that may be operationally interleaved.

For extraction, a Scheduler Block must be associated to the AAL5 Assistant unit and each queue assigned to this scheduler block must be assigned to a VC-merge group to guarantee that complete packets are forwarded to the AAL5 Assistant unit. The scheduler block rates can be adjusted according to the microprocessor interface bandwidth or the intended CPU load. However, the CPU may extract the payload chunks at a lower rate which will result in internal scheduler block backpressure. No data loss will occur in that case. The CPU reads consecutive bytes from the cell's payload chunks that can be re-assembled immediately in the host memory while the AAL5 Assistant unit checks the AAL5 trailer. The section **"AAL5 Packet Extraction" on Page 121** provides programming details.

Refer to **"Scheduler Configuration Table Integer Transfer Registers" on Page 257** for the assignment of scheduler blocks to the AAL5 Assistant and the programming of their rates.

For insertion, the CPU prepares the ATM cell header for the following packet and writes packet payload chunks to the AAL5 Assistant unit which will generate the cells and the AAL5 trailer for automatic completion of the last cell of the packet. Internally, the cells are forwarded to either the downstream or upstream Cell Handler and processed in the same way as cells received by an UTOPIA receive interface.

The section **"AAL5 Packet Insertion" on Page 121** provides the details.

3.2.4 Internal Address Reduction Unit

The ABM-3G requires an internal 16-bit Local Connection Identifier (LCI) to address its resources. Two basic cell addressing schemes are supported to extract/generate an LCI from the cell header:

- LCI Mapping Modes
  An external device generates an LCI and maps it into the ATM cell header. Three different mapping modes are supported by the ABM-3G.
  The LCI mapping modes are described as part of the UTOPIA interface description in chapters **"UTOPIA L2 Interfaces (PHY side)" on Page 124** and **"UTOPIA L2 Interface (Backplane side)" on Page 134**.
- Internal Address Reduction Mode
  The ABM-3G generates its own internal LCI as a programmable combination of the cell header fields VPI, VCI and the Port Number (PN). The port number is taken either from the UTOPIA port number or the UDF1 cell header byte.

Internal Address Reduction

Two parameters in **Register 111 "MODE2" on Page 315** determine the building function of the internal LCI value:

- PNUM(2:0)
  Determines the number of bits taken from the port number field.
- MNUM(3:0)
  Determines the VCI and VPI ranges depending on the cell header VPI value.

Two translation functions are effective, depending on the cell header VPI(11:0) value compared to the configured parameter MNUM.

In the first case

$$VPI(11,0) < 2^x - 1 \quad ; \text{ with } \left\{ \begin{array}{llll} x = 16 - MNUM & \text{for} & MNUM > 0 \\ x = 0 & \text{for} & MNUM = 0 \end{array} \right\}$$

the LCI is built by {VPI, VCI, PN} values whereas the VCI range is given by (MNUM - PNUM) bits and the VPI range is given by (16 - MNUM) bits.

Note: Programming MNUM(3:0) = 0 is interpreted as decimal 16.

The following tables provide the possible LCI building patterns for all allowed PNUM and MNUM configurations. The resulting LCI is internally treated in the same way as in the LCI cell header mapping modes, i.e. the two MSBs are checked against the quarter segment configuration that allows for cascading of up to four ABM-3G devices.

Note: VPI and VCI cell header field positions that are not mapped into the LCI are checked against '0'. A mismatch is treated as 'invalid LCI' and the cell is discarded.

<table>
<tr><th>PNUM</th><th>MNUM</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td>8</td><td colspan="8">VPI(7:0)</td><td colspan="8">VCI(7:0)</td></tr>
<tr><td>0</td><td>9</td><td colspan="7">VPI(6:0)</td><td colspan="9">VCI(8:0)</td></tr>
<tr><td>0</td><td>10</td><td colspan="6">VPI(5:0)</td><td colspan="10">VCI(9:0)</td></tr>
<tr><td>0</td><td>11</td><td colspan="5">VPI(4:0)</td><td colspan="11">VCI(10:0)</td></tr>
<tr><td>0</td><td>12</td><td colspan="4">VPI(3:0)</td><td colspan="12">VCI(11:0)</td></tr>
<tr><td>1</td><td>9</td><td colspan="7">VPI(6:0)</td><td colspan="8">VCI(7:0)</td><td>PN</td></tr>
<tr><td>1</td><td>10</td><td colspan="6">VPI(5:0)</td><td colspan="9">VCI(8:0)</td><td>PN</td></tr>
<tr><td>1</td><td>11</td><td colspan="5">VPI(4:0)</td><td colspan="10">VCI(9:0)</td><td>PN</td></tr>
<tr><td>1</td><td>12</td><td colspan="4">VPI(3:0)</td><td colspan="11">VCI(10:0)</td><td>PN</td></tr>
<tr><td>1</td><td>13</td><td colspan="3">VPI(2:0)</td><td colspan="12">VCI(11:0)</td><td>PN</td></tr>
<tr><td>1</td><td>14</td><td colspan="2">VPI(1:0)</td><td colspan="13">VCI(12:0)</td><td>PN</td></tr>
<tr><td>1</td><td>15</td><td>VPI</td><td colspan="14">VCI(13:0)</td><td>PN</td></tr>
<tr><td>1</td><td>16</td><td colspan="15">VCI(14:0)</td><td>PN</td></tr>
<tr><td>2</td><td>9</td><td colspan="7">VPI(6:0)</td><td colspan="7">VCI(6:0)</td><td colspan="2">PN(1:0)</td></tr>
<tr><td>2</td><td>10</td><td colspan="6">VPI(5:0)</td><td colspan="8">VCI(7:0)</td><td colspan="2">PN(1:0)</td></tr>
<tr><td>2</td><td>11</td><td colspan="5">VPI(4:0)</td><td colspan="9">VCI(8:0)</td><td colspan="2">PN(1:0)</td></tr>
<tr><td>2</td><td>12</td><td colspan="4">VPI(3:0)</td><td colspan="10">VCI(9:0)</td><td colspan="2">PN(1:0)</td></tr>
<tr><td>2</td><td>13</td><td colspan="3">VPI(2:0)</td><td colspan="11">VCI(10:0)</td><td colspan="2">PN(1:0)</td></tr>
<tr><td>2</td><td>14</td><td colspan="2">VPI(1:0)</td><td colspan="12">VCI(11:0)</td><td colspan="2">PN(1:0)</td></tr>
<tr><td>2</td><td>15</td><td>VPI</td><td colspan="13">VCI(12:0)</td><td colspan="2">PN(1:0)</td></tr>
<tr><td>2</td><td>16</td><td colspan="14">VCI(13:0)</td><td colspan="2">PN(1:0)</td></tr>
<tr><td>3</td><td>10</td><td colspan="6">VPI(5:0)</td><td colspan="7">VCI(6:0)</td><td colspan="3">PN(2:0)</td></tr>
<tr><td>3</td><td>11</td><td colspan="5">VPI(4:0)</td><td colspan="8">VCI(7:0)</td><td colspan="3">PN(2:0)</td></tr>
<tr><td>3</td><td>12</td><td colspan="4">VPI(3:0)</td><td colspan="9">VCI(8:0)</td><td colspan="3">PN(2:0)</td></tr>
<tr><td>3</td><td>13</td><td colspan="3">VPI(2:0)</td><td colspan="10">VCI(9:0)</td><td colspan="3">PN(2:0)</td></tr>
<tr><td>3</td><td>14</td><td colspan="2">VPI(1:0)</td><td colspan="11">VCI(10:0)</td><td colspan="3">PN(2:0)</td></tr>
<tr><td>3</td><td>15</td><td>VPI</td><td colspan="12">VCI(11:0)</td><td colspan="3">PN(2:0)</td></tr>
<tr><td>3</td><td>16</td><td colspan="13">VCI(12:0)</td><td colspan="3">PN(2:0)</td></tr>
<tr><td>4</td><td>10</td><td colspan="6">VPI(5:0)</td><td colspan="6">VCI(5:0)</td><td colspan="4">PN(3:0)</td></tr>
<tr><td>4</td><td>11</td><td colspan="5">VPI(4:0)</td><td colspan="7">VCI(6:0)</td><td colspan="4">PN(3:0)</td></tr>
<tr><td>4</td><td>12</td><td colspan="4">VPI(3:0)</td><td colspan="8">VCI(7:0)</td><td colspan="4">PN(3:0)</td></tr>
<tr><td>4</td><td>13</td><td colspan="3">VPI(2:0)</td><td colspan="9">VCI(8:0)</td><td colspan="4">PN(3:0)</td></tr>
<tr><td>4</td><td>14</td><td colspan="2">VPI(1:0)</td><td colspan="10">VCI(9:0)</td><td colspan="4">PN(3:0)</td></tr>
<tr><td>4</td><td>15</td><td>VPI</td><td colspan="11">VCI(10:0)</td><td colspan="4">PN(3:0)</td></tr>
<tr><td>4</td><td>16</td><td colspan="12">VCI(11:0)</td><td colspan="4">PN(3:0)</td></tr>
<tr><td>5</td><td>11</td><td colspan="5">VPI(4:0)</td><td colspan="6">VCI(5:0)</td><td colspan="5">PN(4:0)</td></tr>
<tr><td>5</td><td>12</td><td colspan="4">VPI(3:0)</td><td colspan="7">VCI(6:0)</td><td colspan="5">PN(4:0)</td></tr>
<tr><td>5</td><td>13</td><td colspan="3">VPI(2:0)</td><td colspan="8">VCI(7:0)</td><td colspan="5">PN(4:0)</td></tr>
<tr><td>5</td><td>14</td><td colspan="2">VPI(1:0)</td><td colspan="9">VCI(8:0)</td><td colspan="5">PN(4:0)</td></tr>
<tr><td>5</td><td>15</td><td>VPI</td><td colspan="10">VCI(9:0)</td><td colspan="5">PN(4:0)</td></tr>
<tr><td>5</td><td>16</td><td colspan="11">VCI(10:0)</td><td colspan="5">PN(4:0)</td></tr>
<tr><td>6</td><td>12</td><td colspan="4">VPI(3:0)</td><td colspan="6">VCI(5:0)</td><td colspan="6">PN(5:0)</td></tr>
<tr><td>6</td><td>13</td><td colspan="3">VPI(2:0)</td><td colspan="7">VCI(6:0)</td><td colspan="6">PN(5:0)</td></tr>
<tr><td>6</td><td>14</td><td colspan="2">VPI(1:0)</td><td colspan="8">VCI(7:0)</td><td colspan="6">PN(5:0)</td></tr>
<tr><td>6</td><td>15</td><td>VPI</td><td colspan="9">VCI(8:0)</td><td colspan="6">PN(5:0)</td></tr>
<tr><td>6</td><td>16</td><td colspan="10">VCI(9:0)</td><td colspan="6">PN(5:0)</td></tr>
<tr><td>7</td><td>13</td><td colspan="3">VPI(2:0)</td><td colspan="6">VCI(5:0)</td><td colspan="7">PN(6:0)</td></tr>
<tr><td>7</td><td>14</td><td colspan="2">VPI(1:0)</td><td colspan="7">VCI(6:0)</td><td colspan="7">PN(6:0)</td></tr>
<tr><td>7</td><td>15</td><td>VPI</td><td colspan="8">VCI(7:0)</td><td colspan="7">PN(6:0)</td></tr>
<tr><td>7</td><td>16</td><td colspan="9">VCI(8:0)</td><td colspan="7">PN(6:0)</td></tr>
</table>

Figure 3-5 LCI Building Patterns

In the second case

$$VPI(11,0) \geq 2^{x} - 1 \quad ; \text{with} \begin{Bmatrix} x = 16 - MNUM & \text{for} & MNUM > 0 \\ x = 0 & \text{for} & MNUM = 0 \end{Bmatrix}$$

the LCI is built by {VPI, PN} values only whereas the VPI range is given by MNUM bits.

Note: Programming MNUM(3:0) = 0 is interpreted as decimal 16.

The following tables provide the possible LCI building patterns for all PNUM and MNUM configurations. The resulting LCI is internally treated in the same way as in the LCI cell header mapping modes, i.e. the two MSBs are checked against the quarter segment configuration that allows for cascading of up to four ABM-3G devices.

Note: VPI cell header field positions that are not mapped into the LCI are checked against ‘0’. A mismatch is treated as ‘invalid LCI’ and the cell is discarded.

Note: When QS check is enabled (for cascaded ABM-3Gs), the transparent VPCs are handled by the ABM-3G with QS=11b. See **Register 111 "MODE2" on Page 315**.

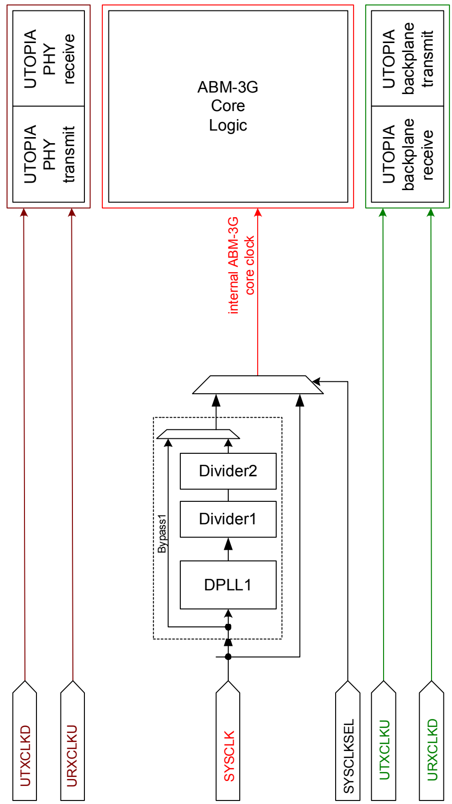
PNUM	MNUM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	8	1	1	1	1	1	1	1	1	VPI(7:0)							
0	9	1	1	1	1	1	1	1	VPI(8:0)								
0	10	1	1	1	1	1	1	VPI(9:0)									
0	11	1	1	1	1	1	VPI(10:0)										
0	12	1	1	1	1	VPI(11:0)											
1	9	1	1	1	1	1	1	1	VPI(7:0)								PN
1	10	1	1	1	1	1	1	VPI(8:0)									PN
1	11	1	1	1	1	1	VPI(9:0)										PN
1	12	1	1	1	1	VPI(10:0)											PN
1	13	1	1	1	VPI(11:0)												PN
1	14	1	1	VPI(12:0)													PN
1	15	1	VPI(13:0)														PN
1	16	VPI(14:0)															PN
2	9	1	1	1	1	1	1	1	VPI(6:0)							PN(1:0)	
2	10	1	1	1	1	1	1	VPI(7:0)								PN(1:0)	
2	11	1	1	1	1	1	VPI(8:0)									PN(1:0)	
2	12	1	1	1	1	VPI(9:0)										PN(1:0)	
2	13	1	1	1	VPI(10:0)											PN(1:0)	
2	14	1	1	VPI(11:0)												PN(1:0)	
2	15	1	VPI(12:0)													PN(1:0)	
2	16	VPI(13:0)														PN(1:0)	
3	10	1	1	1	1	1	1	VPI(6:0)							PN(2:0)		
3	11	1	1	1	1	1	VPI(7:0)								PN(2:0)		
3	12	1	1	1	1	VPI(8:0)									PN(2:0)		
3	13	1	1	1	VPI(9:0)										PN(2:0)		
3	14	1	1	VPI(10:0)											PN(2:0)		
3	15	1	VPI(11:0)												PN(2:0)		
3	16	VPI(12:0)													PN(2:0)		
4	10	1	1	1	1	1	1	VPI(5:0)						PN(3:0)			
4	11	1	1	1	1	1	VPI(6:0)							PN(3:0)			
4	12	1	1	1	1	VPI(7:0)								PN(3:0)			
4	13	1	1	1	VPI(8:0)									PN(3:0)			
4	14	1	1	VPI(9:0)										PN(3:0)			
4	15	1	VPI(10:0)											PN(3:0)			
4	16	VPI(11:0)												PN(3:0)			
5	11	1	1	1	1	1	VPI(5:0)						PN(4:0)				
5	12	1	1	1	1	VPI(6:0)							PN(4:0)				
5	13	1	1	1	VPI(7:0)								PN(4:0)				
5	14	1	1	VPI(8:0)									PN(4:0)				
5	15	1	VPI(9:0)										PN(4:0)				
5	16	VPI(10:0)											PN(4:0)				
6	12	1	1	1	1	VPI(5:0)						PN(5:0)					
6	13	1	1	1	VPI(6:0)							PN(5:0)					
6	14	1	1	VPI(7:0)								PN(5:0)					
6	15	1	VPI(8:0)									PN(5:0)					
6	16	VPI(9:0)										PN(5:0)					
7	13	1	1	1	VPI(5:0)						PN(6:0)						
7	14	1	1	VPI(6:0)							PN(6:0)						
7	15	1	VPI(7:0)								PN(6:0)						
7	16	VPI(8:0)									PN(6:0)						

Figure 3-6 LCI Building Patterns (VPI only)

3.2.5 Clocking System

The clocking system of the ABM-3G distinguishes the core clock and the UTOPIA Interfaces whereas each UTOPIA Interface and direction (transmit/receive) is clocked independently, as shown in **Figure 3-7**.

3.2.5.1 Clocking System Overview



Note:
Testmodes are not illustrated in this figure.

Figure 3-7 Clocking System Overview

3.2.5.2 DPLL Programming

The DPLL features two factors programmed by parameters **m** and **n** in register **"PLL1CONF" on Page 287** :

$$f_1 = f_{in}/(m+1) \quad ; \quad f_2 = f_{in} \times \frac{n+1}{m+1}$$

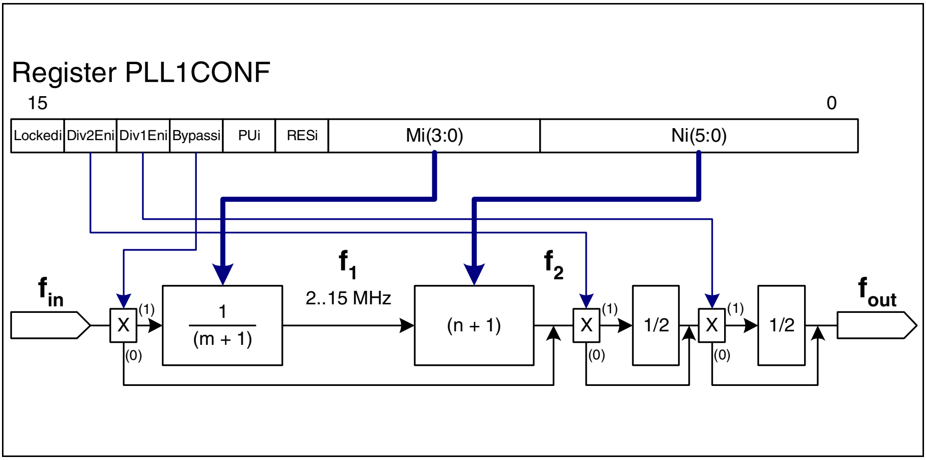


Figure 3-8 DPLL Structure

The division factor determined by **m** must be chosen such that intermediate frequency f_1 is in the range 2..15 MHz based on the input frequency at signal 'SYSCLK'.

The multiplication factor determined by **n** must be chosen such that intermediate frequency f_2 is twice or four times the final value in case of DPLL1.

Finally, one or two divisions by the two factors (f_1,f_2) may be enabled in case of DPLL1 to achieve the final clock frequency.

When choosing the factors **m** and **n**, two conditions must be met:

- n=1..24: f_1 must be in a range of 5..15 MHz
  n=25..63: f_1 must be in a range of 2..6 MHz
- f_2 must be in a range of 100 to 200 MHz

3.2.5.3 Programming Example

The following numbers are assumed for this example:

- ABM-3G internal core clock: 52 MHz

- Clock supply: 52 MHz at signal SYSCLK

In this example, signal SYSCLKSEL must be connected to V_{SS} to connect the internal core clock to the DPLL1 output. (Please refer to **Figure 3-7**)

DPLL1 Programming

A reasonable value for parameter M1 in register **"PLL1CONF" on Page 287** is M1 = 12 which results in
f_1 = 52 MHz / (12 + 1) = 4 MHz.

Now a possible value for parameter N1 is N1 = 25 which results in

f_2 = 4 MHz * (25 + 1) = 104 MHz.

To achieve the 52 MHz core clock division factor 1 shall be enabled.

Thus, for this example the value $3B19_H$ must be programmed to register PLL1CONF.

The conditions given above are met because f_1=4 MHz is in the range of 2..6 MHz (n=25) and f_2=104 MHz is between 100 and 200 MHz.

Note: Multiple combinations of parameters are possible to achieve a 52 MHz clock in this example.

3.2.5.4 Initialization Phase

After power-on reset, the DPLL is in bypass mode which means that signal 'SYSCLK' is directly feeding the internal core clock. After basic configuration of at least the DPLL configuration registers, the bypass can be disabled which will make a glitch-free adjustment of the internal clocks to the selected frequency.

3.2.6 Reset System

The ABM-3G provides three different reset sources, as shown in **Figure 3-9**. The hardware signal $\overline{\text{RESET}}$ affects the entire device. The self-clearing software reset bit 'SWRES' in register **"MODE1" on Page 312** also affects the entire device.

Hardware reset as well as software reset bit 'SWRES' completely initialize the device into power-on reset state.

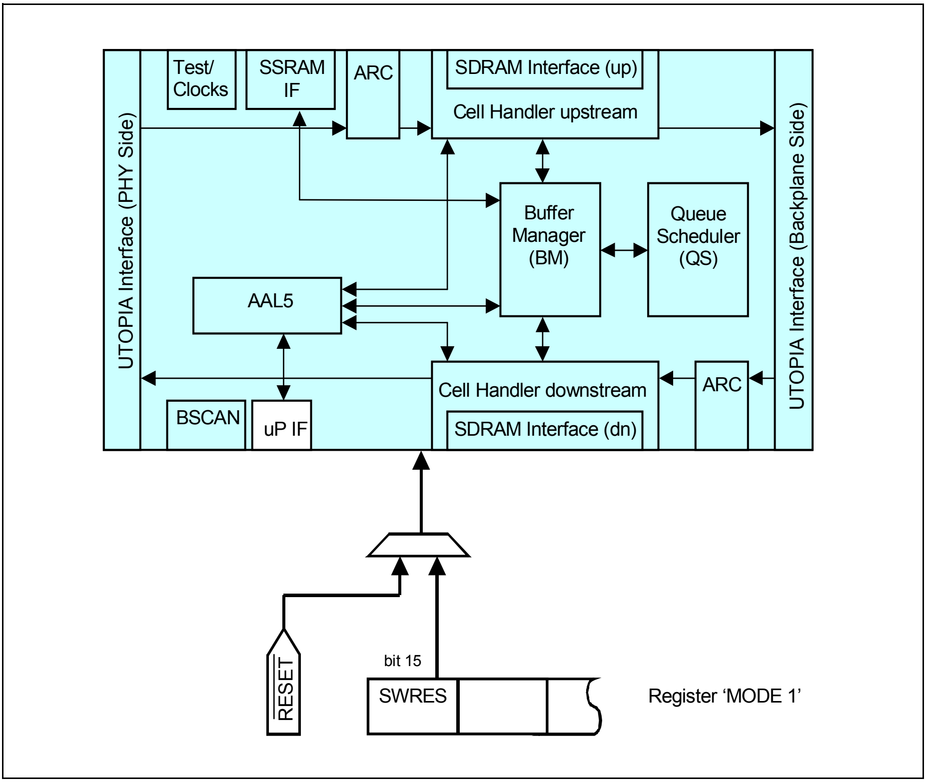


Figure 3-9 Reset System Overview

Note: Initialization of external and internal RAM must be started by software via command bits 'INITRAM' and 'INITSDRAM' in register **"MODE1" on Page 312** following the device reset.

3.3 System Integration

The ABM-3G has two operational modes: Bi-directional mode and Uni-directional mode. The directional terminology for the modes refers to the usage of the ABM-3G cores, not to the connections. The connections are bi-directional in all cases. In Bi-directional mode, one ABM-3G core is used exclusively for the cells of a connection in the upstream direction and the other core exclusively handles cells of the same connection in the downstream direction. In Uni-directional mode, only one core always will be used to handle the cells of a connection both in up- and downstream direction. The two basic applications for these modes are the switch port line card application and the mini-switch, respectively.

On a typical switch port line card, both the upstream and downstream cell flow pass through the same ABM-3G device. One ABM-3G core is used for each direction as shown in **Figure 3-10**.

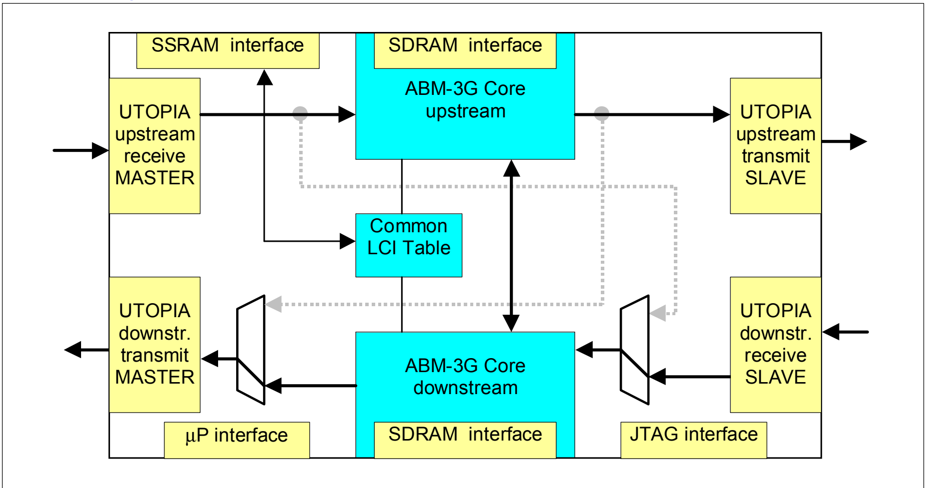


Figure 3-10 ABM-3G in Bi-directional Mode

The ABM-3G assumes that all connections are set up bi-directionally with the same Local Connection Identifier (LCI) in both directions. In the Infineon ATM chip set environment, the LCI is provided by the PXB 4350 E ALP and contains VPI, VCI, and PHY information. If the ABM-3G is not used with the ALP, it can extract the LCI from VPI or VCI fields or generate the LCI by using the internal Address Reduction Circuit (ARC).

In a mini-switch application, the total throughput at 51.84 MHz is 687 Mbit/s. Only the UTOPIA Receive and Transmit interfaces at the PHY-side are active. Both ABM-3G cores are selected from the multiplexer options shown in **Figure 3-11**. Each cell is forwarded to both ABM-3G cores and the LCI table entry for the connection determines which of the two cores accepts the cell. The other core ignores it. Thus, each cell is stored and queued in one of the two cores. The cell streams of both cores are multiplexed together at the output. In normal operation, the schedulers are programmed such that the sum of all output rates does not exceed the maximum rate supported by the UTOPIA transmit interface. However, bandwidth overbooking of the interface is also possible, resulting in backpressure towards the respective ABM-3G core.

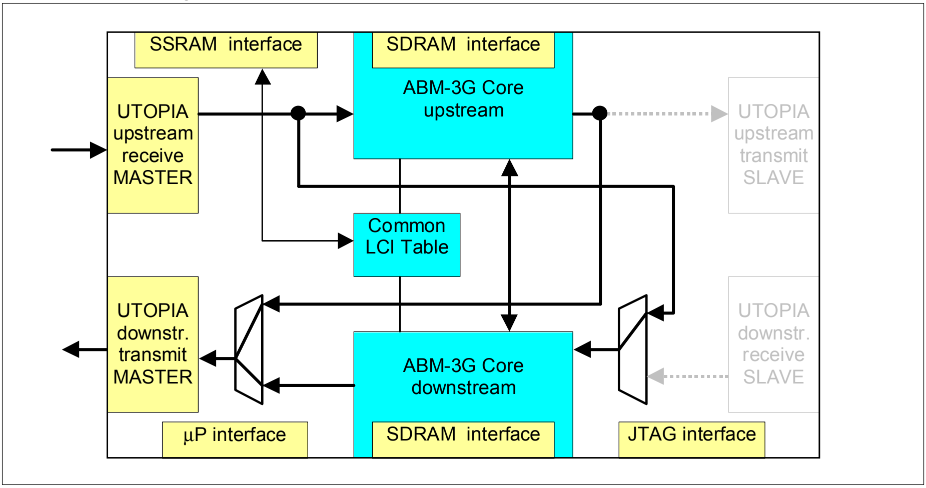


Figure 3-11 ABM-3G in Uni-directional Mode Using both Cores

If the resources of one core are sufficient, the downstream core can be deactivated (see Figure 3-12). This reduces power consumption and allows omission of the external downstream SDRAM. It also permits the SSRAM to be smaller (see below).

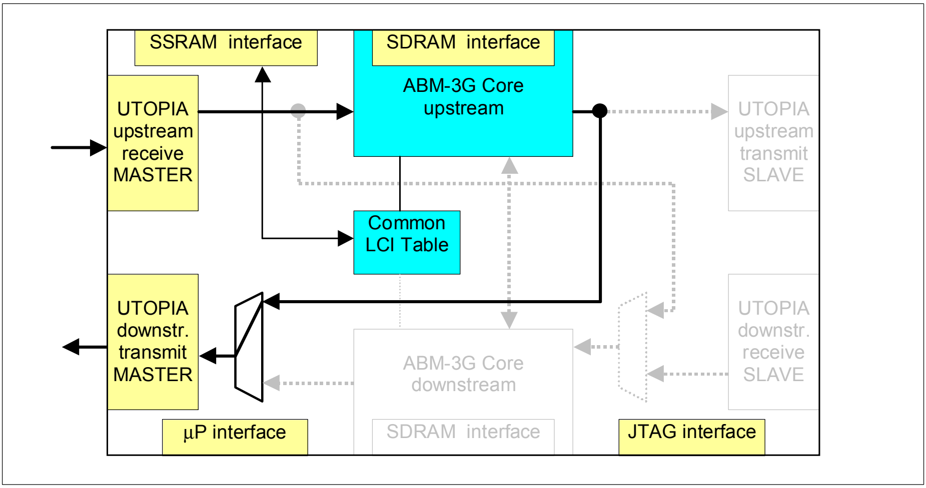


Figure 3-12 ABM-3G in Uni-directional Mode Using one Core

3.3.1 LCI Translation in Mini-Switch Configurations

In Uni-directional applications, the ABM-3G can be programmed to make a minimum header translation. This is necessary in a Mini-Switch configuration as both the forward and backward direction of a connection traverse the devices in the same direction. The OAM functions in the Infineon ALP (PXB 4350) or AOP (PXB 4340) devices need the same LCI for forward and backward direction of a connection.

This is clarified by the example shown in **Figure 3-13** in which a connection is set up from PHY_1 to PHY_2. VPI/VCI_1 is the identifier on the transmission line where PHY_1 is connected. The terminal sends ATM cells with this identifier and expects cells in the backward direction from PHY_2 with the same identifier. The ALP in the upstream direction translates VPI/VCI_1 into LCI_1, the unique local identifier for this connection in the upstream direction. Similarly, for the backward connection from PHY_2 to PHY_1, the ALP receives ATM cells from PHY_2 with the identifier VPI/VCI_2 and translates them into LCI_2.

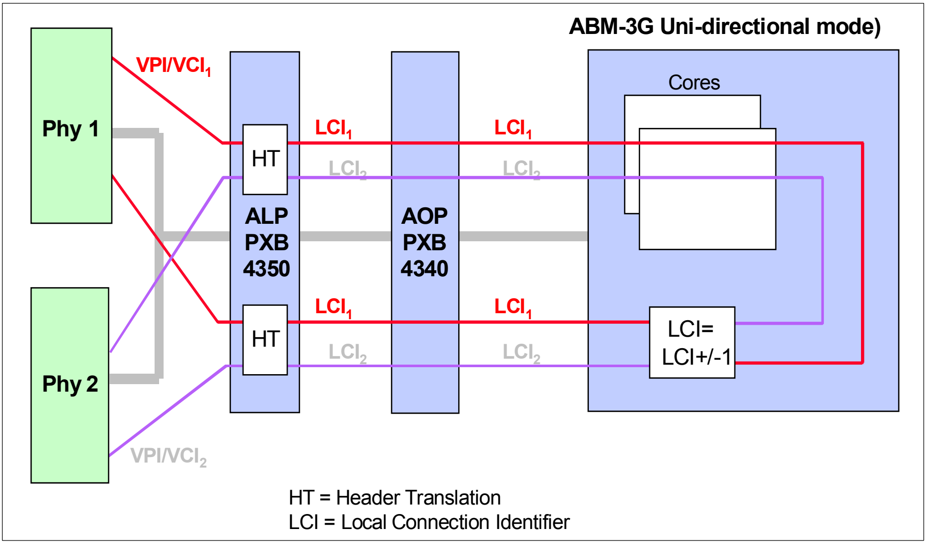


Figure 3-13 Connection Identifiers in Mini-Switch Configuration

For minimum complexity, the header translation of the ABM-3G is done by inverting the Least Significant Bit (LSB) of the LCI. This measure divides the available LCI range into two parts: odd LCI values for forward connections and even LCI values for backward connections (or vice-versa). That is, it reduces the available number of connection identifiers to 8192, because two LCI values are used per connection.

This is not a restriction in the case of arbitrary address reduction modes as, for example, when the ALP chip is used with the CAME chip (PXB 4360), as ATM connections are always set up bi-directionally with the same VPI/VCI in both directions of a link.

Refer to **Register 110 "MODE1" on Page 312** for the configuration of the bi-directional and uni-directional mode, the enabling of the LCI toggling, as well as the deactivation of the downstream core.

Note: In case of fixed address reduction, as, for example, when using the ALP with the built-in Address Reduction Circuit (ARC), the usable LCI range may be seriously restricted, depending on the PHY configuration.

3.4 Buffer Manager and Queue Scheduler Details

This section provides more detailed information about buffering (cell acceptance) and scheduling (cell emission) functions.

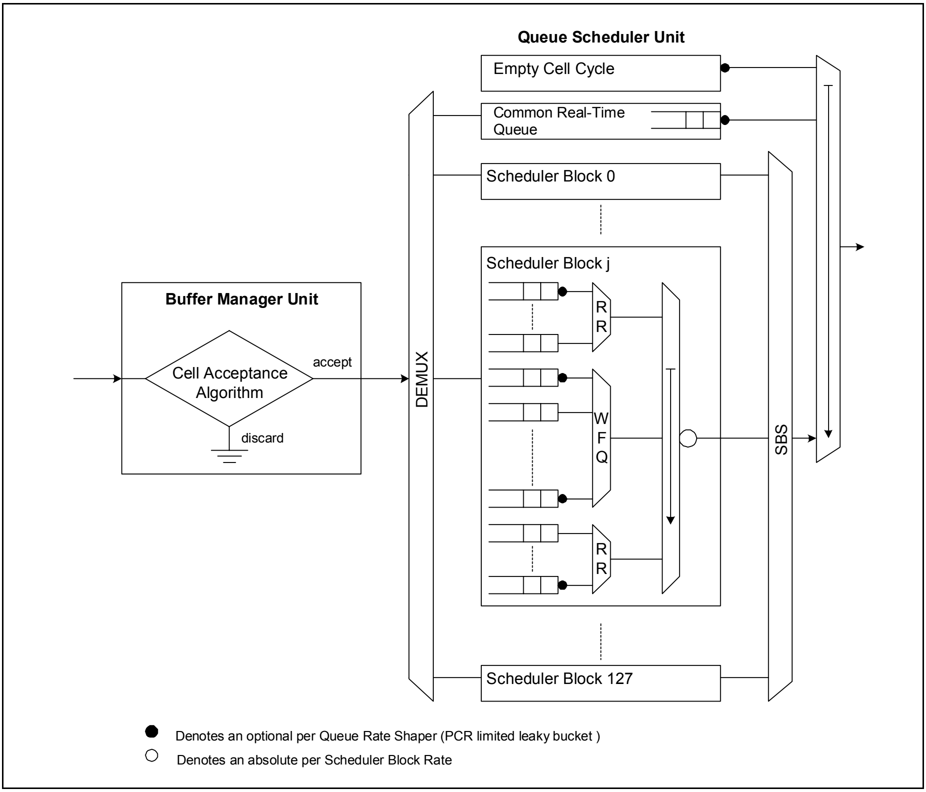


Figure 3-14 Cell Acceptance and Scheduling

3.4.1 Buffer Manager

3.4.1.1 Functional Overview

The basic function of the Buffer Manager (BM) is to decide whether an arriving cell is granted access to the shared buffer or is discarded. This is done by running the Cell Acceptance Algorithm (CAA) (see **Chapter 3.4.1.7**). The buffer manager tables accessed by the CAA are summarized in **Figure 3-15**.

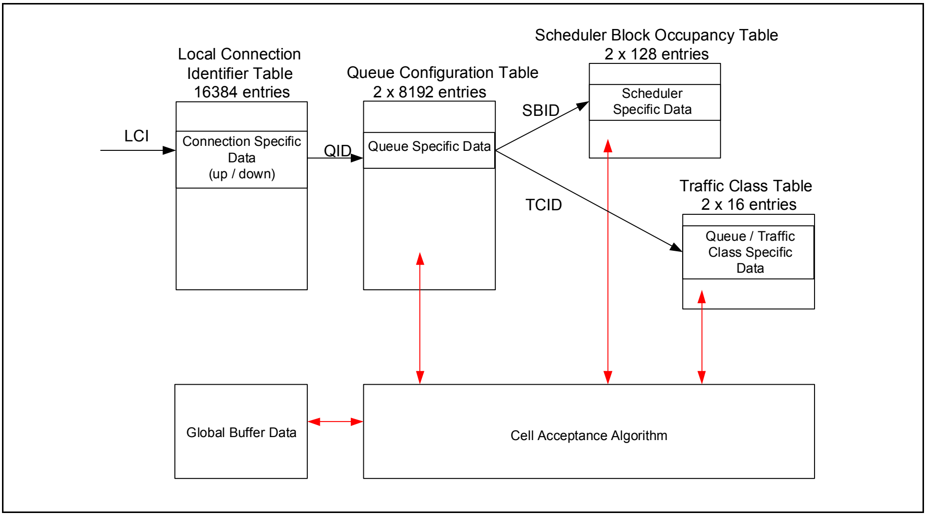


Figure 3-15 Buffer Manager Tables

More generally, the buffer manager allocates the buffer resources needed to fulfill the specific service guarantees of individual connections.

In a first step when receiving a cell, the Local Connection Identifier (LCI) that was previously assigned by the Header Translation (see **Figure 3-13**), is mapped to a corresponding Queue Identifier (QID). The QID represents the logical queue in which the cell will be stored upon acceptance and serves as an index for subsequent table lookups. In particular, the Scheduler Block and the Traffic Class of the received cell is identified with the Scheduler Block Identifier (SBID) and the Traffic Class Identifier (TCID) respectively.

With any incoming cell, the Cell Acceptance Algorithm (CAA) can access the current buffer status information containing counters, thresholds and flags. Based on this data, the cell is either discarded or accepted. The respective counters are updated appropriately.

Under normal operation conditions, once a cell is accepted by the CAA, it will be emitted at a time. The only reason for cell discard after cell acceptance is queue disabling. The cell itself is stored in the external cell store RAM. The logical queue is a linked list of pointers to the cell store RAM providing a FIFO ordering.

3.4.1.2 Logical Buffer Views

The ABM-3G Cell Buffer is structured by the Buffer Manager into the following major logical views:

- Global Buffer,
- Logical Queues,
- Scheduler Blocks,
- Traffic Classes.

Each view is characterized by attributes, state variables (e.g. occupancy counters), and programmable thresholds.

3.4.1.2.1 Global Buffer

A total amount of 262,140 cells can be stored per direction in the global cell buffer. Depending on the particular threshold configuration, global buffer space can be exclusively reserved or shared among different logical queues, scheduler blocks or traffic classes and the individual connections assigned to them.

3.4.1.2.2 Logical Queues

The concept of logical queues is implemented to provide isolation between connections or groups of connections sharing the global buffer. Strict per VC queueing is achieved by exclusively assigning connections to logical queues. However, it is also possible to assign more than one connection to a particular logical queue.

A total of 8192 logical queues is provided per direction, with QIDs ranging from 0 to 8191. QID 0 is reserved for the common real-time (CRT) bypass queue. It may be used for real-time traffic in case of an unstructured ABM-3G output, as e.g. in input buffered switches and also for cascading multiple ABM-3Gs. The common real-time bypass is programmed as a rate limited queue. **Section 3.4.2.1** provides scheduling related details.

3.4.1.2.3 Scheduler Blocks

From a buffer manager perspective, Scheduler Blocks (SB) can be conceived as a grouping of logical queues sharing the bandwidth provided by the configured SB rate. Each logical queue, except the common real-time (CRT) bypass (QID=0), is unambiguously assigned to a scheduler block.

A total of 128 Scheduler Blocks is provided per direction.

Scheduler Blocks are usually assigned to ports, logical channels, or limited terminated VPCs, providing the necessary rate adaptation. **Section 3.4.3** provides the details.

SB occupancy thresholds are provided for buffer protection in case of SB overload.

3.4.1.2.4 Traffic Classes

The concept of traffic classes is introduced to provide a logical grouping of queues with common properties, defined by a set of parameters. Each logical queue is unambiguously assigned to a traffic class and inherits the thresholds and flags defined therein.

The Buffer Manager supports up to 16 distinct parameter sets for traffic classes in the Traffic Class Table (TCT). Each parameter set includes thresholds and flags as listed in **Chapter 3.4.1.3**.

Figure 3-16 shows the independent assignment connections to queues and of queues to traffic classes and schedulers.

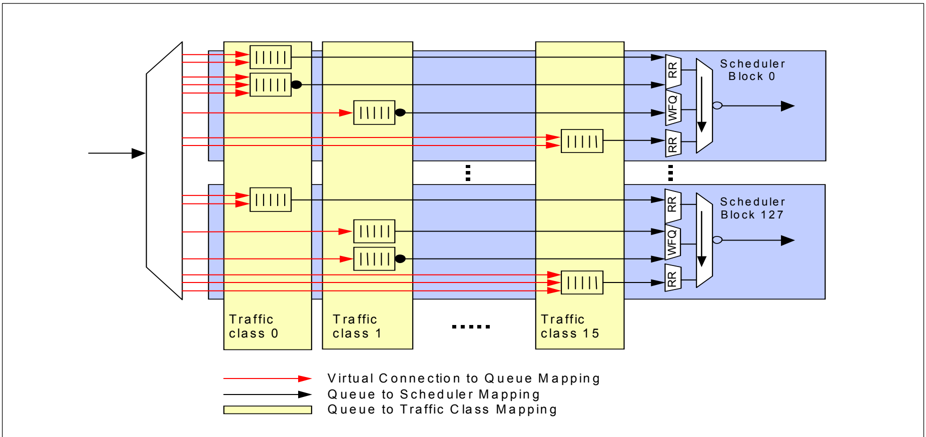


Figure 3-16 Queue Assignment to Traffic Classes and Scheduler Blocks

Traffic classes are the principal buffer management concept for Quality of Service (QoS) differentiation. They are not pre-defined or fixed to the standard ATM service categories. This allows for configuration of generic or new services (e.g. DiffServ Per Hop Behaviors (PHB) as defined by the IETF). Along with the queue scheduler concept of scheduler blocks (see **Section 3.4.2.2**), a wide range of QoS objectives can be met.

3.4.1.3 Threshold Classification

The different threshold types are listed in **Table 3-17**. In this section, each classification includes a short description.

3.4.1.3.1 Discard Thresholds

Discard thresholds are used by the Cell Acceptance Algorithm (see **Chapter 3.4.1.7**). The CAA is invoked every time a cell arrives and calculates a truth value from individual discard conditions.

A discard condition is an expression involving thresholds, counters, flags, parameters, and state variables that renders a truth value as result. Several basic discard conditions can be combined to implement more advanced discard mechanisms (see **Chapter 3.4.1.6**).

Basic Discard Conditions

The simplest discard condition is the comparison of an occupancy counter with a threshold. A common classification of discard conditions includes:

- Maximum
  A discard condition is classified as Maximum Fill if it is independent of the CLP transparency flag or if the CLP transparency flag is set to 1.
- CLP1
  A discard condition is classified as CLP1 if it is dependent on the setting of the CLP transparency flag to 0.
- Packet
  A discard condition refers to a packet if it is dependent on the setting of EPDen = 1 or PPDen = 1.

A particular threshold can participate in several discard conditions. In the ABM-3G, it is quite common to use a threshold in both maximum fill and packet discard conditions. Refer to **Table 3-17**.

Discard Control Parameters

Besides the simple comparison of a threshold value to a counter, several flags and variables are combined to provide more complex discard conditions.

- CLP1DIS
  CLP1 thresholds are only enabled if the number of CLP1 cells in the SB, counted by SBOccLP is greater or equal to CLP1DIS. To enable CLP1 thresholds unconditionally, this threshold must be set to 0 in **Register 19 "CLP1DIS" on Page 180**.
- MinBG
  This queue-specific threshold disables discard when the QueueLength counter is lower than MinBG. The description of the minimum buffer guarantee in **Section 3.4.1.6.4** provides the details.

- DH
  Delta Hysteresis is a traffic class specific factor applied to all maximum thresholds. The description of the hysteresis mechanism in **Section 3.4.1.6.5** provides the details.

3.4.1.3.2 Backpressure Thresholds

- UTOPIA Backpressure Thresholds
  These thresholds (four in upstream and four in downstream direction) are global thresholds with respect to the cell buffer fill level and result in backpressure of specific port groups of the respective UTOPIA receive interface.

3.4.1.4 Counter Classification

The ABM-3G Buffer Manager contains the following counter types

- Occupancy Counters
  These counters reflect the current buffer state and are basic elements in discard, congestion indication and backpressure mechanisms.
- Statistics Counters
  These counters are used for measurements and statistics. Refer also to **Chapter 3.4.1.8**.

3.4.1.5 Threshold and Occupancy Counter Overview

Table 3-17 summarizes thresholds and occupancy counters used by the Cell Acceptance Algorithm. The thresholds are grouped by logical buffer view. For each arriving cell, all conditions in this table are checked. Several thresholds may be exceeded at the same time. Therefore, the table is not a truth table.

Table 3-17 Threshold and Counter Table

Logical Buffer View	Location	Threshold	Related Occupancy Counter	Threshold Type	Granularity	TCT3 Enabling Flags				LCI Table	CRT Queue	Affected Cells
						EPDen	PPDen	GFRen	DH	CLPT		CLP
Global Buffer	Reg 16	BufMax	BufferOcc	Maximum	4	x	x	x	n	x	x	x
				PPD	4	x	1	x	n	x	x	0/1
	TCT0	BufMaxNg	BufferOccNg	Maximum	1024	x	x	x	y	x	x	0/1
				PPD [1)]	1024	x	1	x	n	x	x	0/1
	TCT0	BufEPDNg	BufferOccNg	EPD	1024	1	x	0	n	x	x	0/1
				GFR	1024	1	x	1	n	x	x	0/1
	TCT1	BufCiCLP1	BufferOccNg	CLP1	1024	0	x	x	n	0	x	1
				PPD	1024	0	1	x	n	0	x	1
				EPD	1024	1	x	x	n	0	x	1
	Reg 21	UBTH0	BufferOccNg	UTOPIA backpressure	4	x	x	x	n	x	x	x
	Reg 22	UBTH1			4	x	x	x	n	x	x	x
	Reg 23	UBTH2			4	x	x	x	n	x	x	x
	Reg 24	UBTH3			4	x	x	x	n	x	x	x
Scheduler Block	TCT3	SBMax	SBOccNg	Maximum	1024	0	x	x	y	0	0	0/1
				PPD	1024	0	1	x	n	x	0	0/1
				EPD	1024	1	x	0	n	x	0	0/1
				GFR	1024	1	x	1	n	x	0	0/1
	TCT2	SBCiCLP1	SBOccNg	CLP1	64	0	x	x	n	0	0	1
				PPD	64	0	1	x	n	x	0	1
				EPD	64	1	x	x	n	x	0	1
	Reg 19	CLP1DIS	SBOccLP	Reservation	64	x	x	x	n	x	0	1
Traffic Class	TCT3	TrafClassMax	TrafClassOccNg	Maximum	1024	0	x	x	y	x	x	0/1
				PPD	1024	0	1	x	n	x	x	0/1
				EPD	1024	1	x	0	n	x	x	0/1
				GFR	1024	1	x	1	n	x	x	0/1

Table 3-17 Threshold and Counter Table

Logical Buffer View	Location	Threshold	Related Occupancy Counter	Threshold Type	Granularity	TCT3 Enabling Flags				LCI Table	CRT Queue	Affected Cells
						EPDen	PPDen	GFRen	DH	CLPT		CLP
Queue	Fixed	QueueLimit (16383)	QueueLength	Maximum	1	x	x	x	n	x	x	0/1
				PPD	1	x	1	x	n	x	x	0/1
	TCT1	QueueMax	QueueLength	Maximum	64	0	x	x	y	x	x	0/1
				PPD	64	0	1	x	n	x	x	0/1
				EPD	64	1	x	x	n	x	x	0/1
				GFR	64	1	x	1	n	x	x	0/1
	TCT0	QueueCiCLP1	QueueLength	CLP1	4	0	x	x	n	0	x	1
				PPD	4	0	1	x	n	x	x	1
				EPD	4	1	x	x	n	1	x	1
	QCT2	MinBG	QueueLength	Reservation	1, 8	x	x	x	n	x	x	0/1

1) Not a true PPD threshold because the last cell of the packet is also discarded when BufMaxNg is exceeded.

Note: The flags in columns "TCT3 enabling flags" indicate the traffic class settings required to make the threshold effective during cell acceptance algorithm for a cell (connection) determined to belong to that traffic class. An 'x' means don't care, i.e. the flag has no effect on the threshold. The same applies to flag "CLPT" which is a connection specific setting in the LCI table. The column "affected cells" indicates whether the threshold affects CLP0, CLP1 or all cells.

Note: The thresholds and counters shown above are available in both the upstream and the downstream ABM-3G core. In case of registers, the variable name is prefixed with U for upstream and D for downstream in the register tables of **Chapter 7**.

3.4.1.6 Discard Mechanisms and Buffer Reservation

Each arriving cell is classified by determination of its QID, SBID, and TCID.

The discard mechanisms available in the ABM-3G Buffer Manager are based on occupancy counters and the programmable thresholds described in **Chapter 3.4.1.3** and **Chapter 3.4.1.4**.

3.4.1.6.1 Maximum Fill Discard

A maximum fill discard occurs if the cell counter exceeds the related maximum fill threshold at cell arrival.

The following maximum fill thresholds are available:

BufMax, and QueueLimit are determined by physical limits.

BufMaxNg, SBMax, TrafClassMax, QueueMax are configured per traffic class.

3.4.1.6.2 Selective CLP1 Discard

Selective discard is based on the CLP marking found in the arriving cells and is enabled by the CLP transparency flag (CLPT) stored per connection in the LCI table.

In cell discard mode, the mechanism triggers tail drop for CLP=1 cells only. In this mode, the mechanism is used to limit the buffer space provided for the non-guaranteed part of VBR.2/.3 traffic.

In packet discard mode, the mechanism triggers EPD for CLP=1 frames only. According to the GFR conformance definition, a CLP1 frame is assumed when the first cell of the frame is a CLP1 cell. In this mode, the mechanism is used mainly for the GFR service.

The following discard thresholds are available to control selective CLP1 discard:

BufCiCLP1, SBCiCLP1, QueueCiCLP1.

Note: There is no selective CLP1 discard threshold available for the traffic class view.

3.4.1.6.3 Packet Discard

Packet discard mechanisms rely on the AAL5 End Of Packet (EOP) indication in the PTI field of the cell header. The ABM-3G implements two packet discard mechanisms:

- Early Packet Discard (EPD)
- Partial Packet Discard (PPD).

Packet discard can be enabled individually per traffic class by setting the flags EPDen and PPDen in the TCT respectively. The dynamic status of an ongoing packet discard is stored per connection in the fields LastCellOfPacket, DiscardPacket and DiscardRestOf-Packet in the LCI table.

Both mechanisms are provided to avoid or reduce the volume in the transmission of corrupted packets and therefore improve utilization of buffer and bandwidth resources.

Early Packet Discard (EPD)

The Early Packet Discard (EPD) mechanism drops all cells of a packet if it decides to drop the first cell of that packet. In packet discard mode, if at cell arrival the related cell counter exceeds this threshold, and the flag LastCellOfPacket is enabled in the LCI table, indicating that the arriving cell is the first cell of a packet, then the cell is discarded and the flag DiscardPacket is enabled in the LCI table. All subsequently arriving cells of the packet are discarded without taking into consideration the cell counter.

EPD may only be applied to non real-time connections. The mechanism is enabled by the software configurable flag EPDen, specified per traffic class in the TCT.

The Buffer Manager attempts not to corrupt a packet, once it has accepted the first cell. This means that for EPDen=1, the maximum thresholds TrafClassMax, SBMax and QueueMax are disabled for the rest of the packet. Only the thresholds BufMax, BufMaxNg and QueueLimit can corrupt an accepted packet.

Partial Packet Discard (PPD)

Under the rare circumstances described at the end of the previous section, it may happen that a cell is discarded from within a packet although the EPD algorithm has accepted it. In this case it is meaningful to discard also all following cells of the packet. However, the last cell of a partially discarded packet should be buffered if possible, since the reassemble mechanism at the receiver is triggered by the last cells of user data packets. This mechanism is referred to as Partial Packet Discard (PPD).

In packet discard mode, if at cell arrival the related cell counter exceeds this threshold, and the exceeding cell is not an end of packet or an OAM cell, then the cell is discarded and the flag DiscardRestOfPacket is enabled in the LCI table. All subsequently arriving cells of the packet, excluding the last cell of the packet, are discarded without taking into consideration the cell counter.

PPD may only be applied to non real-time connections. The mechanism is enabled by the software configurable flag PPDen, specified per traffic class in the TCT.

Note: EPD/PPD functionality is offered by the ABM-3G on a per VC basis. Hence, these functions can be supported also for connections sharing a queue.

Note: Cell discarding due to EPD and PPD does not apply to non-user cells, e.g. an OAM cell within a packet is not discarded.

GFR Packet Discard

The EPD mechanism in combination with the flag GFRen is used to support the GFR service. GFR packet discard works only in conjunction with EPDen = 1 and discards only a well defined subset of the packets normally eligible for EPD.

In particular, when EPDen = 1 and GFRen = 1, a packet is discarded only if:

[(BufEPDNg or SBMax or TrafClassMax) and QueueMax] or

any of the EPD CLP1 thresholds is exceeded.

GFRen and PPDen are independent. GFRen has no influence on PPD and PPDen has no influence on GFR.

GFRen has no influence on the discard of CLP=1 frames. Therefore there is no difference between EPD and GFR packet discard regarding CLP=1 frames.

3.4.1.6.4 Minimum Buffer Reservation

A minimum buffer reservation is provided on a per queue basis by setting parameter MinBG. As long as the queue length has not reached this value, an incoming cell can be stored without further checks, except the queue threshold checks. When the MinBG limit is exceeded, the Cell Acceptance Algorithm checks if buffer space is available in the non guaranteed buffer space.

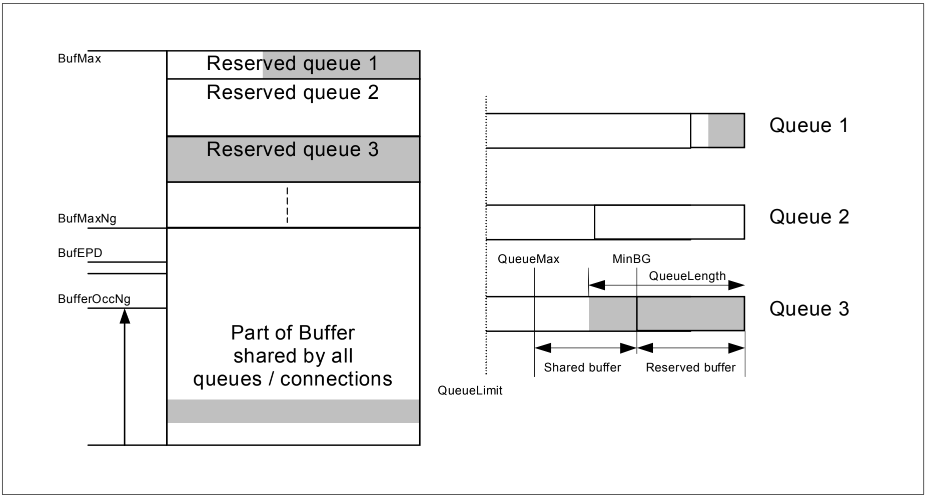


Figure 3-18 Buffer Management with per Queue Minimum Buffer Reservation

For all traffic classes, the threshold BufMaxNg must be adjusted appropriately, such that, if LQ is the set of logical queues allocated so far, then:

$$\text{BufMax} - \text{BufMaxNg} \geq \sum_{\forall i \in LQ} \text{MinBG}_i$$

Although the ABM-3G in principle has the knowledge of all programmed guaranteed minimum queue sizes, it does not perform the summation for complexity reasons.

Refer to **Register 39 "QCT2" on Page 217** for the programming of minimum buffer reservation thresholds. If the condition in the formula above is not fulfilled, then error condition BCFGE occurs and is signalled in **Register 101 "ISRU" on Page 297** or **Register 102 "ISRD" on Page 300** respectively.

3.4.1.6.5 Hysteresis for Maximum Thresholds

Hysteresis is an optional feature for the maximum thresholds BufMaxNg, SBMax, TrafClassMax, and QueueMax in cell discard mode. Hysteresis means that cell discard starts when any of the maximum thresholds mentioned above (referred to as TH for convenience) is exceeded and continues until the level falls below a threshold TL that is considerably lower than TH.

A hysteresis control parameter DH_i is provided per traffic class i. It is used to calculate the low threshold TL_i from a given high threshold TH_i according to:

$TL_i = TH_i - (TH_i \gg [DH_i + 1])$, with DH_i ranging from 1 to 7.

DH_i=0 disables the feature. **"DH" on Page 207** provides the programming details.

An example for the hysteresis mechanism is shown in **Figure 3-19** below.

When TH is exceeded, a connection specific discard flag is set which is cleared again when the buffer fill falls below TL. This flag is used by the cell acceptance algorithm to differentiate between accept state and discard state.

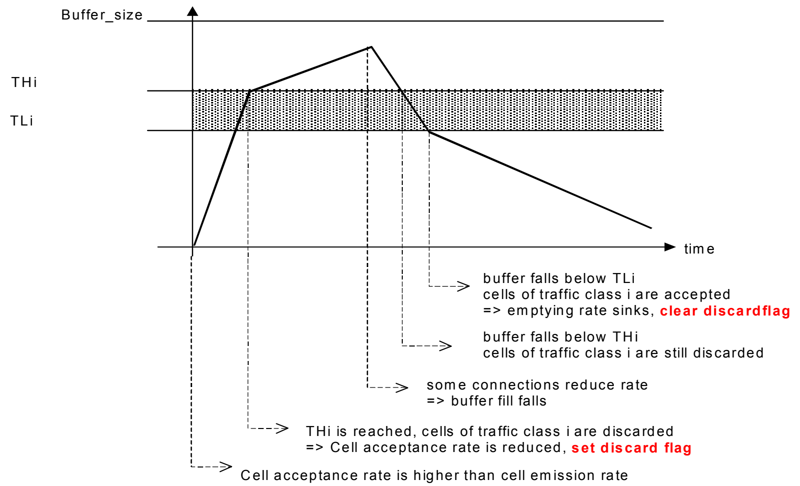


Figure 3-19 Buffer Threshold with Hysteresis

Hysteresis is not used with packet discard and CLP1 discard thresholds.

Hysteresis avoids oscillation effects when the buffer fill is just stable at a certain value and this value just coincides with a certain threshold. A stable buffer fill occurs when input and output flow of the buffer are equal. However, due to cell clumping effects the fill value will vary with a cell jitter in the range 10..100 cells. The hysteresis threshold difference should be larger than the jitter.

3.4.1.7 Cell Acceptance Algorithm

The following pseudo-code provides the cell acceptance algorithm of the ABM-3G based on the parameter set listed in **Chapter 3.4.1.3**.

3.4.1.7.1 Discard Conditions

```
/***** Basic Max/EPD conditions **********************************/
ExceedMaxBuffer =     (BufferOcc = BufMax)
ExceedMaxGlobal =     (BufferOccNg >= BufMaxNg)
ExceedEpdGlobal =     (BufferOccNg >= BufEPDNg)
ExceedMaxSB =         (SBOccNg >= SBMax) AND (QID != 0)
ExceedMaxTrafClass = (TrafClassOccNg >= TrafClassMax)
ExceedMaxQueueLimit= (QueueLength = QueueLimit)
ExceedMaxQueue =      (QueueLength >= QueueMax)

/***** Basic CLP1 conditions ***************************************/
ActiveCLP1 =          (CLP=1) AND (CLPT = FALSE)

ExceedCLP1Global =    (BufferOccNg >= BufCiCLP1) AND ActiveCLP1
ExceedCLP1SB =        (SBOccNg >= SBCiCLP1) AND (QID != 0) AND ActiveCLP1
ExceedCLP1Queue =     (QueueLength >= QueueCiCLP1) AND ActiveCLP1

/***** Basic reservation conditions *******************************/
ExceedMinBG =         (QueueLength >= MinBG)
ExceedCLP1DIS =       (SBOccLP >= CLP1DIS) OR (QID = 0)

/***** Derived conditions *****************************************/
ExceedMaxNg =         ExceedMinBG AND {[
                      (EPDen = FALSE) AND (
                      ExceedMaxTrafClass OR ExceedMaxSB OR ExceedMaxQueue
                      )
                      ] OR ExceedMaxGlobal }

ExceedEpd =           ExceedMinBG AND [
                      ExceedEpdGlobal OR ExceedMaxTrafClass OR ExceedMaxSB
                      ]

ExceedEpdCLP1 =       ExceedCLP1DIS AND {[
                      ExceedMinBG AND (ExceedCLP1Global OR ExceedCLP1SB)
                      ]
                      OR ExceedCLP1Queue }

ExceedCLP1 =          ExceedEpdCLP1 AND (EPDen = FALSE)
```

3.4.1.7.2 EPD Algorithm

Based on the variables set by the EPD support parts of the threshold exceed algorithm and queue specific variables, the EPD algorithm decides upon the acceptance of a packet.

```
IF      LastCellOfPacket AND UserToUserCell
THEN    IF       [(ExceedEpd OR ExceedMaxQueue) AND (GFRen = FALSE)] OR
                 (ExceedEpd AND ExceedMaxQueue) OR
                 ExceedEpdCLP1
        THEN DiscardPacket = TRUE
        ELSE DiscardPacket = FALSE
ELSE    Do nothing

IF      EPDen AND UserToUserCell AND DiscardPacket
THEN    CellAcceptedByEPD = FALSE
ELSE    CellAcceptedByEPD = TRUE

LastCellOfPacket =   UserToUserCell AND EndOfPacket
```

3.4.1.7.3 PPD Algorithm

If the PPD algorithm is applied, the last cell of a corrupted packet should be accepted.

```
IF      PPDen AND UserToUserCell AND EndOfPacket
THEN    DiscardRestOfPacket = FALSE

IF      PPDen AND UserToUserCell AND DiscardRestOfPacket
THEN    CellAcceptedByPPD = FALSE
ELSE    CellAcceptedByPPD = TRUE
```

3.4.1.7.4 Hysteresis Algorithm

```
For any threshold TH:Delta(TH) = TH - TH/2**[DH + 1] with DH in 1..7

FillBelowHyst =       (ExceedMinBG = FALSE) OR (DH = 0) OR [
                      (BufferOccNg < Delta(BufMaxNg)) AND
                      ((SBOccNg < Delta(SBMax)) OR (QID = 0)) AND
                      (TrafClassOccNg < Delta(TrafClassMax)) AND
                      (QueueLength >= Delta(QueueMax)) ]

IF      UserToUserCell AND (PPDen = FALSE) AND FillBelowHyst
THEN    DiscardRestOfPacket = FALSE

IF      UserToUserCell AND (PPDen = FALSE) AND DiscardRestOfPacket
THEN    CellAcceptedByHyst = FALSE
ELSE    CellAcceptedByHyst = TRUE
```

3.4.1.7.5 Overall Cell Acceptance Algorithm

The overall decision whether an arriving cell is buffered is based on the results of the previous algorithms. The arriving cell can only be accepted if all algorithms would accept the cell and if buffer space is available. To obtain the overall decision whether a correctly received cell is finally buffered the following algorithm applies:

```
IF      (ExceedMaxBuffer = FALSE) AND
        (ExceedMaxQueueLimit = FALSE) AND
        (ExceedMaxNg = FALSE) AND
        (ExceedCLP1 = FALSE) AND
        (CellAcceptedByEPD = TRUE) AND
        (CellAcceptedByPPD = TRUE) AND
        (CellAcceptedByHyst = TRUE)
THEN    BufferIncomingCell
ELSE    DiscardIncomingCell
        IF    PPDen AND UserToUserCell AND (EndOfPacket = FALSE)
        THEN  DiscardRestOfPacket = TRUE
        IF    PPDen = FALSE AND UserToUserCell AND ExceedMaxNg
        THEN  DiscardRestOfPacket = TRUE
```

See **Figure 4-9** for an example of threshold configuration.

3.4.1.8 Statistical Counters

In addition to the occupancy counters, which may also be used for statistical purposes, the ABM-3G device provides several dedicated counters for statistics purposes. These are summarized in **Table 3-20**:

Table 3-20 Statistical Counters

BM view	Location	Name	Width	Comment
Buffer	Reg 17	UMAC/DMAC	16	Maximum buffer occupancy value since last readout
	Reg 18	UMIC/DMIC	16	Minimum buffer occupancy value since last readout

Table 3-20 Statistical Counters (cont'd)

BM view	Location	Name	Width	Comment
Traffic Class	TCT2 TCT3	AcceptedCells/ Packets	32	Total transmitted cells or packets, selectable by flag SCNT
	TCT0	LostPackets/CLP1Cells	16	EPD discards or CLP1 discards
	TCT2 TCT3	LostCellsTotal	32	Total cell discards
	TCT1	LostCellsBuffer	4	Global buffer overflow cell discards
	TCT1	LostCellsSB	4	Scheduler block overflow discards
SB	SBOC0 SBOC1	SBOccLPd	18	Scheduler block CLP1 cell discards

3.4.2 Queue Scheduler

3.4.2.1 Functional Overview

The basic function of the hierarchical Queue Scheduler (QS) is to properly allocate cell transmission slots to scheduler blocks and within those to queues, enabling them to send buffered cells. Thereby, the QS allocates the bandwidth resources needed to fulfill the specific service guarantees of individual connections.

Internally, the QS functions are implemented by two basic building blocks: 128 identical scheduler blocks (SB) and a subsequent round robin scheduler (SBS) as depicted in **Figure 3-21**. In addition to these, a prioritized empty cell generator queue (for SDRAM refresh) and a Common Real-Time (CRT) queue which also has priority over the SBS, are provided. These two queues are assumed to be rate limited. **Section 4.2.2.4** and **Section 4.2.2.3** respectively provide the details on the programming of these queues.

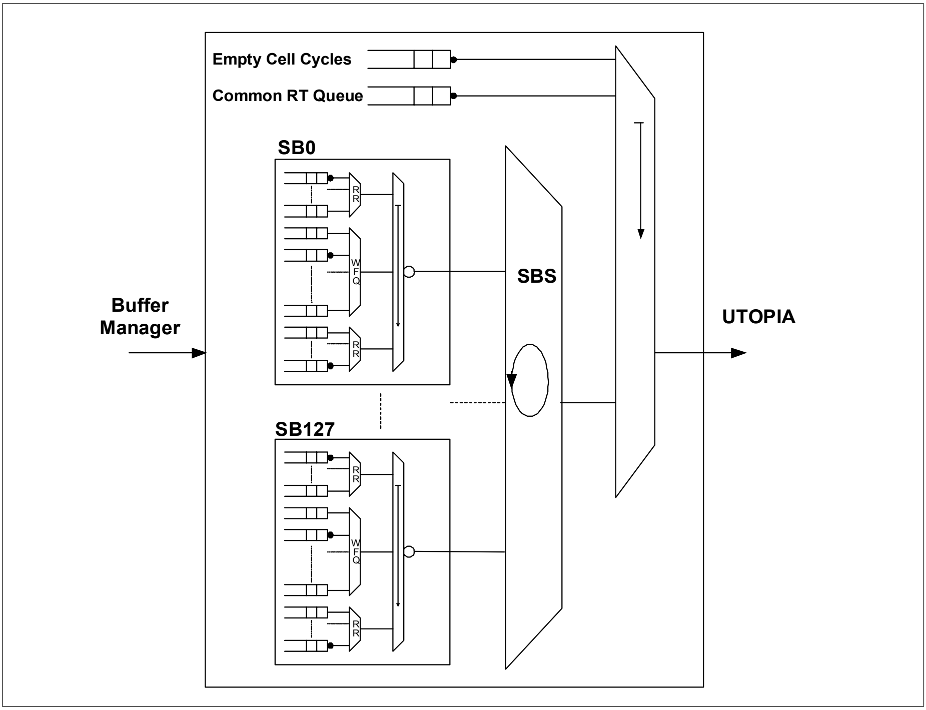


Figure 3-21 Functional Structure of the Hierarchical Queue Scheduler

In summary, the Queue Scheduler calculates a QID for each cell emission opportunity.

3.4.2.2 Scheduler Block

Each Scheduler Block (SB) is a cascade of two scheduling levels, a combination of Weighted Fair Queueing (WFQ) and Round Robin (RR) schedulers in the first stage, followed by a priority scheduler in the second stage as shown in **Figure 3-22**. An arbitrary number of queues from a maximum of 8191 can be assigned to each scheduler input at stage 1. (Queue 0 is reserved for the common real-time bypass).

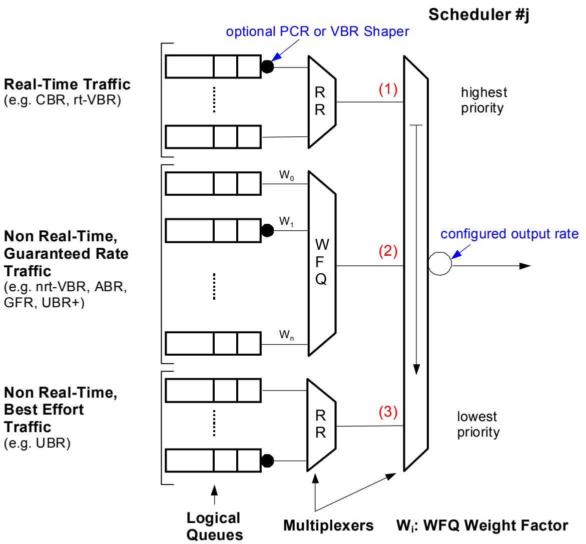


Figure 3-22 Scheduler Block Structure

Scheduler Blocks are the principal queue scheduler concept for QoS differentiation. Together with the buffer manager concept of traffic classes, various QoS objectives can be met.

3.4.2.2.1 Priority Scheduler

The priority scheduler implemented in the scheduler block of the ABM-3G has three priority levels. As long as there are buffered cells destined to pass at priority 1, only these cells are served. Otherwise, buffered cells destined to pass at priority 2 are served. Only when there are neither priority 1 nor priority 2 cells buffered, then cells from priority 3 are allowed to pass. As a result the available bandwidth for priority 1 traffic is the total output bandwidth. The available bandwidth for priority 2 and priority 3 traffic is the leftover bandwidth from the next higher priority level respectively.

Chapter 4.2.2.7 provides the details on the mapping of queues to the 3 priority levels.

3.4.2.2.2 Round Robin Scheduler

The round robin scheduler keeps all of its input queues, which have cells to send in a FIFO structured list. The queue at the head of the list is allowed to send one cell and is then rescheduled at the end of the list. Thereby, the available bandwidth is divided equally among those queues which have cells to send.

3.4.2.2.3 Weighted Fair Queueing Scheduler

Rate guarantees for non real-time connections are achieved with the WFQ scheduler. The WFQ scheduler has an arbitrary number of input queues with a weight factor assigned to each of them. The absolute values of the weights are irrelevant, only the relative values count. See **Chapter 4.2.2.7** for a discussion on appropriate selection of weight factors.

The WFQ scheduler has the following important properties:

- It is work conserving, i.e. the available bandwidth is always used completely as long as any of the attached queues has cells to send.
- It provides a fair distribution of the available bandwidth in proportion to the assigned weights under any load condition.
- It guarantees minimum rates to queues as long as the sum of the configured minimum rates fits into the available bandwidth.

The properties above make the WFQ scheduler particularly useful for bursty connections with start/stop behavior. The WFQ scheduler automatically deals with the varying load situations and always distributes the bandwidth according to the weight factors.

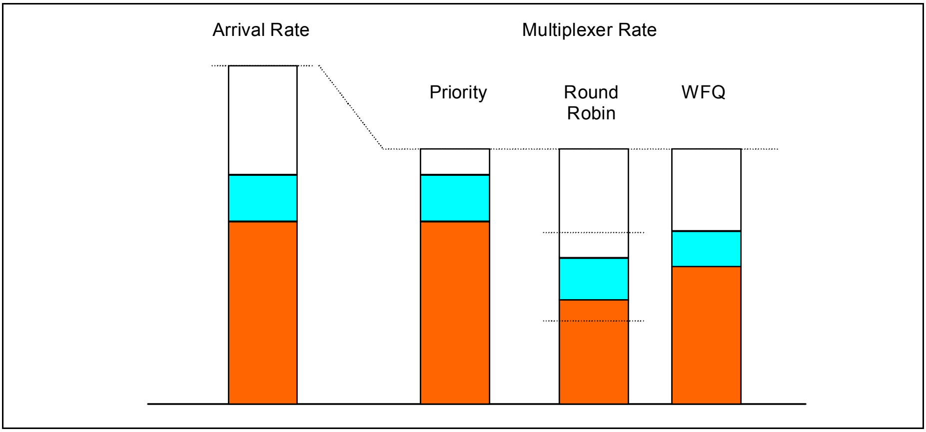


Figure 3-23 Behavior of Different Scheduler Types

For a given arrival rate **Figure 3-23** shows the repartition of the output rate. The priority scheduler simply cuts off the low priority traffic assumed in the white bar. The RR scheduler iteratively divides the output rate into equal shares among the active inputs. The WFQ scheduler divides the output rate in proportion to the assigned weights assumed to be proportional to the respective arrival rates.

3.4.2.3 Quality of Service Support

In the context of ATM service categories, it is useful to introduce the concept of guaranteed rate. This is the rate which the network must guarantee to the user in order to fulfill the QoS demands.

Table 3-24 Guaranteed Rates for each ATM Service Category

ATM Service Category	Guaranteed Rate	Comment
CBR	PCR	
rt-VBR	SCR...PCR	Guaranteed rate is calculated with “effective bandwidth formulas” assuming small buffers and taking into account statistical multiplexing gain.
nrt-VBR	SCR	
GFR	MCR	Guaranteed rate is delivered in complete uncorrupted AAL5 frames.
UBR+	MCR	
UBR	none	Guaranteed rate is always > 0 with queue connected to the WFQ scheduler, can be 0 for arbitrary long times in low priority RR scheduler.

Mapping of connections to stage 1 schedulers depends on the ATM service category of the connection (also shown in **Figure 3-22**) as follows:

– Priority 1 RR: real-time connections (CBR, rt-VBR).
– Priority 2 WFQ: non real-time connections with guaranteed rate (nrt-VBR, GFR, UBR+)
– Priority 3 RR: best effort connections UBR

An example of a scheduler with one priority 1 real-time queue (Queue 1) and nine priority 2 non-real-time queues (Queue 2 through Queue 10) is shown in **Figure 3-25**. Queue 1 is shared by a number of connections with different bit rates.

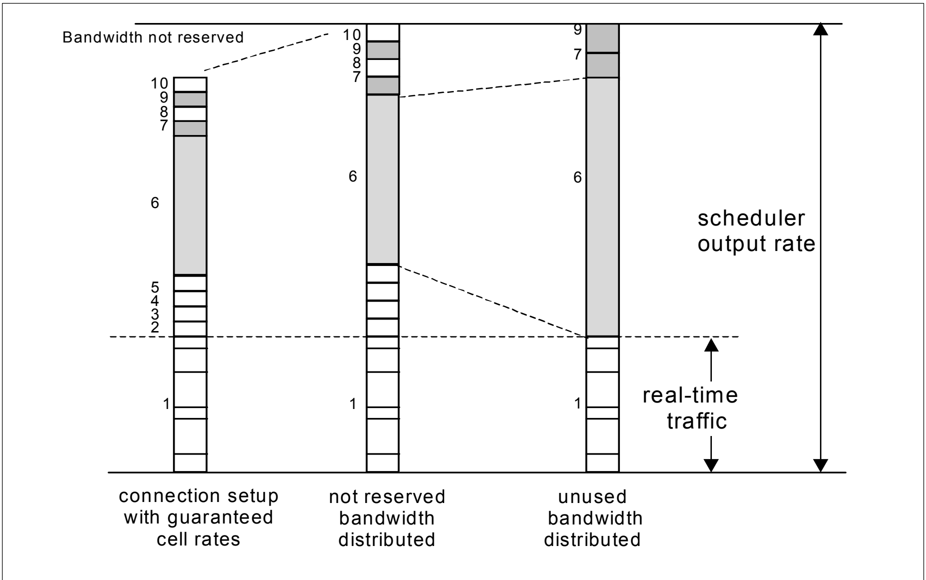


Figure 3-25 Scheduler Behavior Example

The three columns in **Figure 3-25** describe different conditions: The left column shows the scheduler load as seen from Connection Acceptance Control (CAC). New connections are accepted as long as their guaranteed rates fit the spare bandwidth of the scheduler. The center column shows the case in which all Queues 2..10 are filled; that is, all non-real-time connections are sending data. The total non-real-time bandwidth, including the spare bandwidth, is then distributed to the 9 queues according to their weight. In this case, two weight factors are defined. Queue 6 has weight of 1, others have weight of 10. The right column shows the case of only three queues (6, 7 and 9) filled; all other connections are not sending data at this time. Again, the available bandwidth is fairly distributed among the queues, still conserving the 1:10 ratio defined by their weights.

Notice that bandwidth of the real-time connections is not affected by bandwidth re-adjustments; but, remains constant over time under the assumption that real-time connections are constantly sending data. If, however, a real-time connection should not use its bandwidth, the bandwidth would be used immediately by the non-real-time connections. The behavior of the WFQ scheduler shown in **Figure 3-25** for non-real-time connections has advantages for both the network operator and for the end user:

- The available bandwidth is always used completely, resulting in optimum usage of transmission resources.
- A user paying for a higher guaranteed rate also obtains higher throughput under all load conditions.

3.4.2.4 Traffic Shaping

Traffic shaping is a mechanism that alters the characteristics of a cell stream in order to make better use of network resources or to enforce conformance to the negotiated traffic contract at an interface. Conformance is defined operationally in terms of a Generic Cell Rate Algorithm GCRA(T,tau) which specifies the upper limits, in terms of a given tolerance tau, for cells arriving in excess with respect to a given reference cell rate (1/T). The ITU-T Recommendation I.371 [**1**] or the ATM Forum TM Specification 4.1 [**2**] provide the details.

A situation that is particularly prone to produce non-conforming traffic is congestion in a network. **Figure 3-26** shows the need for shapers at the output of a congested network for nrt-VBR traffic. An nrt-VBR cell stream originally shaped to conformance by the terminal (1) traverses Network A, which exhibits burst level congestion. At the output of Network A the cell stream is accumulated into a single large burst, which by far exceeds even the Peak Cell Rate (PCR) of the original connection (2). It is no longer conforming to the traffic contract and therefore would not pass through the subsequent policer. Hence, at the output of Network A, an SCR shaper is enabled, which regenerates a conforming cell stream to match a given burst tolerance BT (3). This cell stream is accepted by the policer and traverses Network B which exhibits cell level congestion only. As a result PCR and SCR vary slightly due to the cell clumping effect (4). This Cell Delay Variation (CDV) is reduced to match a given tolerance (CDVT) by the PCR shaper at the output of Network B (5).

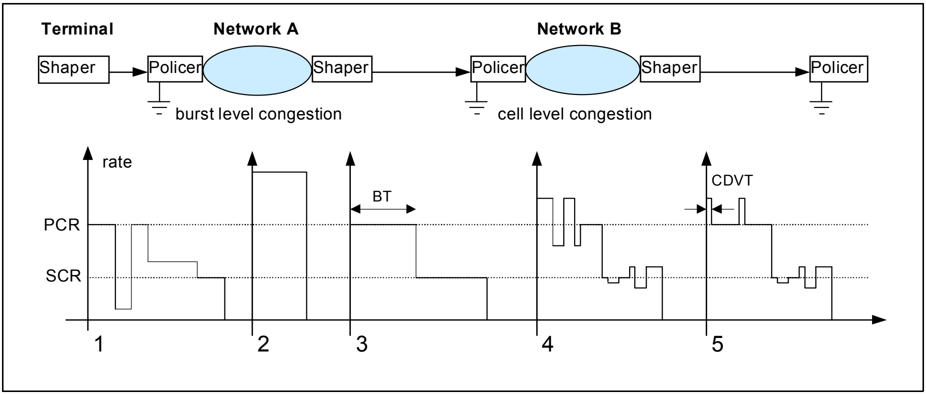


Figure 3-26 Shaping and Policing at Network Boundaries

Note that the outcome of Network B has a very different shape when compared to the input to Network A and to the outcome of Network A. Nevertheless, due to the shapers implied, the traffic is conforming on both the User-Network interface (UNI) and the subsequent Network-Network Interfaces (NNI).

The ABM-3G contains two basic shaping mechanisms, which can be activated per logical queue: PCR limitation and leaky bucket shaping. In particular it is possible to enable both mechanisms simultaneously on the same logical queue, a necessary feature to implement true VBR shaping as explained below.

3.4.2.4.1 PCR Limitation

For all logical queues a rate limitation can be enabled, which controls the peak cell rate (PCR) from this queue. In other words, cells from a PCR limited queue are always spaced by at least TP=1/PCR seconds. Cell clumping within the network is thereby eliminated. Traffic passing through a PCR limiter is conforming to any PCR traffic contract, since the tolerance of the PCR limiter is zero.

3.4.2.4.2 Leaky Bucket Shaping

A leaky bucket shaper controls a given sustainable cell rate (SCR) within the limits of a given Burst Tolerance (BT).

The Burst Tolerance and the SCR determine the Maximum Burst Size (MBS) (in cells) that may be transmitted at an arbitrary PCR according to the following formula (refer to [**2**]):

$$MBS = \left\lfloor 1 + \frac{BT}{\frac{1}{SCR} - \frac{1}{PCR}} \right\rfloor \qquad [\text{cells}] \qquad (1)$$

Vice versa, when the MBS is received (via signalling), the corresponding BT can be calculated according to the following formula:

$$BT = (MBS - 1) \cdot \left(\frac{1}{SCR} - \frac{1}{PCR}\right) \qquad [\text{s}] \qquad (2)$$

In the ABM-3G leaky bucket shaping can be enabled for up to 2048 PCR limited logical queues. In addition to the parameter TP = 1/PCR, the cell spacing for TS = 1/SCR and the burst tolerance tauS = BT must be specified.

Figure 3-27 shows the outcome of the ABM-3G leaky bucket shaper under ideal conditions when loaded with a burst.

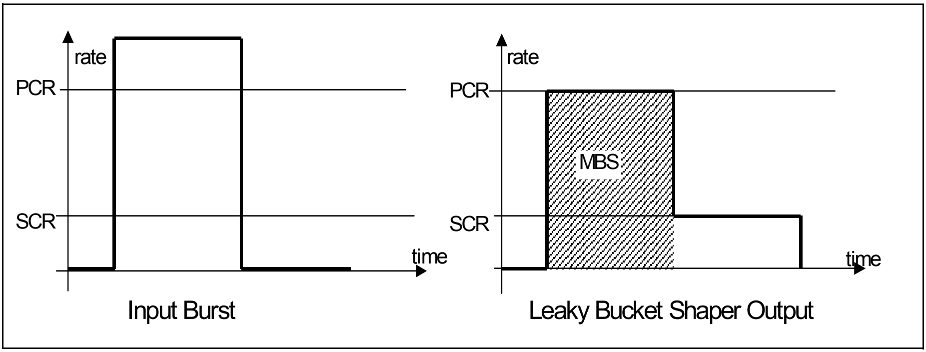


Figure 3-27 Ideal ABM-3G Shaper Output

The implementation of the combined shaper guarantees sending the MBS as fast as possible without exceeding the PCR.

If several cell streams are shaped simultaneously, it may happen that cells from different shapers would have to be sent out at the same cell slot. If N cell streams are shaped, in rare cases, a cell may have to wait up to N-1 cell cycles for transmission. This temporary loss of rate is compensated for by slightly stretching the burst in time.

The additional CDV introduced to the PCR by this effect is monitored. With parameter CDVMax an upper limit on the CDV than can occur without notice is programmed. If this value is exceeded, an interrupt is generated. **"UCDV/DCDV" on Page 239** provides the details.

The difference between ideal and real shaper output is shown in **Figure 3-28**

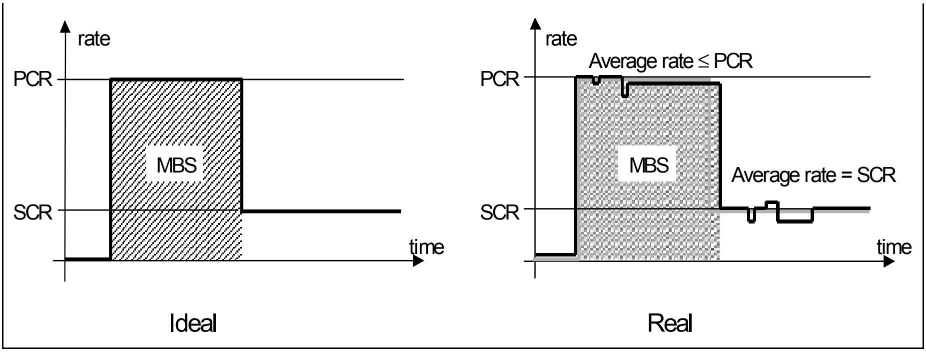


Figure 3-28 Ideal and Real ABM-3G Shaper Output

Table 3-29 summarizes the parameters needed for combined PCR and SCR shaping.

Table 3-29 Summary of VBR Shaping Parameters

Parameter	Derived from	Stored in Table/ Register	Range	Min. Value	Max Value
TP	1/PCR	AVT:TP	16 bit	*)	65471
TS	1/SCR	AVT:TS	16 bit	*)	65471
tauS	MBS or BT	AVT:tauS	16 bit	0	64511
VBR2.3		AVT:Config	1 bit	0	1
CDVMax		UCDV/DCDV	8 bit	16 cell cycles	255 x 16 cell cycles

*) Refer to Table 4.2.2.5f for an explanation of shaper parameter ranges and granularities.

3.4.2.4.3 Shaping for VBR conformance

The standards define three conformance definitions for rt-VBR and nrt-VBR, referred to as VBR.1, VBR.2 and VBR.3. Table 3-30 explains the differences between the three VBR conformance definitions in terms of the relevant cell stream: index 0+1 denotes both CLP=0 and CLP=1 cells while index 0 denotes CLP=0 cells only.

Table 3-30 VBR Conformance Definitions

	PCR Conformance	SCR Conformance
VBR.1	GCRA(PCR_{0+1}, $CDVT_{PCR}$)	GCRA(SCR_{0+1}, BT)
VBR.2	GCRA(PCR_{0+1}, $CDVT_{PCR}$)	GCRA(SCR_0, BT)
VBR.3	GCRA(PCR_{0+1}, $CDVT_{PCR}$)	GCRA(SCR_0, BT), non conforming CLP=0 cells may be tagged (CLP set to 1)

Hence, from a shaping perspective, there is no difference between VBR.2 and VBR.3.

As a consequence, the leaky bucket shaper in the ABM-3G is configurable on a per queue basis to shape either the CLP=0+1 cell stream (config parameter VBR2,3 = 0) or alternatively the CLP=0 cell stream only (config parameter VBR2,3 = 1). The PCR limiter always shapes the CLP=0+1 cell stream.

By enabling a Leaky Bucket Shaper with the parameters TP=1/PCR, TS=1/SCR, tau = BT and VBR2,3 = (0|1), the ABM-3G can be used to produce conforming VBR traffic.

Note that the PCR limiter does not make use of the tolerance $CDVT_{PCR}$ where transmission at higher rates than PCR would be possible. However, $CDVT_{PCR}$ is primarily intended to allow cell clumping and other networks artifacts, not to allow a higher rate. As mentioned earlier, this more rigid shaping does not violate PCR conformance.

3.4.2.4.4 Shaping for CBR conformance

In cases where simple PCR limitation is not sufficient for service categories that define a PCR conformance only, such as CBR, it is possible to use the leaky bucket shaper with parameters TS=1/PCR and tau=$CDVT_{PCR}$. The parameter TP can be set to any suitable value to reflect higher allowed rates than PCR.

3.4.2.5 VC-Merge and Dummy Queue

Any queue can be configured (mutually exclusive) to participate in a VC-merge group or as a 'dummy queue'. A detailed description of enabling/disabling those special queue functions is provided in the description of **"Queue Configuration Table Transfer Registers QCT0..6" on Page 211**.

3.4.2.5.1 VC-Merge

Several logical queues carrying AAL5 packets may be grouped together into one of a maximum of 128 merge groups. Functionally, a Packet Round-Robin (PRR) scheduler stage is inserted between the queues of the merge group and the first scheduling stage of the scheduler block. Whenever a **complete** packet is queued in a QID of a merge group, this QID is enabled to the PRR. The PRR schedules a QID to the SB until all cells of the current packet are transmitted. Then it switches to the next enabled QID.

Hence, viewed from the Scheduler Block, a merge group appears like a single queue with the additional benefit that the output VC maintains AAL5 packet boundaries. See **Figure 3-31**.

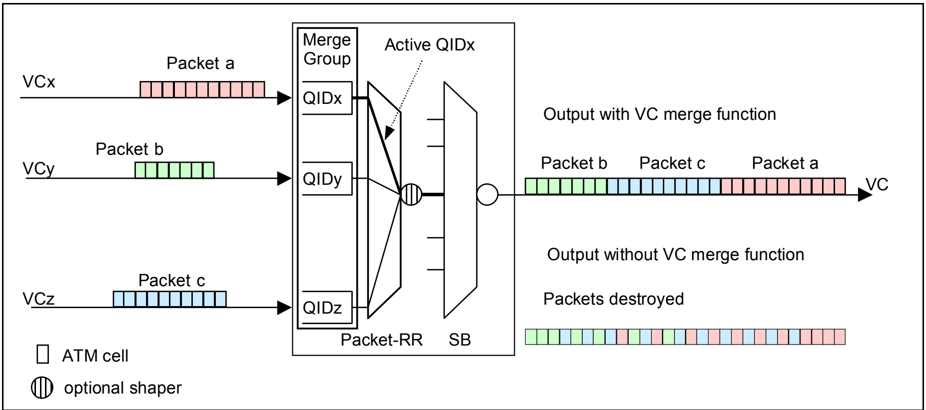


Figure 3-31 VC Merge Scheduling

Any queue can be configured to be member of one of the 128 merge groups in the QCT by setting 'RSall' = 0 in **Register 38 "QCT1" on Page 214** and then setting 'MGconf/DQsch' = 1 and 'MGID' to the desired merge group identifier in **Register 39 "QCT2" on Page 217**.

If the queue is the first queue of the merge group, then its QID must be written into field 'Head_Pointer' in **Register 51 "MGT2" on Page 234**.

Assigning a queue to a VC-merge group already enables the packet boundary aware scheduling of all queues within the same group.

Optionally, the ATM cell header may be overwritten with a new value programmed in the MGT by setting ’LCIOen’ = 1 and ’LCI’ to the desired value in **Register 51 "MGT2" on Page 234**.

A queue is released from its VC-merge group by setting ‘QIDvalid’ = 0 in **Register 38 "QCT1" on Page 214**.

It is recommended to set the parameters of the individual queues in a merge group to equal values, reflecting the desired properties of the outgoing merged VC. In particular, the user must make sure that all queues of a merge group are assigned to the same SB.

Also, for the optional shaping of a merged VC, the shaping parameters TP, TS, tauS and Config must be specified for each of the logical queues of the merge group and should all be equal to the intended shaping parameters of the outgoing merged VC.

The VC-merge shaping mechanism works round robin on a per queue basis with the changing of the QID going on transparently behind the scene. Hence, viewed from the outgoing VC, there is no difference between a single queue VBR shaping and a merge queue VBR shaping. In particular, no cell slot is lost on the transition between queues.

3.4.2.5.2 Dummy Queue

A ‘dummy queue’ (in contrast to a normal queue) is always scheduled by the queue scheduler according to its associated rates and parameters, even though it does not contain stored cells. Scheduling a dummy queue results in an ’empty cell cycle’ (no cell is emitted during this cycle).

Storing cells into a dummy queue is possible, but not recommended, since the cells are never emitted.

Dummy queues can be used for bandwidth reservation e.g. for subsequent multicast operation or any other cell insert/multiplier process.

A queue can be configured as a ‘dummy queue’ by setting ’DQac = 1’ and ‘RSall’ = 1 in **Register 38 "QCT1" on Page 214**. This may only be done if ’MGconf/DQsch’ = 0 in **Register 39 "QCT2" on Page 217** and the queue is empty (QueueLength = 0).

3.4.3 Scheduler Block Usage

The ABM-3G allows arbitrary assignment of connections to queues and of queues to scheduler blocks. A scheduler block can be assigned to any UTOPIA PHY. Usage of a scheduler differs in switch input (upstream) or output (downstream). For the Mini-Switch application the upstream case does not exist.

At a switch output, the scheduler blocks provide constant cell streams to fill the payloads of the PHYs. Either the entire cell stream of a PHY is provided or it is disassembled into several VPCs as shown in **Figure 3-32**. A VPC may contain both real-time and data connections. This is the case for a VPC which connects two corporate networks (virtual private networks), for example. The scheduler block concept has the advantage that data traffic is automatically adjusted after setup or teardown of a real-time connection. The output rate of a scheduler block in both applications is usually constant.

The scheduler blocks always react to UTOPIA backpressure or can be controlled completely by backpressure instead of shaping. All scheduler blocks whose physical outputs are asserting backpressure hold on serving. Scheduler blocks serving time slots which are lost due to temporary backpressure are maintained and served later, if possible. Therefore, the rate with some CDV will be maintained. The maximum number of stored time slots which can be configured is equal to the maximum burst possible for that port or path.

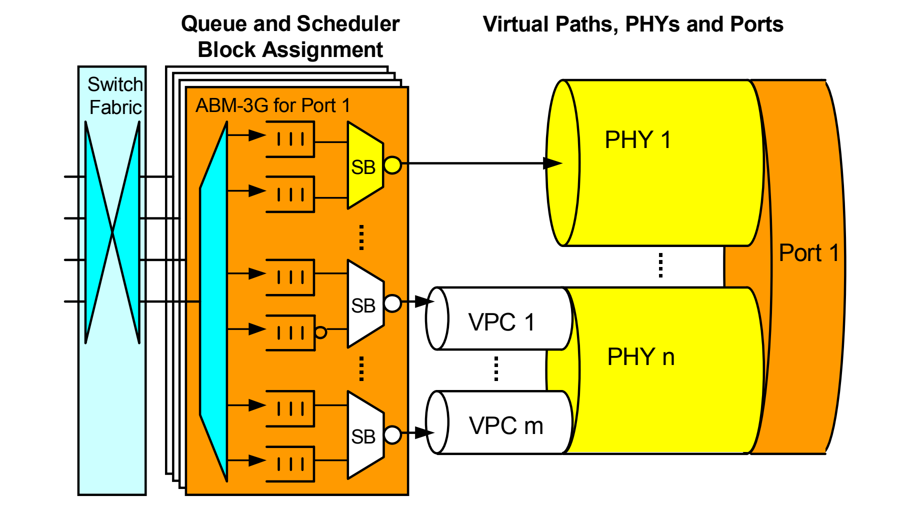


Figure 3-32 Scheduler Block Usage at Switch Output

At a switch input, each scheduler block is assigned to a switch output (**Figure 3-33**). A switch with **n** ports needs **n^2** scheduler blocks. The output rate of each scheduler block is re-adjusted continuously to obtain maximum switch throughput without overloading the switch port output rate. This principle is called Preemptive Congestion Control, that is, congestion due to overload is avoided.

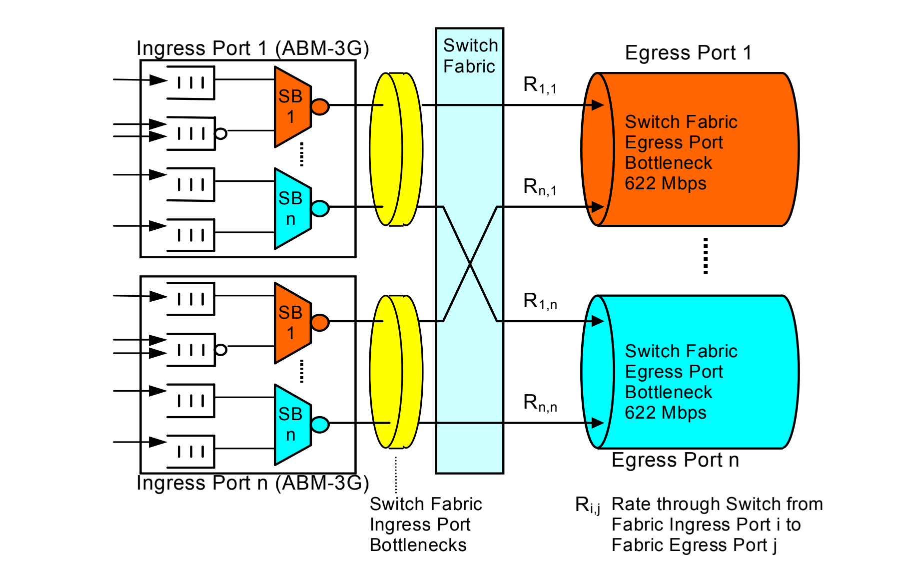


Figure 3-33 Scheduler Block Usage at Switch Input

There are two options for scheduler block rate adjustment:

- After each connection setup or trade-in (static bandwidth allocation).
- Backpressure controlled.

3.4.4 Scheduler Block Scheduler (SBS)

The SBS performs a weighted round robin scheduling among the active SBs. As long as the sum of the configured SB rates is below the service rate of the SBS, each SB receives bandwidth up to the configured rate, depending on the load in the SB.

The SBS is said to be overbooked if the sum of the configured SB rates is above the service rate of the SBS. In this case, the SBS behaves like an RR scheduler for the overbooked SBs, which all receive an equal amount of bandwidth.

The SBS supports up to 128 Scheduler Blocks per direction. In addition to this, a common real-time bypass queue (with fixed QID = 0) is supported.

3.4.5 Supervision Functions

3.4.5.1 Cell Header Protection

To guarantee that the cell header is not corrupted by the external SDRAM, it is protected by an 8-bit interleaved parity octet. It extends over the 5-octet standard header including the UDF1 octet. The BIP-8 octet is calculated for all incoming cells and stored at the place of the UDF2 octet. When a cell is read out, the BIP-8 is calculated again and is compared with the stored BIP-8. In case of a mismatch, an ’BIP8ER’ (**Register 101: ISRU**, **Register 102: ISRD**) interrupt is generated and the cell is discarded or not, depending on the configuration. cell header protection by BIP-8 can be disabled to achieve UDF2 transparency.

3.4.5.2 Cell Queue Supervision

The queueing of cells in the ABM-3G is implemented mostly by pointers. To detect pointer errors, the number of the queue in which the cell is stored is appended to the cell in the external cell storage SDRAM. When the cell is read out later, the selected queue number is compared to the QID stored with the cell. In case of a mismatch, a ’BUFER4’ (**Register 101: ISRU**, **Register 102: ISRD**) interrupt is generated. See also **“Upstream/ Downstream Cell Flow Test Registers” on Page 156**.

3.4.5.3 Scan Unit

The basic function of the Scan Unit is to periodically refresh outdated variables and detect idle connections.

The Scan Unit generates the (relative) cell clock **Tnow** needed by the VBR shaping mechanism and two (absolute) 1.25 ms and 10 ms clocks referred to as **ms125count** and **ms10count**.

The Scan Unit accesses the complete AVT Context RAM periodically every 1.25ms. In a first step dword0 containing the Config(6:0) bits is read. These bits are interpreted and then in a second step the respective dwords are read which contain the time information. In case of time-outs the information is modified and written back.

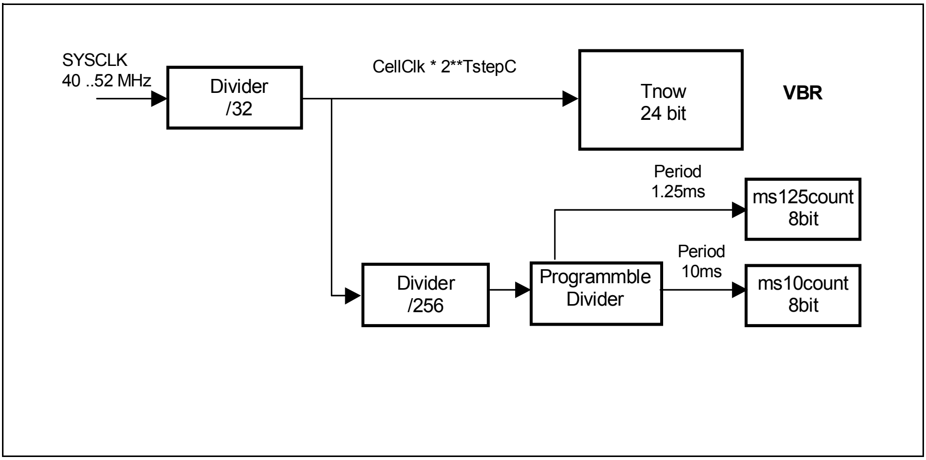


Figure 3-34 SCAN Timer Generation

The 40...60 MHz SYSCLK is divided by 32 to obtain a cell clock CellClk.

The **Tnow** counter with 24-bit width increments by 2**TStepC every CellClk. The value of this counter is made available as relative time reference to other blocks. Parameter TStepC is set in **Register 63 "USCONF/DSCONF" on Page 246**.

The absolute time bases are provided by dividing the CellClk first by 256 and then by a programmable divider of 7 bit (1...127).

Timer **ms125count** is derived from bit 4 of the programmable divider.

Timer **ms10count** is derived by from bit 7 of the programmable divider.

The divider is programmed with the parameter SCANP found in register **“ERCCONF0” on Page 286** depending on the SYSCLK value:

Table 3-35 Timer Values for Clock Generation

Frequency [MHz]	SCANP	period of ms10count [s]	delta [%]
40	49	0.010035	0.35
51.84	63	0.009956	0.44

Default value is SCANP=63, for the frequency of 51.84 MHz, which is easy to obtain as 1/3 of 155.52 MHz, the SDH/Sonet frequency.

The following scan is performed:

- For VBR
  Scan over all VBR QID
  Refresh TETvalid=Config[0], STvalid=Config[1] and TeV

The Scan Unit can be disabled with flag SCAND found in register **"ERCCONF0" on Page 286**.

3.5 Internal Tables

3.5.1 Table Overview

The ABM-3G provides a set of internal tables for configuration and runtime parameters. Figure 3-36 gives an overview of all (user accessible) tables and related control/transfer/mask registers:

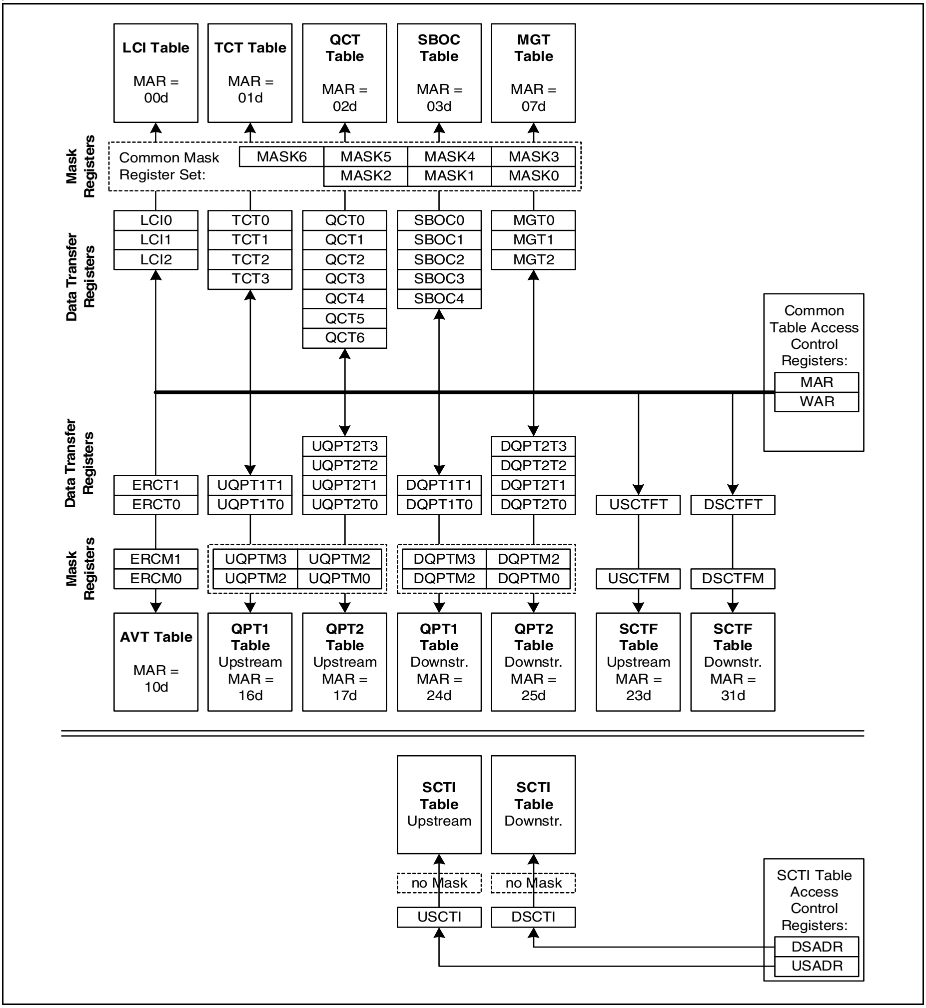


Figure 3-36 Table Access Overview

The tables are accessed by the microcontroller via control registers, data transfer registers and mask registers. While the control registers **"MAR" on Page 307** and **"WAR" on Page 309** are common to all tables (except SCTI tables), sets of mask registers are dedicated or shared among some tables. Data transfer registers are always dedicated to the specific table.

3.5.2 LCI: Local Connection Identifier Table

The basic function of the LCI table is assigning the connection (identified by the LCI) to one out of 8192 queues per direction. Single connections can be assigned to a dedicated queue (per VC queueing) or multiple connections might be assigned to the same queue.

"LCI Table Transfer Registers" on Page 191 provides the details.

3.5.3 QCT: Queue Configuration Table

The basic function of the QCT table is to determine queue specific parameters and to assign the queue to dedicated resources (Traffic Class, Scheduler Block, Merge Group).

"Queue Configuration Table Transfer Registers" on Page 211 provides the details.

3.5.4 QPT: Queue Parameter Table

The function of the QPT table is to configure the weight factor (in case a queue is assigned to the WFQ scheduler) and the peak cell rate value (in case the peak cell rate shaper is enabled).

"Queue Parameter Table Transfer Registers" on Page 247 provides the details.

3.5.5 TCT: Traffic Class Table

The function of the TCT table is to configure the buffer management behavior of up to 16 traffic classes.

"Traffic Class Table Transfer Registers" on Page 195 provides the details.

3.5.6 SBOC: Scheduler Block Occupancy Table

The function of the SBOC table (for 2*128 scheduler blocks) is to maintain the buffer filling levels associated with the dedicated scheduler.

"Scheduler Block Occupancy Table Transfer Registers" on Page 223 provides the details.

3.5.7 SCT: Scheduler Configuration Table

The function of the SCT table (for 2*128 scheduler blocks) is to determine the integer part (SCTI) and fractional part (SCTF) of the scheduler block output rates as well as the UTOPIA port number the scheduler is assigned to.

"Scheduler Configuration Table Integer Transfer Registers" on Page 257 and **"Scheduler Configuration Table Fractional Transfer Registers" on Page 267** provide the details.

3.5.8 MGT: Merge Group Table

The function of the MGT table (for 128 merge groups per direction) is to enable and specify the cell header overwrite function for the merge group output streams.

"Merge Group Table Transfer Registers" on Page 230 provides the details.

3.5.9 AVT: VBR Configuration Table

The AVT table is the main context RAM of the VBR shaping sub-system.

3.5.9.1 AVT Context RAM Organization and Addressing

The AVT Context RAM addressing scheme imposes some restrictions to the choice of QID numbers for support of VBR shaping. The table is organized into 2 K sections of 4 double words (32-bit) each whereas each section corresponds to the respective QID number.

Support of VBR shaping requires one section per connection, i.e. up to 2k-1 connections assigned to QID numbers (1, ..., 2047) can be supported for VBR shaping.

QID 0 is reserved for the common real-time queue.

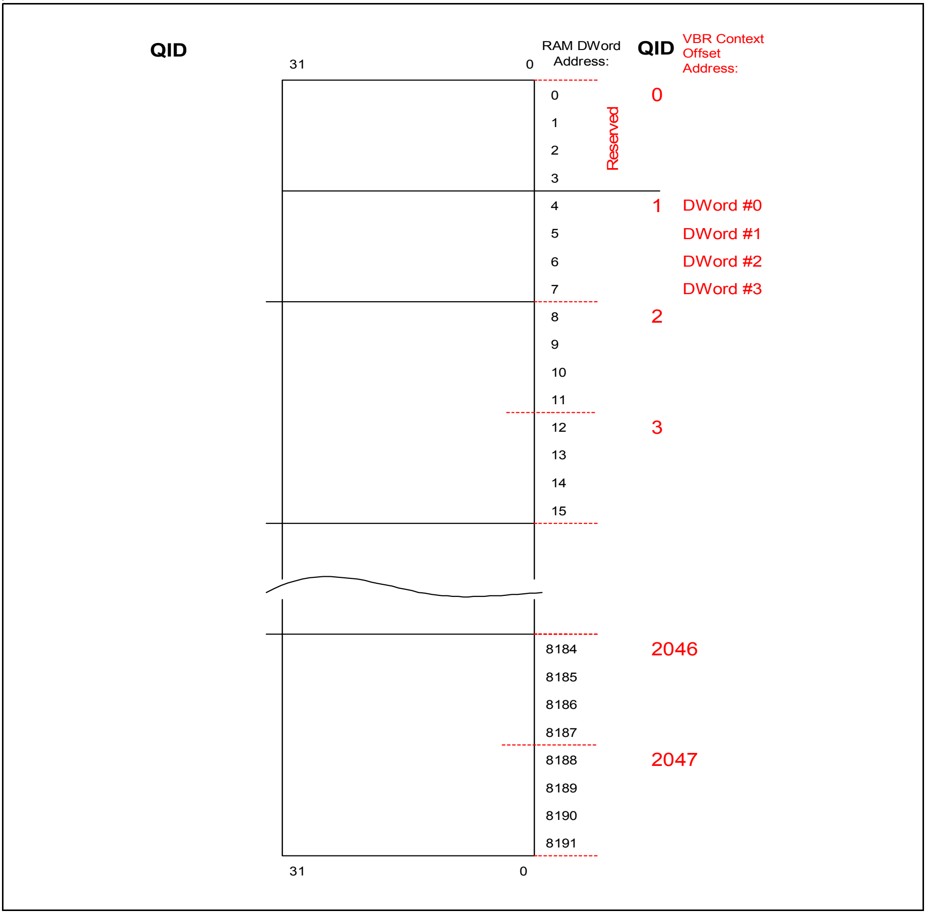


Figure 3-37 AVT Context RAM Addressing Scheme

The parameter utilization of each section depends on the mode selected for the particular queue (QID) in the Config field of the section. The mode specific parameter sets are described in subsequent chapters.

3.5.9.2 AVT Context RAM Section for VBR Shaping Support

In VBR shaping mode, one connection entry requires one AVT Context RAM section with a total of four double words. Since the AVT table is accessed from the external micro controller via a 16-bit transfer register, the VBR connection context appears as a 16-bit organized table with 8 entries as shown in **Table 3-38**:

Table 3-38 AVT Context Table: VBR Shaping (Table Layout)

<table>
<tr><th></th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td colspan="7">Config(6:0)</td><td></td><td colspan="8">TET(23:16)</td></tr>
<tr><td>1</td><td colspan="16">TET(15:0)</td></tr>
<tr><td>2a</td><td colspan="13">ST1(12:0)</td><td colspan="3">ST0(12:10)</td></tr>
<tr><td>3a</td><td colspan="10">ST0(9:0)</td><td colspan="6">STf(5:0)</td></tr>
<tr><td>2b</td><td colspan="13">unused</td><td colspan="3">VDT(18:16)</td></tr>
<tr><td>3b</td><td colspan="16">VDT(15:0)</td></tr>
<tr><td>4</td><td colspan="2">unused</td><td>TeV</td><td colspan="13">Temit(12:0)</td></tr>
<tr><td>5</td><td colspan="16">tauS(15:0)</td></tr>
<tr><td>6</td><td colspan="16">TS(15:0)</td></tr>
<tr><td>7</td><td colspan="16">TP(15:0)</td></tr>
</table>

Note: Entry 2/3 is used for 2 purposes:
a) Internal Relog–Relog/Reschedule: two possible ST values for low and high priority cells
b) Relog/Reschedule–Emit: VDT of next cell

Table 3-39 AVT Context Table: VBR Shaping Parameter Description

Parameter	Initial Value	Comment
Config(6:0)	configure	See **Section 3.5.9.3** for mapping
tauS(15:0)	configure	Delay tolerance parameter tau for SCR extension (15:10) and integer (9:0) part
TP(15:0)	configure	Rate parameter for peak rate limiter integer (15:6) and fractional (5:0) part
TS(15:0)	configure	Rate parameter for SCR-Leaky Bucket integer (15:6) and fractional (5:0) part
TET(23:0)	don’t care	Theoretical Emit Time for SCR
VDT(18:0)	don’t care	Virtual departure time of cell extension (18:16), integer (15:6) and fractional (5:0) part

Table 3-39 AVT Context Table: VBR Shaping Parameter Description (cont'd)

Parameter	Initial Value	Comment
ST0(12:0)	don't care	Scheduled departure Time for CLP=0 cell extension (12:10) and integer (9:0) part
ST1(12:0)	don't care	Scheduled departure Time for CLP=1 cell extension (12:10) and integer (9:0) part
STf(5:0)	don't care	Scheduled departure Time common fractional part for CLP=0 and CLP=1
TeV	0	Temit valid
Temit(12:0)	don't care	Real Emit Time

3.5.9.3 Common AVT CONFIG Field

The first word (WORD0) of each entry defines the entry type (inactive, VBR) with its respective submodes. The mapping of the 7 configuration bits Config(6:0) is summarized in **Table 3-40**.

Table 3-40 Config(6:0) Bit Map

Config field bit position	absolute WORD bit position	Function	
Bit 6	Bit 15	enable	'1' VBR shaping enabled
Bit 5	Bit 14	reserved	'0'
Bit 4	Bit 13	Core select	'0': upstream core '1': downstream core
Bit 3	Bit 12	VBR mode	'0': VBR1 '1': VBR2 and VBR3
Bit 2	Bit 11	used internally	CLP def. don't care
Bit 1	Bit 10	used internally	STvalid def. 0
Bit 0	Bit 9	used internally	TETvalid def. 0

4 Operational Description

4.1 Basic Device Initialization

The following actions are recommended to be performed after reset to prepare the ABM-3G chip for operation:

Basic settings

- Configure clocking system (DPLLs)
- Check register reset values
- Initialize SDRAM
- Reset internal tables (RAM)

ABM-3G diagnostic possibilities

- Check all internal RAM and register values
- Check external RAM

Data path setting and initial queueing and scheduling initialization

- Set MODE1 and MODE2 registers
  (Uni-directional Mode or Bi-directional Mode)
- Configure UTOPIA Interfaces: modes, number of PHYs
- Set global thresholds
- Initialize traffic class tables
- Set interrupt mask registers
- Programming of Scheduler output rates
- Programming of Empty Cell Rate generator
- Programming of Common Real Time Queue rate
- Assignment of Scheduler Blocks to PHYs at switch egress side
- Assignment of Scheduler Blocks to switch outputs at ingress side

Refer to the detailed register descriptions in **Chapter 7** for a complete picture of the necessary initializations.

4.2 Basic Traffic Management Initialization

To set up a connection, the complete table structure must be established:

LCI $\rightarrow$ QID $\rightarrow$ SBID and

LCI $\rightarrow$ QID $\rightarrow$ TCID

(see **Figure 4-1**). Additionally, bandwidth and buffer space reservations must be performed (see below). Depending on the traffic class, special functions must be enabled; for example: EPD/PPD for UBR.

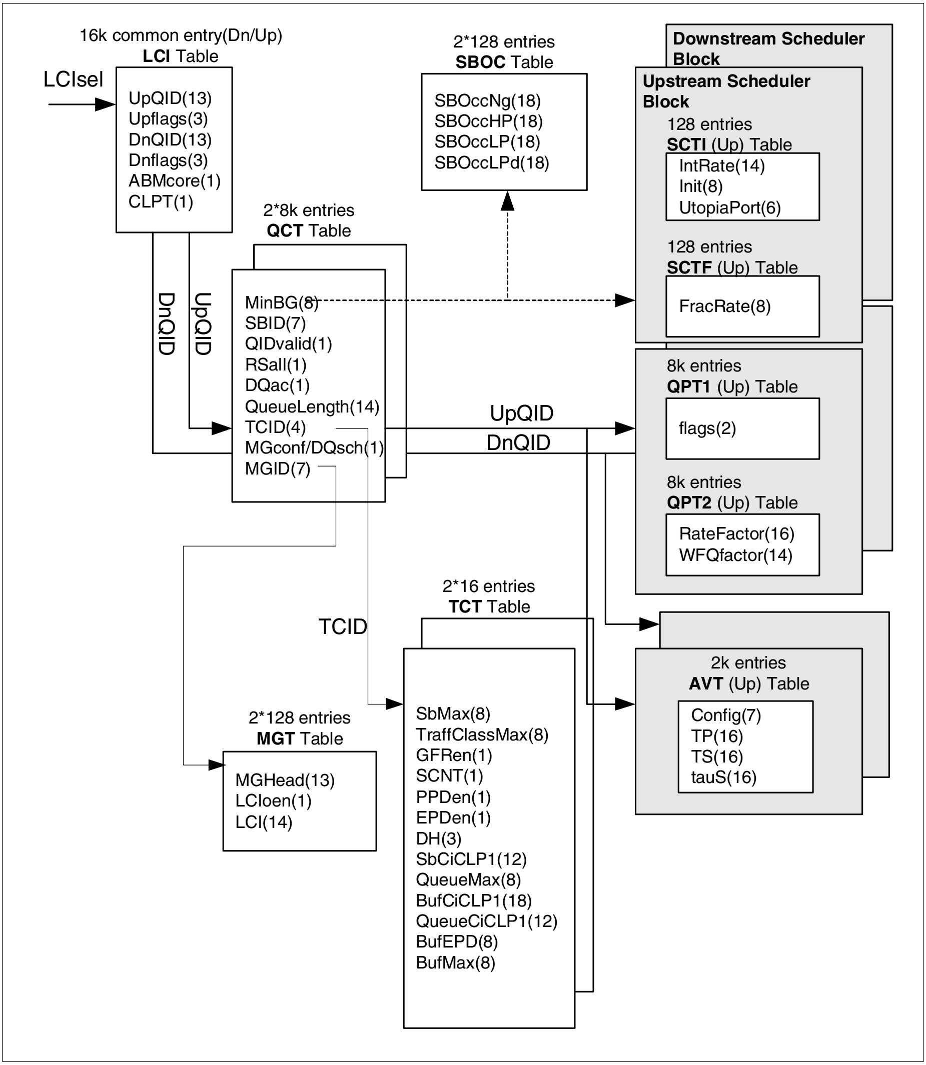


Figure 4-1 Parameters for Connection Setup (bit field width indicated)

Figure 4-1 refers to the following parameters:

ABM-3G Transfer Register	Parameter	Description	See page
LCI0	CLPT	If set, the CLP bit of the cells is ignored. (not to be set for GFR; optional for UBR)	7-192
	ABMcore	Selects upstream or downstream ABM-3G Core in the Uni-directional Mode	7-192
LCI1	DnQID	Points to the queue assigned to this connection in the downstream direction	7-193
	Dnflags	PPD(0), EPD(1), EOP(2)	7-193
LCI2	UpQID	Points to the queue assigned to this connection in the upstream direction	7-194
	Upflags	PPD(0), EPD(1), EOP(2)	7-194
QCT0	QueueLength	Status value (Read only)	7-214
QCT1	SBID	Selects the Scheduler Block	7-214
	QIDvalid	Enables queue; if cleared, cells directed to this queue are discarded and interrupt QID-INV (see 7-297f.) occurs	7-214
	TCID	Selects the Traffic Class	7-214
	RSall	Enables the dummy queue function	7-214
	DQac	Status bit	7-214
QCT2	MinBG	Minimum buffer guaranteed per queue	7-217
	MGID	Selects the VC-Merge Group the queue is assigned to	7-217
	MGconf/DQsch	Command bit to enable merge group assignment or dummy queue status indication	7-217

ABM-3G Transfer Register	Parameter	Description	See page
TCT0	BufMax	Defines maximum number of non-guaranteed cells allowed in the entire buffer for this traffic class	7-198
	BufEPD	Defines threshold for EPD/maximum[1)] for this traffic class for the entire buffer	7-198
	QueueCiCLP1	Combined threshold for each queue for CLP=1 cell discard in case of CLPT=0	7-198
TCT1	QueueMax	Defines threshold for each queue for this traffic class	7-201
	BufCiCLP	This 8-bit value determines a global cell filling level threshold with a granularity of 1024 cells that triggers early packet discard (EPD) for CLP=1 tagged frames used by GFR traffic class service (low watermark)	7-201
TCT2	SBCiCLP	This threshold determines a maximum number of low priority cells allowed to be stored per scheduler block with a granularity of 64 cells	7-204

ABM-3G Transfer Register	Parameter	Description	See page
TCT3	DH	Selects the hysteresis value for threshold evaluation	7-207
	EPDen	If set, EPD is enabled	7-207
	PPDen	If set, PPD is enabled	7-207
	SCNT	Selects whether accepted packets or cells are counted	7-207
	GFRen	This bit enables a modified EPD threshold evaluation for GFR traffic	7-207
	TrafClassMax	Defines maximum number of cells for this traffic class	7-207
	SBMax	Defines threshold for the number of cells of this traffic class allowed in the associated Scheduler	7-207
QPT1	flags	Initialization value	7-249
QPT2	RateFactor	Select value of peak rate limiter	7-253
	WFQFactor	Weight of scheduler input in 16,320 steps	7-254
SCTI	IntRate	Integer part of incremental value for Scheduler output rate	7-260
	Init	Initialization value for SB counter	
	UTOPIAPort	Specify UTOPIA port for this scheduler	7-260
SCTF	FracRate	Fractional part of incremental value for Scheduler output rate	7-269

[1)] mixed threshold: EPD if enabled; otherwise, maximum threshold

4.2.1 Setup of Queues

Before assigning a connection to a new queue, it should be verified to be empty, as some cells could remain from the previous connection. A queue is emptied by setting it ‘invalid’ while maintaining the scheduling parameters. An invalid queue will not except further cells; cells will be scheduled and de-queued, but not transmitted to the UTOPIA Interface. The queue length can be monitored by the external microprocessor.

4.2.2 Programming Queue Scheduler Rates and Granularities

4.2.2.1 Scheduler Block Scheduler

The aggregate theoretical **peak cell rate** of the SBS is calculated as follows:

$$PCR_{SBS} = \frac{SYSCLK}{32} \qquad [cells/s] \tag{3}$$

SYSCLK designates the core clock frequency. Each cell cycle needs 32 clock cycles. With the core SYSCLK = 51.84 [MHz] we have PCR_{SBS} = 1620000 [cells/s].

This corresponds to 686,8 [Mbit/s] for 53 byte cells

Note: Due to the need to perform internal SDRAM refresh cycles, the PCR_{SBS} contains empty cells. A discussion on the empty cell rate PCR_{empty}, which restricts the maximum scheduler block rate is contained in **Section 4.2.2.4**.

4.2.2.2 Programming the Scheduler Block Rates

For the **peak cell rate** of an SB we can have $PCR_{SB} = PCR_{SBS} - PCR_{empty}$.

In the following, let LC denote the logical channel assigned to an SB. Recall that a logical channel can subsume the whole output port or an reasonable subdivision.

Let CCR_{SB} denote the **configured cell rate** of an SB (i.e. the desired output cell rate).

$CCR_{SB(LC)} = PCR_{LC}$ must be chosen to match the peak cell rates of the LC as close as possible. Both permanent overload, leading to UTOPIA backpressure, and permanent underload, leading to poor channel utilization, should be avoided.

Overall, the following holds

$$\sum_{LC} CCR_{SB(LC)} \le PCR_{UTOPIA} \tag{4}$$

Note: For short periods of time PCR_{SB} as defined above can occur internally, independent of the particular CCR_{SB}

Deriving Internal Parameters from a Given CCR_{SB}

Internally the scheduler block output cell rate CCR_{SB} is represented by two parameters:

$T_{SB(i)}$[13:0], the 14 bit <u>integer</u> division factor

$T_{SB(f)}$[7:0], the 8 bit <u>fractional</u> division factor

These parameters are dimensionless and thus only indirectly represent the output rate. The following formulas show how to derive the two parameters assuming a given desired output rate CCR_{SB}:

First, a dimensionless floating point number T_{SB} is calculated from CCR_{SB} as follows:

$$T_{SB} = \frac{SYSCLK}{32 \times CCR_{SB}} \tag{5}$$

with T_{SB} constrained internally to

$$T_{SB} \le 2^{14} - \frac{1}{2^8} \tag{6}$$

Therefore T_{SBmax} = 16383,99609.

Given a particular T_{SB}, the internal parameters for the SB rate can be calculated:

The integer division factor is calculated as:

$$T_{SB(i)} = \lfloor T_{SB} \rfloor \tag{7}$$

The fractional division factor is calculated as:

$$T_{SB(f)} = \min(\lceil \langle T_{SB} - \lfloor T_{SB} \rfloor \rangle \times 2^8 \rceil, 255) \tag{8}$$

with $\lfloor X \rfloor$ designating the integer part of X and $\lceil X \rceil$ designating the next integer greater or equal to X.

The integer and fractional division factor defined above are referred to as **IntRate** and **FracRate** in the register description. Refer to **"USCTI/DSCTI" on Page 260** and **"USCTFT/DSCTFT" on Page 269**.

The **minimum cell rate** possible in an SB is configured with T_{SBmax} according to:

$$MCR_{SB} = \frac{SYSCLK}{32 \times T_{SBmax}} \tag{9}$$

The following **Table 4-2** shows the rate limits for the SB as a function of the system clock SYSCLK.

Table 4-2 Scheduler Block Rate Limits

SYSCLK [MHz]	**Cell cycle [ns]**	**PCR_{SB} [cells/s]**	**MCR_{SB} [cells/s]**	**MBR_{SB} [bit/s] (53)**
51.84	617	1556000	98.8769	41924
60	533	1811000	114.4409	48523

In **Table 4-3**, the numerical values of the integer and fractional divisors are shown for different desired CCR_{SB}. Due to the limited resolution of the internal rate representation, the delivered CCR_{SB} measured at the scheduler output does not always match exactly the desired CCR_{SB}. The delivered CCR_{SB} is calculated by:

$$CCR_{SB} = \frac{SYSCLK}{32 \times \langle T_{SB\langle i\rangle} + \frac{T_{SB\langle f\rangle}}{256}\rangle} \qquad (10)$$

Table 4-3 SB Rate Calculation Examples for SYSCLK = 51.84 MHz

Desired CCR_{SB} [cells/s]	T_{SB}	$T_{SB(i)}$	$T_{SB(f)}$	Delivered CCR_{SB} [cells/s]
4830	335.4037	335	104	4829.963
353108	4.5878	4	151	352953.191
1412429	1.1469	1	38	1410612.245

The deviation of the delivered CCR from the desired CCR is always less than 1 ‰ and improves towards lower CCR.

Scheduler Block Burst Limitation

Per scheduler block cell bursts can occur due to previously unused cell cycles. Each SB has an event generator that determines when this SB should be served based on the programmed SB rates. Because several SB may share one UTOPIA interface, it can happen that events cannot be served immediately due to active cell transfers of previous events. Such 'unused cell cycles' are counted and can be used for later cell bursts allowing a near 100% SB rate utilization. Cell bursts due to this mechanism are not rate limited.

The maximum burst size (MBS) generated due to previously counted 'unused cell cycles', is controlled by bit field MaxBurstS(3:0) in the range 0..15 cells (a minimum value of at least 1 is recommended). MaxBurst is programmed in registers **"UECRI/DECRI" on Page 263**.

Per SB MBS dimensioning depends on the burst tolerance (BT) of subsequent devices (buffer capacity and backpressure capability).

For example, if PHY(s) connected to the ABM-3G do not support backpressure and provide a 3-cell transmit buffer, a value in the range 1..3 is recommended to avoid PHY buffer overflows resulting in cell losses (e.g. typical for ADSL PHYs connected to the ABM-3G).

If a PHY is connected that supports port specific backpressure to prevent its transmit buffers from overflowing or provides sufficient buffering, the maximum value of 15 can be programmed, guaranteeing a near 100% scheduler rate utilization.

4.2.2.3 Programming the Common Real-Time Bypass

The Common Real-Time bypass (CRT) is denoted by the reserved logical queue identifier QID = 0. The rate assigned to the CRT bypass is programmed in the same way as the SB rates. The parameters **CRTIntRate** and **CRTFracRate** are described in registers **"UCRTRI/DCRTRI" on Page 278** and **"UCRTRF/DCRTRF" on Page 279**.

4.2.2.4 Programming the SDRAM Refresh Empty Cell Cycles

The programming of the rate for the internal SDRAM refresh generator is done by calculating the integer and fractional parts of the dimensionless value T_{empty} according to the SB formulas (**Equation (7)** and **Equation (8)**).

T_{empty} is constrained by the need to allow a minimum number of empty cell cycles for the internal SDRAM refresh generator according to:

$$T_{empty} \leq \frac{SYSCLK \times RefreshPeriod}{32 \times RefreshCycles} \qquad (11)$$

Given values of RefreshPeriod = 64ms, RefreshCycles = 4096 then

at SYSCLK = 51.84 MHz, T_{empty} = 25.3125, $T_{empty(i)}$ = 25, $T_{empty(f)}$ = 80

This renders PCR_{empty} = 64000 [cells/s] .

In case additional bandwidth needs to be reserved (e.g. for multicast operation in subsequent devices), a second maximum condition for parameter $T_{emptyMC}$ can be derived depending on the empty cell rate required for multicast bandwidth reservation.

The cell rate for the empty cell cycles PCR_{empty} is programmed by setting $T_{empty(i)}$ and $T_{empty(f)}$, referred to as **ECIntRate** and **ECFracRate** in the corresponding registers **"UECRI/DECRI" on Page 263** and **"UECRF/DECRF" on Page 264**.

4.2.2.5 Programming the PCR Limiter

For each logical queue, an optional peak rate shaper can be programmed.

Each cell passing the PCR limiter needs at least 2 cell cycles to emit. This limits the maximum PCR that can be shaped to:

$$PCR_{RSmax} = \frac{SYSCLK}{32} \times \frac{1}{2} \qquad [cells/s] \qquad (12)$$

The resolution of the PCR limiter is determined by the global parameter TstepC, common for all shapers in an ABM-3G core.

TstepC is configured per direction by the field TstepC[2:0] described in **“USCONF/DSCONF” on Page 246**. Internally the shaper use a derived value Tstep with the following interpretation:

$$Tstep = 2^{TstepC - 8} \tag{13}$$

This renders Tstep in the range 1/2 ... 1/256.

Smaller values for TstepC and in consequence Tstep imply lower shaping rates.

Given a particular TP, the resulting PCR shaping rate is calculated as follows:

$$PCR_{RS} = \frac{SYSCLK}{32} \times Tstep \times \frac{64}{TP} \tag{14}$$

Vice versa, for a given PCR, the corresponding TP value is calculated as:

$$TP = \left\lceil \frac{SYSCLK}{32} \times Tstep \times \frac{64}{PCR_{RS}} \right\rceil \tag{15}$$

The value of parameter TP is constrained internally to:

$$TP \le 2^{16} - 2^{6} \tag{16}$$

Therefore, TP_{max} = 65472.

Though possible to specify, very low values of TP do not make much sense, because the shaper is limited by PCR_{RSmax} in any case (see **Equation (12)**). Together with **Equation (14)** this leads to the following constraint on TP:

$$TP \ge \max(1, Tstep \times 128) \tag{17}$$

The following special case must be considered:

TP = 0 disables the shaper, connecting the queue directly to the level 1 schedulers (RR / WFQ).

Table 4-4 shows minimum PCR shaper rates for all the possible values of TstepC calculated at a SYSCLK of 51.84 MHz and 60 MHz with TPmax and **Equation (14)**.

Table 4-4 Minimum Shaper Rates as a Function of TstepC and SYSCLK

TstepC	1/Tstep	SYSCLK = 51.84 [MHz]		SYSCLK = 60 [MHz]	
		PCR_{RSmin} [cells/s]	PBR_{RSmin} [bit/s]	PCR_{RSmin} [cells/s]	PBR_{RSmin} [bit/s]
0	256	6.185	2622	7.160	3036
1	128	12.371	5245	14.320	6072
2	64	24.743	10491	28.639	12143
3	32	49.487	20982	57.278	24286
4	16	98.975	41965	114.555	48572
5	8	197.950	83930	229.110	97143
6	4	395.900	167861	458.219	194285
7	2	791.800	335723	916.437	388569

The accuracy of the shaping rate is defined as:

$$acc_{PCR} = \frac{PCR_{in} - PCR_{out}}{PCR_{out}} \tag{18}$$

with PCR_{in} denoting the desired PCR and PCR_{out} denoting the delivered PCR, which is always less than PCR_{in}.

PCR_{out} is calculated by first deriving TP from PCR_{in} in **Equation (15)** and then substituting TP in **Equation (14)**.

The accuracy improves towards lower shaping rates and higher values of TstepC.

Note: The improvement is not monotonic and depends on the rounding error made at the calculation of TP. However, from the formulas given above, it can be deduced that the accuracy is always better than:

$$acc_{PCR} \leq \frac{PCR_{in}}{2 \times SYSCLK \times Tstep} \tag{19}$$

Table 4-5 shows the accuracy of the shaping rate at some characteristic rates for three selected values of TstepC.

Table 4-5 Shaper Accuracy as a Function of desired PCR and TstepC

desired PCR	acc_{PCR} at SYSCLK = 51.84 [MHz]		
	TstepC = 0	**TstepC = 4**	**TstepC = 7**
32	0.000059	not possible	not possible
64	0.000138	not possible	not possible
170	0.000271	0.000009	not possible
4830	0.001774	0.000286	0.000007
101957	0.006934	0.006934	0.001081
353108	0.425621	0.034140	0.001288

Regarding the inevitable jitter (CDV) produced by the rate shaper due to its limited accuracy, it improves towards higher shaping rates and higher values of TstepC.

The value of parameter TP derived above is programmed into the field **RateFactor** in register “UQPT2T0/DQPT2T0” on Page 253.

Note: A value of 0 in field RateFactor disables both the PCR limiter and the leaky bucket shaper. Values other than 0 in field RateFactor are ignored for queues with an additional leaky bucket shaper enabled. The parameter TP defined there overrides. See Section 4.2.2.6.

4.2.2.6 Programming the Leaky Bucket Shaper

Regarding the Leaky Bucket Shaper, the formulas given previously in Section 4.2.2.5 apply accordingly when substituting SCR for PCR and TS for TP.

In addition, given MBS, the parameter tauS is calculated as:

$$tauS = (MBS - 1) \times \left(\frac{TS - TP}{64}\right) \tag{20}$$

with tauS constrained internally to:

$$tauS \le 2^{16} - 2^{10} \tag{21}$$

Therefore, $tauS_{max}$ = 64512.

Given a particular tauS, the burst tolerance BT and the corresponding MBS produced by the leaky bucket shaper is calculated as:

$$BT = \frac{tauS}{Tstep} \times \frac{32}{SYSCLK} \qquad [sec] \tag{22}$$

and

$$MBS = \left\lfloor 1 + \frac{tauS \times 64}{TS - TP} \right\rfloor \qquad [cells] \tag{23}$$

The maximum BT has been derived from $tauS_{max}$ and is shown in **Table 4-6** for different values of TstepC and SYSCLK.

Table 4-6 Maximum BT as a Function of TstepC and SYSCLK

TstepC	1/Tstep	BT [s]	
		SYSCLK = 51.84 [MHz]	SYSCLK = 60 [MHz]
0	256	10.192	8.807
1	128	5.097	4.403
2	64	2.548	2.201
3	32	1.274	1.100
4	16	0.637	0.550
5	8	0.318	0.275
6	4	0.159	0.137
7	2	0.079	0.068

Refer to **"AVT Context Table: VBR Shaping (Table Layout)" on Page 97** for a detailed description and layout of the parameter fields.

4.2.2.7 Guaranteed Cell Rates and WFQ Weight Factors

The total WFQ scheduler rate is calculated as follows:

$$GCR_{WFQ} = CCR_{SB} - ECR_{RT(SB)} \tag{24}$$

with CCR_{SB} being the configured SB rate as defined in **Section 4.2.2.2** and $ECR_{RT(SB)}$ being the effective cell rate of the high priority RR scheduler in the SB.

GCR_{WFQ} is distributed to the queues in proportion to the queue's relative weight factor 1/ T_{WFQ}.

The guaranteed cell rate for connection i is calculated according to:

$$GCR_i = \frac{GCR_{WFQ}}{T_{WFQ(i)} \times \sum_{\forall k \in \text{Active Queues}} 1/T_{WFQ(k)}} \tag{25}$$

with T_{WFQ} constrained internally to:

$$T_{WFQ} \le 2^{14} - 2^{6} \tag{26}$$

Therefore, T_{WFQmax} = 16320.

The minimum guaranteed cell rate at a given GCR_{WFQ} is therefore:

$$GCR_{min} = \frac{GCR_{WFQ}}{T_{WFQmax}} \tag{27}$$

Assuming a fixed given GCR_{min}, then for any given GCR >= GCR_{min} the corresponding T_{WFQ} can be calculated as:

$$T_{WFQ} = \left\lfloor \frac{GCR_{min} \times T_{WFQmax}}{GCR} \right\rfloor \tag{28}$$

The integer function in equation above selects the next smaller value of the integer T_{WFQ}, that is to say, the weight factor is higher than required and, thus, the queue is served slightly faster in order to guarantee the rate.

Two special cases must be considered:

T_{WFQ} = 0 is used to assign the queue to the high priority round robin scheduler.

T_{WFQ} = 16383 is used to assign the queue to the low priority round robin scheduler.

T_{WFQ} is referred to as parameter **WFQFactor** in the register description **"UQPT2T1/ DQPT2T1" on Page 254**.

4.2.3 ABM-3G Configuration Example

In this section, a popular mini-switch scenario (**Figure 4-7**) is used to describe the most important points for the software configuration of the ABM-3G. Among other things, the following fixed assignments can be made in software by the user:

- Assignment of Schedulers to PHYs and programming of Scheduler output rates
- Definition of the necessary traffic classes
- Assignment of the queues to the traffic classes
- Assignment of the queues (QIDs) to the Schedulers (SBIDs)

Assignment of Schedulers and Programming Output Rates

The ABM-3G has 256 Schedulers (128 in the upstream direction and 128 in the downstream direction). In this example each xDSL device is assigned to a separate Scheduler (this guarantees each xDSL device a 2-Mbit/s data throughput without bandwidth restrictions caused by the other xDSL devices); then, 255 xDSL devices can be connected. The 256th Scheduler will be occupied by the E3 uplink to the public network. The assignment of the Schedulers to the PHYs is totally independent and even such a strong asymmetrical structure as in (**Figure 4-7**) can be supported. The output rates of the Schedulers must be programmed in such a way that the total sum does not exceed 622 Mbit/s (payload rate). From the example, the following result is derived: 255 x 2 Mbit/s + 1 x 34 Mbit/s = 544 Mbit/s ≤ 622 Mbit/s.

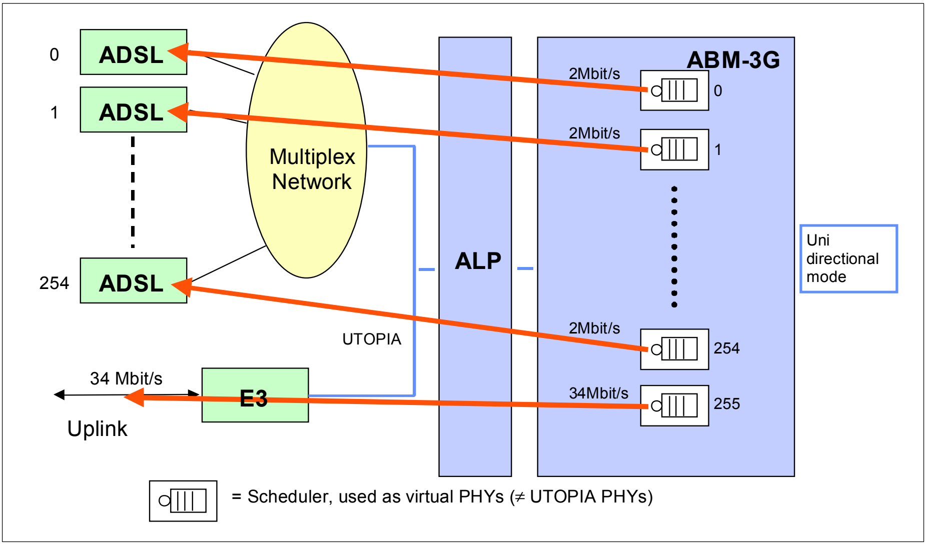


Figure 4-7 ABM-3G Application Example: DSLAM

Definition of Necessary Traffic Classes

The ABM-3G allows up to 16 traffic classes to be defined by Traffic Class Table RAM entry via the registers TCT0 to TCT3 (see **Page 198**f). In this example, there are 3 traffic classes:

- CBR (real-time) = traffic class 1
- GFR (non-real-time) = traffic class 2
- UBR (non-real-time) = traffic class 3

Assignment of the Queues to the Traffic Classes

Each queue must relate to a defined traffic class according to the Queue Configuration Table RAM entry via the TCID(3:0) bits of the QCT table.

Assignment of the Queues (QIDs) to the Scheduler Blocks (SBIDs)

Every Scheduler Block (SB) possesses a certain number of queues depending on the assignment by the user of the SBID(5:0) bits of register **"QCT1" on Page 214**. In the example, every ADSL device has four data connections so that four queues per SB are necessary. Each SB of the ABM-3G has one real-time queue and an arbitrary number of non-real-time queues. For SB 0..254, indicate that the first queue belongs to Traffic Class 1, the 2nd and 3rd Queue to Traffic Class 2, and the 4th Queue to Traffic Class 3. There are 1020 (1..1020) queues altogether for SB 0..254. The 256th SB must be able to serve the 255 xDSL devices (255 SBs and appropriate queues). Thus, SB 255 has 255 x 2 = 510 non-real-time queues as every SB from 0..254 possesses two GFR non-real-time queues (GFR has a guaranteed minimum rate; thus, each GFR queue needs a per VC queueing). The 255 UBR queues of SBs 0..254 need only one UBR queue at the 256th SB as UBR has no guaranteed minimum rate. As every SB has only one real-time queue, the 255 real-time queues from SBs 0..254 flow into the one real-time queue of SB 255. Therefore, SB 256 needs the assignment of 510 (GFR) + 1 (UBR) + 1 (CBR) = 512 queues.

4.2.4 Normal Operation

In normal operation, no microprocessor interaction is necessary as the ABM-3G chip does all queueing and scheduling automatically. For maintenance purposes, periodically the microprocessor could read out the counters for buffer overflow events. Some overflow events may also be programmed as interrupts.

4.2.5 Bandwidth Reservation

Due to the WFQ Scheduler concept of the ABM-3G, the Connection Acceptance Check (CAC) is very simple:

- Check if the Guaranteed Rate of the connection fits within the spare bandwidth of the Scheduler.

For the definition of the Guaranteed Rate, see Table 3-24. Mathematically, the CAC can be reduced to the following formulas:

For all connections make sure that no overbooking of the configured scheduler output rate CCR_{out} occurs, i.e.:

$$\sum_i GCR_i = CCR_{out} \tag{29}$$

For real-time connections, (CBR, rt-VBR) Equation (29) is the only condition required.

For non-real-time connections or connections using the WFQ scheduler, additional conditions must be fulfilled.

VBR and UBR+ connections must be setup in per VC queueing configurations, that is, an empty queue must be found for the connection. The Guaranteed Rate determines the weight of the queue.

4.2.5.1 Bandwidth Reservation Example

As an example, an access network multiplexer is assumed with ADSL lines and an E3 uplink. CBR and UBR+ connections are supported. A minimum Guaranteed Rate of GR_{min} = 19.2 Kbps is selected. This allows GR up to 314.57 Mbit/s with increasing granularity for higher values.

This behavior is well suited to the Guaranteed Rates which are minimum or sustainable rates. The values for MCR and SCR will be well below 10 Mbit/s for public networks. In high speed LANs with high MCR and SCR values, a higher minimum rate could be selected.

Additionally, it is assumed that three types of line interfaces (PHY) exist in the system: 34 Mbit/s for the uplink, ADSL rates of 8 Mbit/s downstream, and 0.6 Mbit/s upstream. For each PHY, a maximum possible weight factor 1/n exists: n_{max} = 9, n_{max}= 39, and n_{max} = 524, respectively.

Two types of non-real-time connection are defined with Guaranteed Rates of 100 kbit/s and 20 Kbps with the weight factors 1/n, n_{100} = 3146 and n_{20} = 15730, respectively. The 100 Kbps connections would be used for the downstream direction, and the 20 Kbps connections for the upstream direction. Table 4-8 provides the maximum number of connections possible on each PHY.

Table 4-8 Number of Possible Connections per PHY

PHY	GR = 100 Kbps	GR = 20 Kbps
34 Mbit/s	349	1747
8 Mbit/s	80	403
0.6 Mbit/s	6	30

For example, if the maximum number of connections for each Subscriber is fixed (such as 5 data connections), the queues can be pre-configured for each Subscriber so that only the LCI assignment must be changed when a connection is setup or released.

4.2.6 Buffer Reservation

In addition to the bandwidth reservation, buffer space must be assigned by the appropriate setting of discard thresholds.

Figure 4-9 shows an example of threshold configurations for four traffic classes (real-time, nrt-VBR, GFR, UBR).

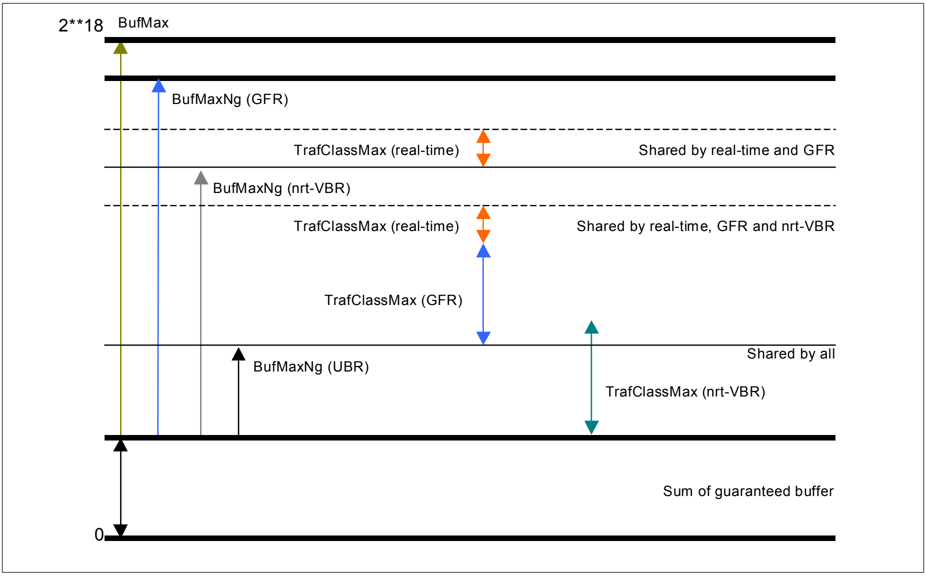


Figure 4-9 Example of Threshold Configuration

4.2.7 Support of Standard ATM Service Categories

The following sections provide some insight into how the ABM-3G supports connections belonging to the well known ATM Forum service categories.

4.2.7.1 CBR Connections

These connections should use the real-time bypass of the respective scheduler block. However, if two priority levels for real-time connections must be offered, a slightly lower real-time performance can be achieved by using the WFQ scheduler with maximum weight. In this case, the bandwidth must fit into the WFQ scheduler (conditions **(1)** and **(2)** in **"Bandwidth Reservation" on Page 116**).

4.2.7.2 rt-VBR Connections

These connections can be treated like CBR connections with a guaranteed cell rate less than or equal to the Peak Cell Rate (PCR). Depending on the behavior of the sources, a statistical benefit could be obtained by reserving less than PCR.

As an example, assume 1000 connections with compressed voice are multiplexed on a link. PCR is 32 Kbps, but on average only 16 Kbps. SCR is 8 Kbps. Hence, instead of reserving 32 Mbit/s for the ensemble of connections, only 16 Mbit/s must be reserved. The large number of connections guarantees that the mean sum rate of 16 Mbit/s is exceeded only with a negligible probability.

4.2.7.3 nrt-VBR Connections

For these connections, the three parameters PCR, SCR, and MBS are given. One queue is reserved for each nrt-VBR connection with SCR programmed as the weight of the respective Scheduler queue. The maximum queue size is set to MBS plus approximately 100 cells for cell level bursts. If the buffer space reserved for nrt-VBR connections is set to the sum of all MBS, it is guaranteed that no cell is lost. However, with a large number of nrt-VBR connections, the total reserved buffer can be smaller with a negligible number of cell losses.

For the PCR, no adjustment is necessary as the rates of the queues of a Scheduler always adjust automatically to the maximum possible values.

As an option for network endpoints, for both rt-VBR and nrt-VBR the PCR and SCR may be shaped by the PCR limiter and SCR leaky bucket shaper as described in **Chapter 3.4.2.4**. This is useful at network boundaries (UNI/NNI) to provide conforming traffic to the subsequent policer.

4.2.7.4 UBR+ Connections

UBR+ connections are UBR connections with MCR. They must be setup in individual queues with the weight factor guaranteeing the MCR.

To enhance the overall throughput, the EPD/PPD function is enabled.

4.2.7.5 GFR Connections

GFR Connections are setup like UBR+ connections with a Guaranteed Rate in individual queues, with the weight factor guaranteeing the rate for the high-priority packets. The threshold for the discard for low-priority packets must be set accordingly.

4.2.7.6 UBR Connections

As described in **"Bandwidth Reservation" on Page 116**, one queue per Scheduler is reserved for UBR connections with the smallest weight assigned. All UBR connections share this queue. EPD/PPD can be enabled as the relevant parameters are stored per connection (LCI table).

4.2.7.7 Generic Service Classes

Besides the standard ATM Forum service categories, other generic service classes can be flexibly supported by the ABM-3G.

Quality of service differentiation in terms of absolute and relative guarantees can be achieved for any traffic stream that is segmentable into the ABM-3G cell format.

4.3 Connection Teardown Example

Teardown of Queues

Disabling a queue via the queue-disable bit does not clear the cells in the queue, but:

- The acceptance of the queue for new cells is disabled
- The queue is still served, but the cells are discarded internally

Normally, at the time a queue is cleared, there will be no more cells in the queue. This can be checked by reading the queue length. In case of a highly filled queue which is served slowly, the time to empty the queue could be long. To deplete the queue more quickly, its weight can be increased temporarily. However, because the discarded cells produce idle times on the UTOPIA output, the chosen weight factor should not be too high.

4.4 AAL5 Packet Insertion/Extraction

Refer to **Chapter 3.2.3** for a more general description.

4.4.1 AAL5 Packet Insertion

First, the header octets are assembled from the VPI, VCI and/or LCI and written to the corresponding registers UA5TXHD0/DA5TXHD0 and UA5TXHD1/DA5TXHD1. The CPCS-UU and CPI are also provided to register UA5TXTR/DA5TXTR. The packet payload length is written to UA5TXCMD/DA5TXCMD together with the AAL5EN flag. Four octets of payload are written to the two data registers UA5TXDAT0/DA5TXDAT0 and UA5TXDAT1/DA5TXDAT1. The Status register UA5SARS/DA5SARS should be read afterwards to check the current state of the assembly unit. The assembly of the cells is done without interaction of the microprocessor.

4.4.2 AAL5 Packet Extraction

If an AAL5 interrupt indicates that an AAL5 packets has arrived first the cell header should be read. Before each access to the data registers the status register UA5SARS/DA5SARS should be read to get the current status of the extraction unit.

As long as the AAL5 status register does not indicate End of Packet (PE), the payload can be received from the data registers UA5RXDAT0/DA5RXDAT0 and UA5RXDAT1/DA5RXDAT1. This data registers should always be read together. If the PE flag is set the next read accesses to the both data registers will return the last payload octets. After this access the Status register still contains the PE flag but additionally a length information of the packet stored in the OV flags. Again the data registers are read to get the trailer of the packet (CPCS-UU and CPI) and the Status Byte. Depending on the packet length there are four possibilities for the mapping of these octets to the two data registers, indicated by the OV flags. The four cases are depicted in **Figure 4-10**.

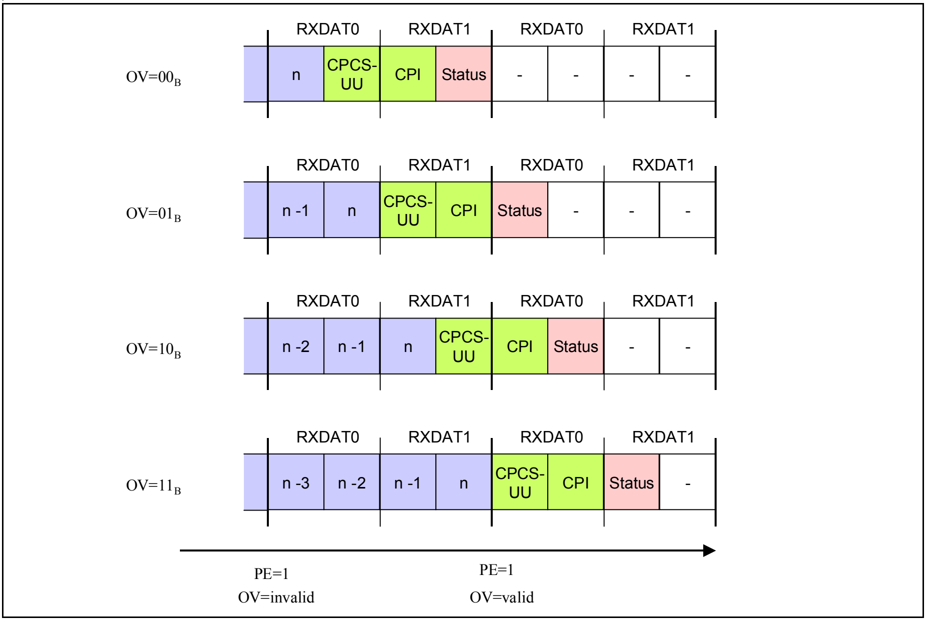


Figure 4-10 AAL5 Extraction: End of packet, Trailer and Status Byte

The Status Byte returns some information about the received packet:

Bit	7	6	5	4	3	2	1	0
	unused		END	ICHN	CLP	CGST	UUE	CPIE

Table 4-11 AAL5 Status Byte

Flag	Description
END	Error bit. Set if a cell with a different header is received before the end of a packet. Should not occur if VC merge is used, but the user might have a programming error.
ICHN	Invalid channel number. Indicates a change of the cell header before end of packet.
CLP	CLP=1 in at least one cell of the packet
CGST	Congestion occurred, i.e. PT(1)=1 in at least one cell of the packet
UUE	CPCS-UU value is not 0; no other action
CPIE	CPI value is not 0; no other action

Note: If a packet is extracted too slowly, an MUXOV interrupt might occur. To avoid this, either mask the MUXOV interrupt during extraction or reduce the output rate of the scheduler.

4.5 Exception Handling

The ABM-3G provides a set interrupts classified as:

- Fatal
- Notification
- Normal

Fatal interrupts

It is recommended to reset the device upon occurrence of a ‘fatal interrupt’ which is generated by the ABM-3G detecting internal consistency violations.

Notifications/Normal interrupts

- Control interrupts for activation/de-activation of VC-merge groups
- Control interrupts for activation/de-activation of ‘dummy’ queues

5 Interface Description

5.1 UTOPIA L2 Interfaces (PHY side)

The UTOPIA Interface to the PHY is ATMF UTOPIA Level 2 and Level 1 compliant. The interface can be configured in Master or Slave Mode. Internal UTOPIA FIFOs guarantee Head-of-Line blocking-free operation in both modes. Each interface direction (receive and transmit) is independently clocked. The PHY side and backplane side UTOPIA Interfaces are identical with minor exceptions as described in the subsequent chapters.

5.1.1 URXU: UTOPIA Receive Upstream (PHY side)

The UTOPIA Receive Interface supports up to 48 PHY addresses that can be individually enabled. In Master Mode and Slave Mode, 48 PHYs are supported in four groups (4*12 scheme).

Note: In Slave Mode, the interface responds to all enabled port addresses.

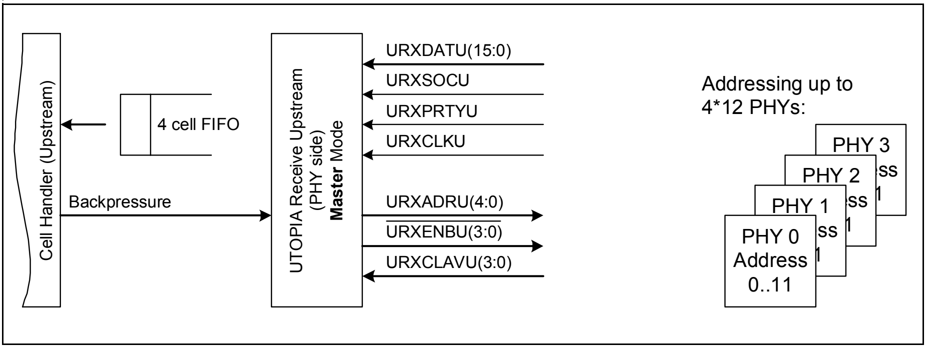


Figure 5-1 UTOPIA Receive Upstream Master Mode

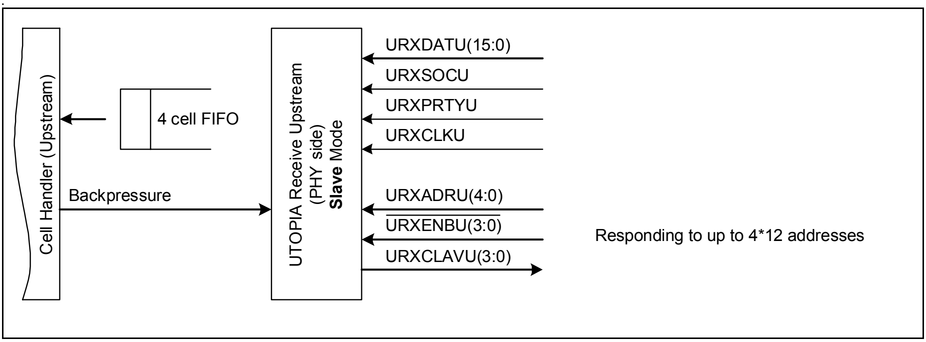


Figure 5-2 UTOPIA Receive Upstream Slave Mode

Head of Line Blocking Avoidance

The internal Cell Handler Unit accepts any cell from the common UTOPIA receive FIFO to either accept the cell or discard the cell depending on threshold decisions. Thus, no HOL blocking can occur. Optionally, internal thresholds can be enabled to generate backpressure to UTOPIA port groups in a fixed scheme:

- Threshold 0 effects ports {0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44}
- Threshold 1 effects ports {1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45}
- Threshold 2 effects ports {2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46}
- Threshold 3 effects ports {3, 7, 11, 15, 19, 23, 27, 31, 35, 39, 43, 47}

In case of pending backpressure, a specific port reacts in the same way as being disabled:

- Master Mode:
  A backpressured (or disabled) port is deleted from the polling scheme.
- Slave Mode:
  A backpressured (or disabled) port does not generate a cell available signal indication.

Note: The internal backpressure does only effect the polling/response scheme. The UTOPIA receive FIFO is served in any case to avoid HOL blocking.

5.1.2 UTXD: UTOPIA Transmit Downstream (PHY side)

The UTOPIA transmit interface supports up to 48 PHY addresses that can be individually enabled.

In Master Mode, 48 PHYs are supported in four groups (4*12 scheme).

In Slave configuration, two polling modes are supported:

- Up to 48 Ports in 4 groups (4*12 scheme)
- Up to 31 Ports in 1 group (1*31 scheme)

Note: In Slave Mode, the interface responds to all enabled port addresses in either scheme.

A cell buffer pool of 64 cells is provided for UTOPIA port specific queues. The number of enabled ports determines the queue length that can be configured. At least one cell buffer per queue is provided.

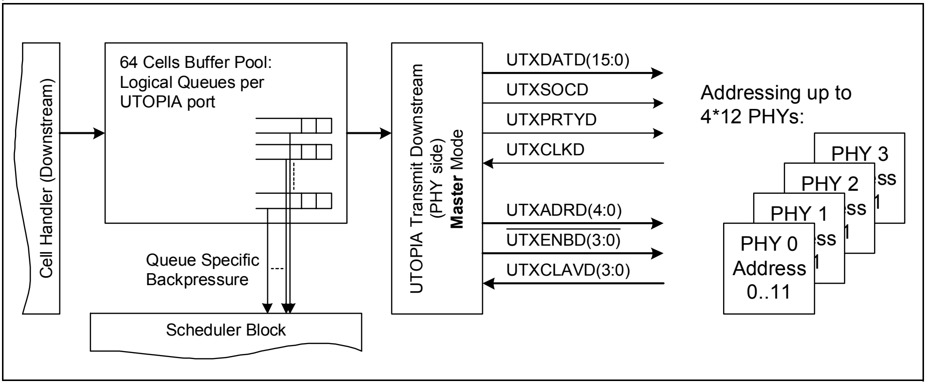


Figure 5-3 UTOPIA Transmit Downstream Master Mode

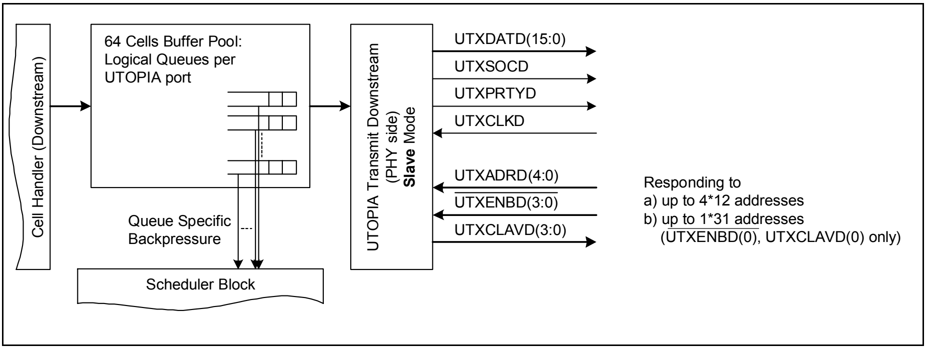


Figure 5-4 UTOPIA Transmit Downstream Slave Mode

Head of Line Blocking Avoidance

The internal Cell Handler Unit forwards cells to UTOPIA port-specific queues. In case of a filled queue, queue-specific backpressure is signalled to all schedulers that are associated to that queue/port prohibiting further cell emits. Thus no HOL blocking can occur.

5.1.3 UTOPIA Port/Address Mapping (PHY side)

Table 5-1 describes the mapping of UTOPIA addresses and groups to port numbers.

Table 5-1 Port/Address Mapping

Port Number	Group 0		Group 1	Group 2	Group 3
Address	**Slave Mode 1*31**	**Slave Mode 4*12 and Master Modes**			
30	30	-	-	-	-
...	...	...	...	...	...
12	12	-	-	-	-
11	11	11	23	35	47
10	10	10	22	34	46
9	9	9	21	33	45
8	8	8	20	32	44
7	7	7	19	31	43
6	6	6	18	30	42
5	5	5	17	29	41
4	4	4	16	28	40
3	3	3	15	27	39
2	2	2	14	26	38
1	1	1	13	25	37
0	0	0	12	24	36

5.1.4 Functional UTOPIA Timing (PHY side)

The functional timing is compatible to ATMF UTOPIA Level 2 standard [4] and ATMF UTOPIA Level 1 standard [3] respectively.

Remark 1

The ABM-3G UTOPIA Interfaces in Master Mode always introduce at least 1 idle clock between transmission or reception of subsequent ATM cells.

Remark 2

The ABM-3G UTOPIA Interfaces in **Level 1 Slave Mode** do not support constant active enable signals $\overline{\text{UTXENBi}}$/$\overline{\text{URXENBi}}$ (i = {D(Downstream); U(Upstream)}).

The enable signals must be deasserted with each cell cycle.

5.1.5 UTOPIA Master Mode Polling Scheme (PHY side)

The polling scheme is based on a port priority list. A serviced port is automatically moved to the end of the priority list. The priority list port sequence is based on incrementing addresses; for a given address, the port numbers are in increasing order:

Table 5-2 Port Polling Sequence

Address	**0**				**1**				**2**				**3**				**4**
Sequence	0	12	24	36	1	13	**25**	37	2	14	26	38	3	15	27	39	4
Priority	decreasing priority ->					min Prio.	**max Prio.**	decreasing priority ->									

Example

Assume Port 25 (printed bold in example pattern) is at the top of the priority list and gets serviced. Now, the list top pointer is moved to the next entry which is Port 37 (i.e. Port 25 becomes the end of the list).

Note: Disabled or internally backpressured ports are deleted from the priority list. Polling operation of Receive and Transmit interfaces is independent of each other.

5.1.6 UTOPIA Cell Format (PHY side)

The following sections describe the cell format expected by the ABM-3G, depending on the selected mapping mode. Transmitted cells have the same format.

The ABM-3G may modify the LCI field (VC-Merge function), depending on the configuration. For internal use, also field UDF2 may be modified. The CRC10 field gets recalculated accordingly.

5.1.6.1 UTOPIA Level 2 Standard Cell Formats

Table 5-3 Standardized UTOPIA Level 2 Cell Format (16-bit)

<table>
<tr><th>bit:</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td colspan="12">VPI(11:0)</td><td colspan="4">VCI(15:12)</td></tr>
<tr><td>1</td><td colspan="12">VCI(11:0)</td><td colspan="3">PT(2:0)</td><td>CLP</td></tr>
<tr><td>2</td><td colspan="8">UDF1</td><td colspan="8">UDF2</td></tr>
<tr><td>3</td><td colspan="8">Payload Octet 1</td><td colspan="8">Payload Octet 2</td></tr>
<tr><td>4</td><td colspan="8">Payload Octet 3</td><td colspan="8">Payload Octet 4</td></tr>
<tr><td>...</td><td colspan="8">:</td><td colspan="8">:</td></tr>
<tr><td>26</td><td colspan="8">Payload Octet 47</td><td colspan="8">Payload Octet 48</td></tr>
</table>

Note: All Fields According to Standards, Unused Octets Shaded

Table 5-4 Standardized UTOPIA Level 2 Cell Format (16-bit): OAM Cells

<table>
<tr><th>bit:</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td colspan="12">VPI(11:0)</td><td colspan="4">VCI(15:12)</td></tr>
<tr><td>1</td><td colspan="12">VCI(11:0)</td><td colspan="3">PT(2:0)</td><td>CLP</td></tr>
<tr><td>2</td><td colspan="8">UDF1</td><td colspan="8">UDF2</td></tr>
<tr><td>3</td><td colspan="4">OAM Type(3:0)</td><td colspan="4">Function Type(3:0)</td><td colspan="8">Function Specific Octet 1</td></tr>
<tr><td>4</td><td colspan="8">Function Specific Octet 2</td><td colspan="8">Function Specific Octet 3</td></tr>
<tr><td>...</td><td colspan="8">:</td><td colspan="8">:</td></tr>
<tr><td>25</td><td colspan="8">Function Specific Octet 44</td><td colspan="8">Function Specific Octet 45</td></tr>
<tr><td>26</td><td colspan="6">Reserved</td><td colspan="10">CRC10</td></tr>
</table>

Note: All fields according to standards, unused octets are shaded.

5.1.6.2 LCI Mapping Mode: VPI Mode

In Mapping Mode ‘VPI’, the ABM-3G expects a 12-bit local connection identifier in the location of the VPI field. Mapping Mode ‘VPI’ is configured via bit field LCIMOD(1:0)=’00’ in Register **“MODE1” on Page 312**.

Table 5-5 Standardized UTOPIA Level 2 Cell Format (16-bit)

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LCI(11:0)												VCI(15:12)			
1	VCI(11:0)												PT(2:0)			CLP
2	UDF1								UDF2							
3	Payload Octet 1								Payload Octet 2							
4	Payload Octet 3								Payload Octet 4							
...	:								:							
26	Payload Octet 47								Payload Octet 48							

5.1.6.3 LCI Mapping Mode: VCI Mode

In Mapping Mode ‘VCI’, the ABM-3G expects a 16-bit local connection identifier in the location of the VCI field. Mapping mode ‘VCI’ is configured via bit field LCIMOD(1:0)=’01’ in Register **“MODE1” on Page 312**.

Table 5-6 Standardized UTOPIA Level 2 Cell Format (16-bit)

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	VPI(11:0)												LCI(15:12)			
1	LCI(11:0)												PT(2:0)			CLP
2	UDF1								UDF2							
3	Payload Octet 1								Payload Octet 2							
4	Payload Octet 3								Payload Octet 4							
...	:								:							
26	Payload Octet 47								Payload Octet 48							

Since the ABM-3G supports 16 K connections, the MSB bits 15 and 14 of the LCI must match the selected quarter segment. Otherwise, the cells are automatically forwarded to the global real time bypass queue (Queue 0) and may be handled by a subsequent ABM-3G device.

5.1.6.4 LCI Mapping Mode: Infineon Mode

In Mapping Mode 'Infineon', the ABM-3G expects a 16-bit local connection identifier in the location of the VPI field and the UDF1 byte as shown below. Mapping Mode 'Infineon' is configured via bit field LCIMOD(1:0)='10' in Register **"MODE1" on Page 312**.

Table 5-7 Standardized UTOPIA Level 2 Cell Format (16-bit)

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LCI(11:0)												VCI(15:12)			
1	VCI(11:0)												PT(2:0)			CLP
2	LCI(13:12)		transparent				LCI(15:14)		UDF2							
3	Payload Octet 1								Payload Octet 2							
4	Payload Octet 3								Payload Octet 4							
...	:								:							
26	Payload Octet 47								Payload Octet 48							

Since the ABM-3G supports 16 K connections, the MSB bits 15 and 14 of the LCI must match the selected quarter segment. Otherwise the cells are automatically forwarded to the global real time bypass queue (Queue 0) and may be handled by a subsequent ABM-3G device.

5.1.6.5 LCI Mapping Mode: Address Reduction Mode

In Mapping Mode 'Address Reduction', the ABM-3G generates a 16-bit local connection identifier based on the marked bit fields. Mapping Mode 'Address Reduction' is configured via bit field LCIMOD(1:0)='11' in Register **"MODE1" on Page 312**.

Table 5-8 Standardized UTOPIA Level 2 Cell Format (16-bit)

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	VPI(11:0)												VCI(15:12)			
1	VCI(11:0)												PT(2:0)			CLP
2	transp.		optional PNUT(5:0)						UDF2							
3	Payload Octet 1								Payload Octet 2							
4	Payload Octet 3								Payload Octet 4							
...	:								:							
26	Payload Octet 47								Payload Octet 48							

To generate an Local Connection Identifier (LCI), programmable parts of the fields VCI and VPI optionally supplemented by the UTOPIA port number can be used as basis. The UTOPIA port number is internally provided either by side-band signals (no modifications to ATM cell) or mapped into either the UDF2 field of the cells. In this case, the respective UDF2 field is not transparent.

Address Reduction Mode is described in **Chapter 3.2.4**.

5.2 UTOPIA L2 Interface (Backplane side)

5.2.1 URXD: UTOPIA Receive Downstream (Backplane side)

The UTOPIA Receive Downstream Interface is identical to the UTOPIA Receive Upstream Interface as described in **Chapter 5.1.1**.

Standard Exceeding UTOPIA Feature

To support system architectures that require a bandwidth overprovisioning from the backplane, the URXD can be operated up to 60 MHz which corresponds to a data rate of 795 Mbit/s received from the backplane. This provides an overprovisioning factor of 1.32 to OC12 data rate on the line side as described in **Chapter 3.1.1**.

5.2.2 UTXU: UTOPIA Transmit Upstream (Backplane side)

The UTOPIA Transmit Upstream Interface is identical to the UTOPIA Transmit Downstream Interface as described in **Chapter 5.1.2**.

5.2.3 UTOPIA Port/Address Mapping (Backplane side)

The UTOPIA Port/Address mapping (Backplane side) is identical to the UTOPIA Port/ Address Mapping as described in **Chapter 5.1.3**.

5.2.4 Functional UTOPIA Timing (Backplane side)

The functional timing is compatible to ATMF UTOPIA Level 2 standard [4] and ATMF UTOPIA Level 1 standard [3] respectively.

Remark 1

The ABM-3G UTOPIA Interfaces in master mode always introduce at least 1 idle clock between transmission or reception of subsequent ATM cells.

Remark 2

The ABM-3G UTOPIA Interfaces in **Level 1 Slave Mode** do not support constant active enable signals $\overline{\text{UTXENBi}}$/$\overline{\text{URXENBi}}$ (i = {D(Downstream); U(Upstream)}).

The enable signals must be deasserted with each cell cycle.

5.2.5 UTOPIA Master Mode Polling Scheme (Backplane side)

The UTOPIA Polling scheme (Backplane side) is identical to the UTOPIA Polling scheme as described in **Chapter 5.1.5**.

5.2.6 UTOPIA Cell Format (Backplane side)

The UTOPIA Polling scheme (Backplane side) is identical to the UTOPIA Polling scheme as described in **Chapter 5.1.6**.

5.3 MPI: Microprocessor Interface

The ABM-3G Microprocessor Interface is a generic asynchronous 16-bit slave-only interface that supports Intel and Motorola style control signals. The interface is 'ready' signal controlled.

5.3.1 Intel Style Write Access

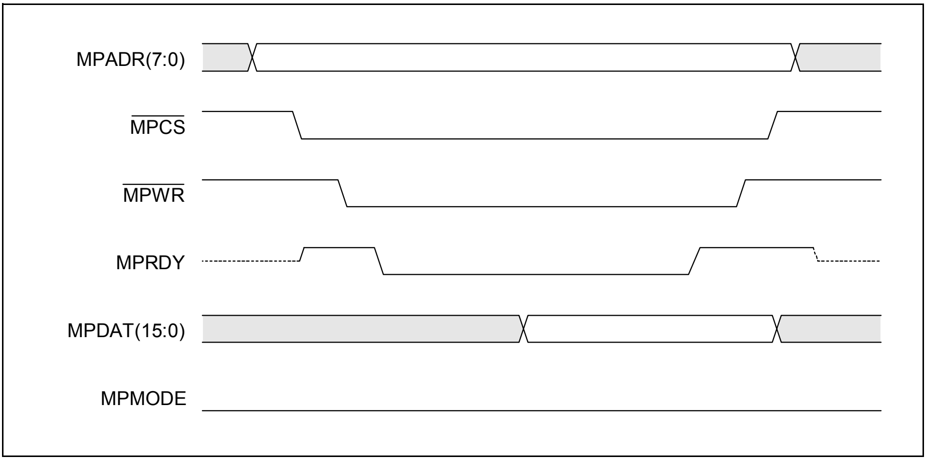


Figure 5-5 Intel Style Write Access

5.3.2 Intel Style Read Access

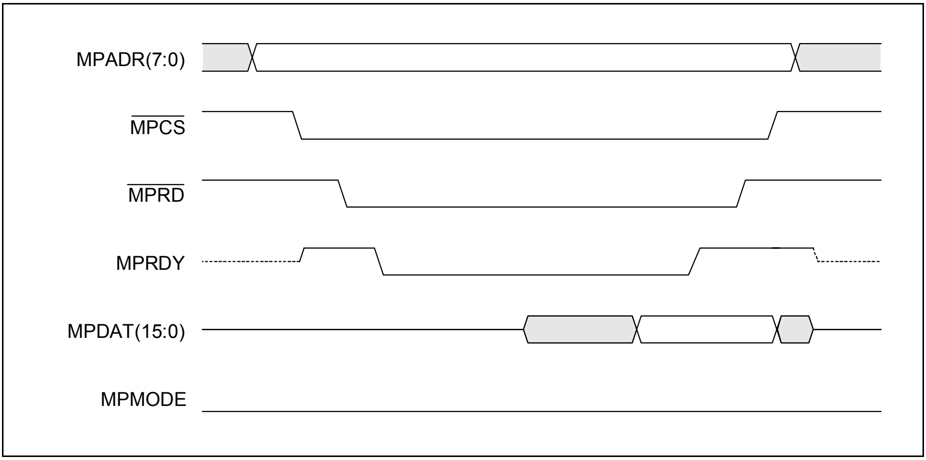


Figure 5-6 Intel Style Read Access

5.3.3 Motorola Style Write Access

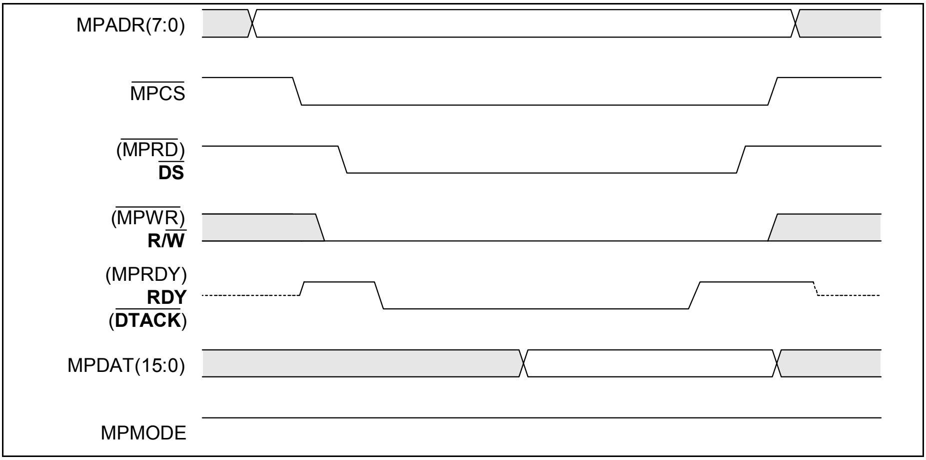


Figure 5-7 Motorola Style Write Access

5.3.4 Motorola Style Read Access

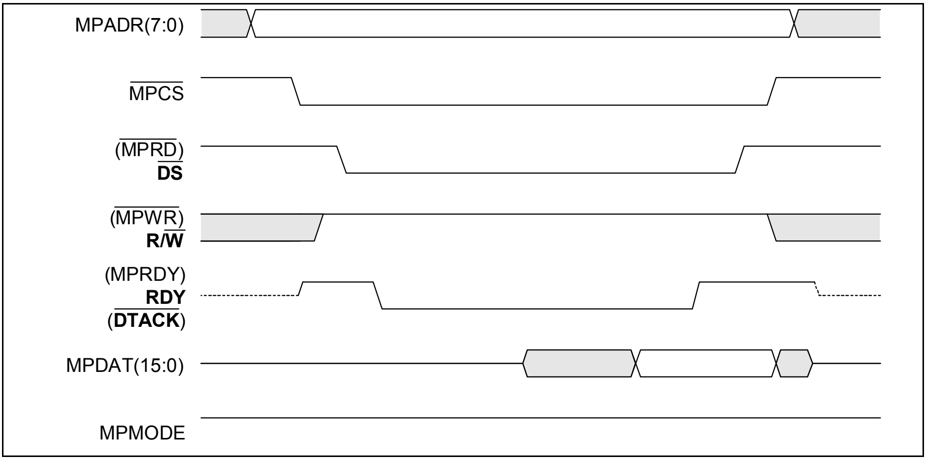


Figure 5-8 Motorola Style Read Access

5.3.5 Interrupt Signals

The ABM-3G asserts its interrupt signals MPINT and MPINTD if non-masked interrupt events are pending in the respective interrupt status registers. Interrupt signals are deasserted in case all events are cleared by writing '1' to pending interrupt bits (e.g. write $0xFFFF_H$ to the respective Interrupt Status Register). This allows edge sensitive interrupt implementations.

Interrupt signals are of type 'Open Drain' to allow wired-or implementations sharing one interrupt signal with other devices.

5.4 External RAM Interfaces

5.4.1 RAM Configurations

The ABM-3G device uses synchronous dynamic RAM (SDRAM) for the storage of ATM cells and synchronous static RAM (SSRAM) for the storage of cell pointers. Two SDRAM Interfaces and one SSRAM Interface are provided. Each of the two SDRAM Interfaces is associated with one of the ABM Cores. The SSRAM Interface is shared by both ABM-3G Cores. All RAM Interfaces are operated with the system clock provided by the ABM-3G:

Table 5-9 External RAM Sizes

Cell Pointer SSRAM	Min. Required Up-stream Cell SDRAM	Min. Required Down-stream Cell SDRAM	UBMTH	Up-stream Buffer	DBMTH	Down-stream Buffer
e.g. 512 k x 32 bit	128 Mb e.g. 2*(4Mb*16)	128 Mb e.g. 2*(4Mb*16)	$3FFFF_H$	256K cells	$3FFFF_H$	256K cells
e.g. 256 k x 32 bit	64 Mb e.g. 1*(2Mb*32)	64 Mb e.g. 1*(2Mb*32)	$1FFFF_H$	128K cells	$1FFFF_H$	128Kk cells
e.g. 128 k x 32 bit	32 Mb	32 Mb	$0FFFF_H$	64K cells	$0FFFF_H$	64K cells
e.g. 256 k x 32 bit	128 Mb e.g. 2*(4Mb*16)	none	$3FFFF_H$	256K cells	0000_H	0
e.g. 128 k x 32 bit	64 Mb e.g. 1*(2Mb*32)	none	$1FFFF_H$	128K cells	0000_H	0
e.g. 64 k x 32 bit	32 Mb	none	$0FFFF_H$	64K cells	0000_H	0

Note: The upstream cell storage RAM must always be connected.

The minimum required width of the cell pointer SSRAM is in the range 16..20 bits depending on the selected Cell Storage Size and additional feature configurations:

Table 5-10 SSRAM Configuration Examples

Cell Storage RAM cell capacity (each)	Enabled Features	Stored Address Pointer Width	Feature Bits	Min. SSRAM Width
256K	VBR.2/3 + EOP marking	18	2	20
	EOP marking	18	1	19
	none	18	0	18
128K	VBR.2/3 + EOP marking	17	2	19
	EOP marking	17	1	18
	none	17	0	17
64K	VBR.2/3 + EOP marking	16	2	18
	EOP marking	16	1	17
	none	16	0	16

Note: VBR.2/3 represents VBR shaping function 2 and 3 requiring one additional bit storage in the CPR for the CLP bit.
EOP marking represents one additional bit storage in the CPR for End-of-Packet indication required by EPD/PPD and VC-Merge operation.

Table 5-11 gives an example of supported SDRAM configuration:

Table 5-11 SDRAM Configuration Examples

Type	Configuration per Direction
512k * 32 (4 bank) (64Mb Type)	1 SDRAM: 8-bit column address 10-bit row address 2-bit bank select Note: This Configuration supports only 128k cells storage per direction.
1Mb * 16 (4 bank) (64Mb Types)	2 SDRAM: 8-bit column address 12-bit row address 2-bit bank select Note: This Configuration supports 256k cells storage per direction.
2Mb * 16 (4 bank) (128Mb Types)	2 SDRAM: 9-bit column address 12-bit row address 2-bit bank select Note: This Configuration supports 256k cells storage per direction. (50% memory remains unused)
4Mb * 16 (4 bank) (256Mb Types)	2 SDRAM: 9-bit column address 12-bit row address (13) 2-bit bank select Note: This Configuration supports 256k cells storage per direction. (75% memory remains unused; one of the 13 memory address bits remains unused)

Note: Both CSR Interfaces support 8-bit and 9-bit column address width SDRAM types (see register **"MODE2" on Page 315**).

Table 5-12 gives an example of supported SSRAM configurations:

Table 5-12 SSRAM and SDRAM Type Examples

Type		Configuration
SSRAM		
1	Micron MT58V512V32F (flow through)	512k * 32
SDRAM		
1	Infineon HYB39S64160BT	4 banks * 1M * 16
2	Infineon HYB39S256160BT	4 banks * 4M * 16

5.5 Test Interface

The boundary scan functionality is implemented according to IEEE 1149.1, using a 5-pin test access port.

5.6 Clock and Reset Interface

5.6.1 Clocking

The ABM-3G supports different clock domains and clock generation configurations. **"Clocking System" on Page 52** provides the details.

5.6.2 Reset

The Reset signal can be asserted anytime asynchronously to the system clock. After detecting an active reset, the ABM-3G starts internal initialization processes and resets all registers to their reset value. Chapter **"Reset System" on Page 54** provides the details.

Note: Internal and external RAM initialization must be initiated by software via register **"MODE1" on Page 312**.

6 Memory Structure

The ABM-3G is a slave device in relation to the microcontroller bus and provides a set of 256 16-bit wide registers. Internal tables are accessed via dedicated transfer registers (see **Figure 7-1**). Typically, the register structure is mapped into the memory address space of the local controller.

7 Register Description

This chapter provides both an overview of the ATM Buffer Manager ABM-3G Register Set and detailed register descriptions and Table Access descriptions.

7.1 Overview of the ABM-3G Register Set

Control and operation of the ABM-3G chip can be done by directly configuring Status Registers or, to a large extent, by programming the internal tables. Access to these tables is not direct, but occurs via Transfer Registers and Transfer Commands. Any transfer must be prepared by writing appropriate values to the Transfer Registers. Bit positions named 'don't Write' must be masked by writing **1** to the corresponding bit positions in the Mask Register. This avoids overwriting these table bit positions with the Transfer Register contents, which may cause fatal malfunction. The specific table position which should be modified with the Transfer Register contents is selected via Register WAR. Transfer is started by writing the table address to Register MAR and also setting the 'Start' bit. The ABM-3G device will reset the 'Start' bit after transfer completion.

The ABM-3G contains the following internal tables for configuration:

- LCI Table (LCI)
- Traffic Class Table (TCT)
- Queue Configuration Table (QCT)
- Queue Parameter Table 1 (QPT1)
- Queue Parameter Table 2 (QPT2)
- Scheduler Block Occupancy Table (SBOC)
- Scheduler Block Rate Tables (consisting of 4 tables):
  - SCTI Upstream
  - SCTI Downstream
  - SCTF Upstream
  - SCTF Downstream
- Merge Group Table (MGT)
- VBR Table (AVT)

Figure 7-1 gives an overview of all (user accessible) tables and related control/transfer/mask registers:

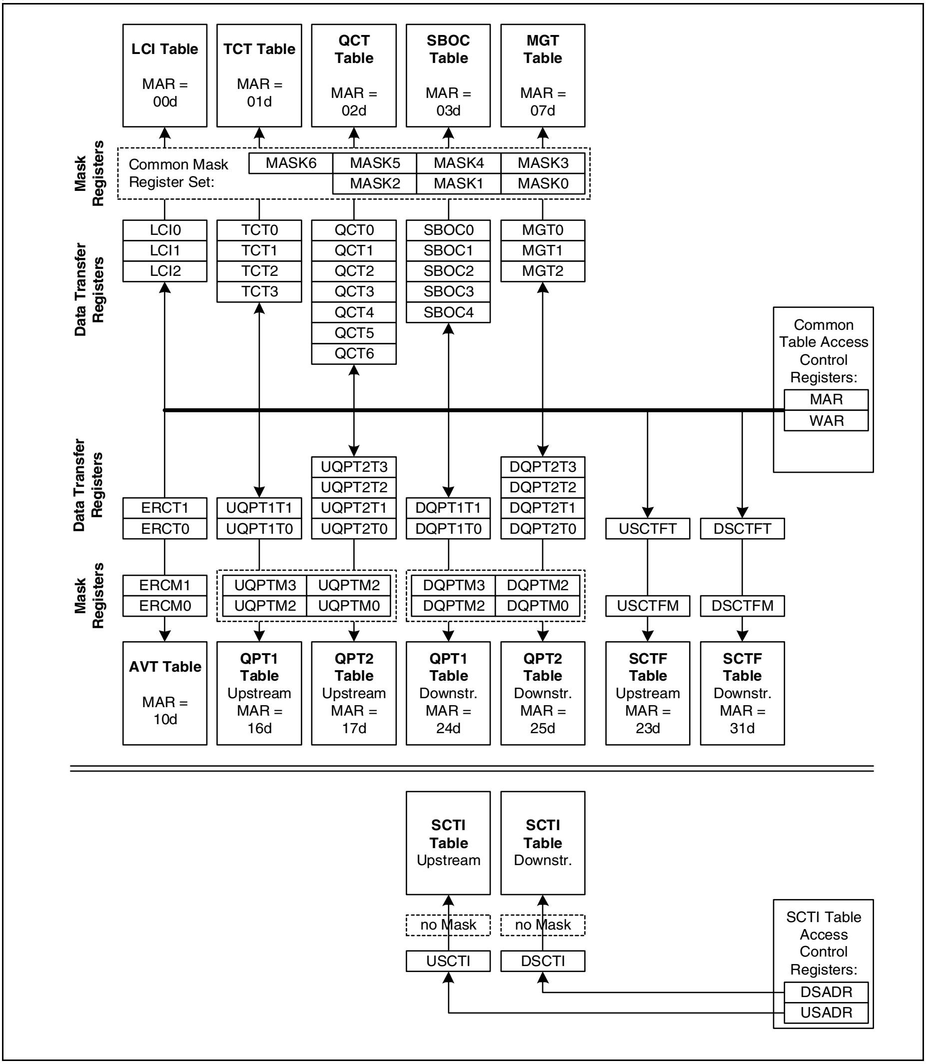


Figure 7-1 Table Access Overview

The Status Registers and Transfer Registers are described below in Table 7-2. Offset addresses are 16-bit word addresses. in order to prevent malfunctions and to guarantee upwards compatibility to future versions of the device, performing Write accesses to 'Reserved Register' addresses is not recommended.

Internal table entries contain bit fields for internal device operation only. Table 7-1 identifies the color conventions used for the various types of fields described in this register chapter:

Table 7-1 Color Convention for Internal Table Field Illustration

Color	Meaning
(grey)	Grey shaded fields are 'unused'. Reading these fields will return '0'.
(green)	Green shaded fields require attention by CPU. They can be written or read by CPU; usage depends on the respective field description. Typically green fields must be written for initialization and configuration or read for status query.
(blue)	Blue shaded fields require/allow **READ** attention by CPU. Typically blue fields provide counter or status information. The CPU **MUST NOT** write to blue fields.
(red)	Red shaded fields are for device internal use only and require **NO** attention by CPU. The CPU **MUST NOT** write to red fields.

Table 7-2 ABM-3G Registers Overview

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
Cell Flow Test Registers					
01/11	UCFTST/ DCFTST	Upstream/Downstream Cell Flow Test Registers	0000	R/W	156
SDRAM Configuration Registers					
02/12	URCFG/ DRCFG	Upstream/Downstream SDRAM Configuration Registers	0033	R/W	157
03/13	-	Reserved Register	0000	R	-
04/14	-	Reserved Register	0000	R	-
Cell Insertion/Extraction and AAL5 Control Registers					
05/15	UA5TXHD0/ DA5TXHD0	Upstream/Downstream AAL5 Transmit Header 0 Registers	0000	R/W	158
06/16	UA5TXHD1/ DA5TXHD1	Upstream/Downstream AAL5Transmit Header 1 Registers	0000	R/W	160
07/17	UA5TXDAT0/ DA5TXDAT0	Upstream/Downstream AAL5Transmit Data 0 Registers	0000	R/W	162

Table 7-2 ABM-3G Registers Overview (cont'd)

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
08/18	UA5TXDAT1/ DA5TXDAT1	Upstream/Downstream AAL5 Transmit Data 1 Registers	0000	R/W	163
09/19	UA5TXTR/ DA5TXTR	Upstream/Downstream AAL5 Transmit Trailer Registers	0000	R/W	164
0A/1A	UA5TXCMD/ DA5TXCMD	Upstream/Downstream AAL5 Transmit Command Registers	0000	R/W	165
0B/1B	UA5RXHD0/ DA5RXHD0	Upstream/Downstream AAL5 Receive Header 0 Registers	0000	R/W	166
0C/1C	UA5RXHD1/ DA5RXHD1	Upstream/Downstream AAL5 Receive Header 1 Registers	0000	R/W	168
0D/1D	UA5RXDAT0/ DA5RXDAT0	Upstream/Downstream AAL5 Receive Data 0 Registers	0000	R/W	170
0E/1E	UA5RXDAT1/ DA5RXDAT1	Upstream/Downstream AAL5 Receive Data 1 Registers	0000	R/W	171
0F/1F	UA5SARS/ DA5SARS	Upstream/Downstream AAL5 SAR Status Registers	0000	R/W	172
Buffer Occupation Counter Registers					
20	UBufferOcc	Upstream/Downstream Buffer Occupation Registers	0000	R	174
21	DBufferOcc		0000	R	174
22	UBufferOccNg	Up-/Downstream Non-Guaranteed Buffer Occupation Registers	0000	R	175
23	DBufferOccNg		0000	R	175
Buffer Threshold and Occupation Capture Registers					
24	UBufMax	Upstream/Downstream Buffer Maximum Threshold Registers	0000	R/W	176
25	DBufMax		0000	R/W	176
26	UMAC	Upstream/Downstream Maximum Occupation Capture Registers	0000	R	178
27	DMAC		0000	R	178
28	UMIC	Upstream/Downstream Minimum Occupation Capture Registers	FFFF	R	179
29	DMIC		FFFF	R	179
2A	CLP1DIS	CLP1 Discard Global Threshold Registers	0000	R/W	180

Table 7-2 ABM-3G Registers Overview (cont'd)

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
Configuration Register					
2B	CONFIG	Configuration Register	0000	R/W	181
Backpressure Control Registers					
2C	UUBPTH0	Upstream UTOPIA Backpressure Threshold Register 0	FFFF	R/W	181
2D	UUBPTH1	Upstream UTOPIA Backpressure Threshold Register 1	FFFF	R/W	183
2E	UUBPTH2	Upstream UTOPIA Backpressure Threshold Register 2	FFFF	R/W	184
2F	UUBPTH3	Upstream UTOPIA Backpressure Threshold Register 3	FFFF	R/W	185
30	UBPEI	UTOPIA Backpressure Exceed Indication Register	0000	R/W	186
31	DUBPTH0	Downstream UTOPIA Backpressure Threshold Register 0	FFFF	R/W	187
32	DUBPTH1	Downstream UTOPIA Backpressure Threshold Register 1	FFFF	R/W	188
33	DUBPTH2	Downstream UTOPIA Backpressure Threshold Register 2	FFFF	R/W	189
34	DUBPTH3	Downstream UTOPIA Backpressure Threshold Register 3	FFFF	R/W	190
35	-	Reserved Register	0080	R/W	-
36	-	Reserved Register	0000	R/W	-
37	-	Reserved Register	0000	R/W	-
38	-	Reserved Register	0000	R/W	-
39	-	Reserved Register	0000	R/W	-
3A	-	Reserved Register	0000	R	-
LCI Table Transfer Registers					
3B	LCI0	LCI Transfer Register 0	0000	R/W	192
3C	LCI1	LCI Transfer Register 1	0000	R/W	193
3D	LCI2	LCI Transfer Register 2	0000	R/W	194

Table 7-2 ABM-3G Registers Overview (cont'd)

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
Traffic Class Table Transfer Registers					
3E	TCT0	TCT Transfer Register 0	0000	R/W	198
3F	TCT1	TCT Transfer Register 1	0000	R/W	201
40	TCT2	TCT Transfer Register 2	0000	R/W	204
41	TCT3	TCT Transfer Register 3	0000	R/W	207
Queue Configuration Table Transfer Registers					
42	QCT0	Queue Configuration Transfer Register 0	0000	R/W	213
43	QCT1	Queue Configuration Transfer Register 1	0000	R/W	214
44	QCT2	Queue Configuration Transfer Register 2	0000	R/W	217
45	QCT3	Queue Configuration Transfer Register 3	0000	R/W	219
46	QCT4	Queue Configuration Transfer Register 4	0000	R/W	220
47	QCT5	Queue Configuration Transfer Register 5	0000	R/W	221
48	QCT6	Queue Configuration Transfer Register 6	0000	R/W	222
Scheduler Block Occupancy Table Transfer Registers					
49	SBOC0	SBOC Transfer Register 0	0000	R/W	225
4A	SBOC1	SBOC Transfer Register 1	0000	R/W	226
4B	SBOC2	SBOC Transfer Register 2	0000	R/W	227
4C	SBOC3	SBOC Transfer Register 3	0000	R/W	228
4D	SBOC4	SBOC Transfer Register 4	0000	R/W	229
Merge Group Table Transfer Registers					
4E	MGT0	MGT Transfer Register 0	0000	R/W	232
4F	MGT1	MGT Transfer Register 1	0000	R/W	233
50	MGT2	MGT Transfer Register 2	0000	R/W	234
51	-	Reserved Register	0000	R/W	-
52	-	Reserved Register	0000	R/W	-
53	-	Reserved Register	0000	R/W	-
54	-	Reserved Register	0000	R/W	-
Mask Registers					

Table 7-2 ABM-3G Registers Overview (cont'd)

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
for Read/Write transfer access control of LCI-, Traffic Class-, Queue Configuration-, Scheduler Block Occupancy and Merge Group Tables					
55/56	MASK0/ MASK1	Table Access Mask Registers 0/1	0000	R/W	235
57/58	MASK2/ MASK3	Table Access Mask Registers 2/3	0000	R/W	236
59/5A	MASK4/ MASK5	Table Access Mask Registers 4/5	0000	R/W	237
5B	MASK6	Table Access Mask Registers 6	0000	R/W	238
5C	-	Reserved Register	0000	R/W	-
5D	-	Reserved Register	0000	R/W	-
5E	-	Reserved Register	0000	R/W	-
5F	-	Reserved Register	0000	R/W	-
Rate Shaper CDV Registers					
60/80	-	Reserved Register	0000	R	-
61/81	-	Reserved Register	0000	R	-
62/82	UCDV/ DCDV	Upstream/Downstream Rate Shaper CDV Registers	0000	R/W	239
63/83	-	Reserved Register	0000	R	-
64/84	-	Reserved Register	0000	R	-
Queue Parameter Table Mask Registers					
65/85	UQPTM0/ DQPTM0	Upstream/Downstream Queue Parameter Table Mask Registers 0	0000	R/W	240
66/86	UQPTM1/ DQPTM1	Upstream/Downstream Queue Parameter Table Mask Registers 1	0000	R/W	241
67/87	UQPTM2/ DQPTM2	Upstream/Downstream Queue Parameter Table Mask Registers 2	0000	R/W	242

Table 7-2 ABM-3G Registers Overview (cont'd)

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
68/88	UQPTM3/ DQPTM3	Upstream/Downstream Queue Parameter Table Mask Registers 3	0000	R/W	243
69/89	UQPTM4/ DQPTM4	Upstream/Downstream Queue Parameter Table Mask Registers 4	0000	R/W	244
6A/8A	UQPTM5/ DQPTM5	Upstream/Downstream Queue Parameter Table Mask Registers 5	0000	R/W	245
Scheduler Configuration Register					
6B/8B	USCONF/ DSCONF	Upstream/Downstream Scheduler Configuration Registers	0000	R/W	246
6C/8C	-	Reserved Register	0000	R	-
6D/8D	-	Reserved Register	0000	R	-
6E/8E	-	Reserved Register	0000	R	-
6F/8F	-	Reserved Register	0000	R	-
Queue Parameter Table Transfer Registers					
70/90	UQPT1T0/ DQPT1T0	Upstream/Downstream QPT1 Table Transfer Register 0	0000	R/W	249
71/91	UQPT1T1/ DQPT1T1	Upstream/Downstream QPT1 Table Transfer Register 1	0000	R/W	250
72/92	UQPT2T0/ DQPT2T0	Upstream/Downstream QPT2 Table Transfer Register 0	0000	R/W	253
73/93	UQPT2T1/ DQPT2T1	Upstream/Downstream QPT2 Table Transfer Register 1	0000	R/W	254
74/94	UQPT2T2/ DQPT2T2	Upstream/Downstream QPT2 Table Transfer Register 2	0000	R/W	255
75/95	UQPT2T3/ DQPT2T3	Upstream/Downstream QPT2 Table Transfer Register 3	0000	R/W	256
76/96	-	Reserved Register	0000	R/W	-
77/97	-	Reserved Register	0000	R/W	-
78/98	-	Reserved Register	0000	R/W	-
79/99	-	Reserved Register	0000	R/W	-
7A/9A	-	Reserved Register	0000	R/W	-

Table 7-2 ABM-3G Registers Overview (cont'd)

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
7B/9B	-	Reserved Register	0000	R/W	-
7C/9C	-	Reserved Register	0000	R/W	-
7D/9D	-	Reserved Register	0000	R/W	-
7E/9E	-	Reserved Register	0000	R/W	-
7F/9F	-	Reserved Register	0000	R/W	-
Scheduler Block Configuration Table Transfer/Mask Registers SDRAM Refresh Registers UTOPIA Port Select of Common Real Time Queue Registers					
A0/B8	USADR/ DSADR	Upstream/Downstream SCTI Address Registers	0000	R/W	259
A1/B9	USCTI/ DSCTI	Upstream/Downstream SCTI Transfer Registers	0000	R/W	260
A2/BA	UECRI/ DECRI	Upstream/Downstream Empty Cycle Rate Integer Part Registers	0000	R/W	263
A3/BB	UECRF/ DECRF	Upstream/Downstream Empty Cycle Rate Fractional Part Registers	0000	R/W	264
A4/BC	UCRTQ/ DCRTQ	Upstream/Downstream Common Real Time Queue UTOPIA Port Select Registers	0000	R/W	265
A5/BD	USCTFM/ DSCTFM	Upstream/Downstream SCTF Mask Registers	0000	R/W	266
A6/BE	USCTFT/ DSCTFT	Upstream/Downstream SCTF Transfer Registers	0000	R/W	269
A7/BF	-	Reserved Register	0000	R	-
Scheduler Block Enable Registers					
A8/C0	USCEN0/ DSCEN0	Upstream/Downstream Scheduler Block Enable 0 Registers	0000	R/W	270
A9/C1	USCEN1/ DSCEN1	Upstream/Downstream Scheduler Block Enable 1 Registers	0000	R/W	271
AA/C2	USCEN2/ DSCEN2	Upstream/Downstream Scheduler Block Enable 2 Registers	0000	R/W	272
AB/C3	USCEN3/ DSCEN3	Upstream/Downstream Scheduler Block Enable 3 Registers	0000	R/W	273

Table 7-2 ABM-3G Registers Overview (cont'd)

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
AC/C4	USCEN4/ DSCEN4	Upstream/Downstream Scheduler Block Enable 4 Registers	0000	R/W	274
AD/C5	USCEN5/ DSCEN5	Upstream/Downstream Scheduler Block Enable 5 Registers	0000	R/W	275
AE/C6	USCEN6/ DSCEN6	Upstream/Downstream Scheduler Block Enable 6 Registers	0000	R/W	276
AF/C7	USCEN7/ DSCEN7	Upstream/Downstream Scheduler Block Enable 7 Registers	0000	R/W	277
Common Real Time Queue Rate Registers					
B0/C8	UCRTRI/ DCRTRI	Upstream/Downstream CRT Rate Integer Registers	0000	R/W	278
B1/C9	UCRTRF/ DCRTRF	Upstream/Downstream CRT Rate Fractional Registers	0000	R/W	279
B2	-	Reserved Register	0000	R	-
B3	-	Reserved Register	0000	R	-
B4	-	Reserved Register	0000	R	-
B5	-	Reserved Register	0000	R	-
B6	-	Reserved Register	0000	R	-
B7	-	Reserved Register	0000	R	-
AVT Table Registers					
CA	ERCT0	AVT Table Transfer Register 0	0000	R/W	282
CB	ERCT1	AVT Table Transfer Register 1	0000	R/W	283
CC	ERCM0	AVT Table Access Mask Register 0	0000	R/W	284
CD	ERCM1	AVT Table Access Mask Register 1	0000	R/W	285
CE	-	Reserved Register	0000	R	-
CF	-	Reserved Register	0000	R	-
D0	-	Reserved Register	0000	R	-
D1	-	Reserved Register	0000	R	-
D2	-	Reserved Register	0000	R	-
D3	-	Reserved Register	0000	R	-

Table 7-2 ABM-3G Registers Overview (cont'd)

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
D4	-	Reserved Register	0000	R	-
D5	ERCCONF0	ERC Configuration Register 0	0000	R/W	286
D6	-	Reserved Register	0000	R	-
PLL Control Registers					
D7	PLL1CONF	PLL1 Configuration Register	0000	R/W	287
D8	-	Reserved Register	0000	R	-
D9	PLLTST	PLL Test Register	0000	R/W	289
External RAM Test Registers					
DC	EXTRAMD0	External RAM Test Data Register 0	0000	R/W	290
DD	EXTRAMD1	External RAM Test Data Register 1	0000	R/W	291
DE	EXTRAMA0	External RAM Test Address Register Low	0000	R/W	292
DF	EXTRAMA1	External RAM Test Address Register High	0000	R/W	293
E0	EXTRAMC	External RAM Test Command Register	0000	R/W	294
ABM-3G Version Code Registers					
E1	VERL	Version Number Low Register	F083	R	295
E2	VERH	Version Number High Register	1007	R	296
Interrupt Status/Mask Registers					
E3	ISRU	Interrupt Status Register Upstream	0000	R/W	297
E4	ISRD	Interrupt Status Register Downstream	0000	R/W	300
E5	ISRC	Interrupt Status Register Common	0000	R/W	303
E6	IMRU	Interrupt Mask Register Upstream	0000	R/W	304
E7	IMRD	Interrupt Mask Register Downstream	0000	R/W	305
E8	IMRC	Interrupt Mask Register Common	0000	R/W	306
E9	-	Reserved Register	0000	R	-
EA	-	Reserved Register	0000	R	-

Table 7-2 ABM-3G Registers Overview (cont'd)

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
RAM Select Registers					
EB	MAR	Memory Address Register	0000	R/W	307
EC	WAR	Word Address Register	0000	R/W	309
Global ABM-3G Status and Mode Registers					
ED	USTATUS	ABM-3G UTOPIA Status Register	0000	R/W	311
EE	MODE1	ABM-3G Mode 1 Register	0000	R/W	312
EF	MODE2	ABM-3G Mode 2 Register	0000	R/W	315
UTOPIA Configuration Registers					
F0	UTRXCFG	Upstream/Downstream UTOPIA Receive Configuration Register	0001	R/W	317
F1	UUTRXP0	Upstream UTOPIA Receive Port Register 0	0000	R/W	319
F2	UUTRXP1	Upstream UTOPIA Receive Port Register 1	0000	R/W	320
F3	UUTRXP2	Upstream UTOPIA Receive Port Register 2	0000	R/W	321
F4	DUTRXP0	Downstream UTOPIA Receive Port Register 0	0000	R/W	322
F5	DUTRXP1	Downstream UTOPIA Receive Port Register 1	0000	R/W	323
F6	DUTRXP2	Downstream UTOPIA Receive Port Register 2	0000	R/W	324
F7	UUTTXCFG	Upstream UTOPIA Transmit Configuration Register	0000	R/W	325
F8	DUTTXCFG	Downstream UTOPIA Transmit Configuration Register	0001	R/W	327
F9	UUTTXP0	Upstream UTOPIA Transmit Port Register 0	0000	R/W	329
FA	UUTTXP1	Upstream UTOPIA Transmit Port Register 1	0000	R/W	330

Table 7-2 ABM-3G Registers Overview (cont'd)

Addr (hex)	Register	Description	Reset value (hex)	µP	See page
FB	UUTTXP2	Upstream UTOPIA Transmit Port Register 2	0000	R/W	331
FC	DUTTXP0	Downstream UTOPIA Transmit Port Register 0	0000	R/W	332
FD	DUTTXD1	Downstream UTOPIA Transmit Port Register 1	0000	R/W	333
FE	DUTTXD2	Downstream UTOPIA Transmit Port Register 2	0000	R/W	334
Test Registers/Special Mode Registers					
FF	TEST	TEST Register	0000	R/W	335

7.2 Detailed Register Descriptions

7.2.1 Cell Flow Test Registers

Register 1 UCFTST/DCFTST
Upstream/Downstream Cell Flow Test Registers

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **UCFTST** **01_H** **DCFTST** **11_H**
Typical Usage: Written by CPU to test internal integrity functions during special system test scenarios

Bit	15	14	13	12	11	10	9	8
	Unused(15:8)							

Bit	7	6	5	4	3	2	1	0
	Unused(7:2)						TSTBIP	TSTQID

TSTBIP **Test BIP-8 Supervision**

0 **Normal Operation**:
BIP-8 for cell protection is generated normally. No ’BIP8ER’ interrupt should occur indicating a cell storage failure.

1 **Test Mode**:
Least Significant Bit (LSB) of BIP-8 is inverted to test BIP-8 checking function. A ’BIP8ER’ (**Register 101: ISRU**, **Register 102: ISRD**) interrupt is generated whenever a cell is Read out of the Cell Buffer RAM.

TSTQID **Test Queue ID Supervision**
(see **“Cell Queue Supervision” on Page 90**)

0 **Normal Operation**:
A correct QID is generated. No ’BUFER4’ interrupt should occur indicating an internal queue pointer failure.

1	**Test Mode**: The LSB of the QID is inverted to test the QID checking function. A 'BUFER4' (**Register 101: ISRU**, **Register 102: ISRD**) interrupt is generated whenever a cell is Read out from the Cell Buffer RAM.

Note: The respective QID value is stored with each cell when written to the appropriate queue in the cell storage RAM. The ABM-3G checks the stored QID value against the supposed QID when a cell is read back from the cell storage RAM.

7.2.2 SDRAM Configuration Registers

Register 2 URCFG/DRCFG
Upstream/Downstream SDRAM Configuration Registers

CPU Accessibility: **Read/Write**
Reset Value: **0033_H**
Offset Address: **URCFG** **02_H** **DRCFG** **12_H**
Typical Usage: (Reserved)

Bit	15	14	13	12	11	10	9	8
	Reserved(15:8)							

Bit	7	6	5	4	3	2	1	0
	Reserved(7:0)							

Note: These registers are for internal use only. Do not to Write a value different from the Reset Value 0033_H to Registers URCFG/DRCFG.

7.2.3 Cell Insertion/Extraction and AAL5 Control Registers

Register 3 UA5TXHD0/DA5TXHD0
Upstream/Downstream AAL5 Transmit Header 0 Registers

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **UA5TXHD0 05_H** **DA5TXHD0 15_H**
Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	LCI(11:4), VPI(11:4) or GFC(3:0) | VPI(7:4), LCI(11:4), VPI(11:4) or GFC(3:0) | VPI(7:4),							

Bit	7	6	5	4	3	2	1	0
	LCI(3:0), VPI(3:0), LCI(3:0), VPI(3:0)				VCI(15:12), LCI(15:12), VCI(15:12), VCI(15:12)			

First 16-bit word of an ATM cell.
The ABM-3G does not interpret these bit fields, but copies them into ATM cells that are inserted during AAL5 packet segmentation process. Inserted cells are forwarded to the ABM-3G like any cell received by the respective UTOPIA Interface. Thus the bit field usage must comply to the selected LCI mapping mode in the particular application.

VPI(11:0) or GFC(3:0) | VPI(7:0) or LCI(11:0)

The meaning of this bit field depends on the selected LCI mapping mode in **Register 110: MODE1**:
MODE1->LCIMOD(1:0):

’00’ VPI Address translated mode: LCI(11:0)

’01’ VPI transparent mode:
- NNI cell format: 12-bit VPI field
- UNI cell format: 4-bit GFC field and 8-bit VPI field

’10’ VPI Address translated mode: LCI(11:0)

’11’ VPI transparent mode:
- NNI cell format: 12-bit VPI field
- UNI cell format: 4-bit GFC field and 8 bit VPI field

Note: If LCI mapping mode ’10’ is chosen LCI(13:12) cannot be specified, i.e. AAL5 cell insertion is limited to the LCI range 0..4095.

VCI(15:12) or LCI(15:12) or VCI(15:12)

The meaning of this bit field depends on the selected LCI mapping mode in **Register 110: MODE1**:
MODE1->LCIMOD(1:0):

’00’	VCI transparent mode: VCI(15:12)
’01’	VCI Address translated mode: LCI(15:12)
’10’	VCI transparent mode: VCI(15:12)
’11’	VCI transparent mode: VCI(15:12)

Register 4 UA5TXHD1/DA5TXHD1
Upstream/Downstream AAL5Transmit Header 1 Registers

CPU Accessibility:	**Read/Write**		
Reset Value:	**0000_H**		
Offset Address:	**UA5TXHD1 06_H**	**DA5TXHD1 16_H**	
Typical Usage:	Written by CPU		

Bit	15	14	13	12	11	10	9	8
	VCI(11:4), LCI(11:4), VCI(11:4), VCI(11:4)							

Bit	7	6	5	4	3	2	1	0
	VCI(3:0), LCI(3:0), VCI(3:0), VCI(3:0)				PT(2:0)			CLP

Second 16-bit word of an ATM cell.
The ABM-3G does not interpret these bit fields, but copies them into ATM cells that are inserted during AAL5 packet segmentation process. Inserted cells are forwarded to the ABM-3G like any cell received by the respective UTOPIA Interface. Thus the bit field usage must comply to the selected LCI mapping mode in the particular application.

VCI(11:0) or LCI(11:0) The meaning of this bit field depends on the selected LCI mapping mode in **Register 110: MODE1**:
MODE1->LCIMOD(1:0):

'00'	VCI transparent mode: VCI(11:0)
'01'	VCI Address translated mode: LCI(11:0)
'10'	VCI transparent mode: VCI(11:0)
'11'	VCI transparent mode: VCI(11:0)

PT(2:0) **Payload Type Field in ATM cell Header**

PT(0) is automatically handled by the ABM-3G (End of Packet indication set to '1' in last cell of any AAL5 segmented packet).
PT(1) ('Congestion Experienced') may be overwritten by CPU anytime during segmentation process and will be inserted in the following AAL5 cell generated.
This field must be initialized to all 0s.

CLP **Cell Loss Priority Bit in ATM cell Header**

The CLP bit is copied transparently and may be overwritten (changed) by CPU anytime during segmentation process (new value will be inserted in the following AAL5 cell generated).

Register 5 **UA5TXDAT0/DA5TXDAT0**
Upstream/Downstream AAL5Transmit Data 0 Registers

CPU Accessibility:	**Read/Write**		
Reset Value:	**0000_H**		
Offset Address:	**UA5TXDAT0**	**07_H**	**DA5TXDAT0** **17_H**
Typical Usage:	Written by CPU		

Bit	15	14	13	12	11	10	9	8
	Octet(4n)(7:0)							

Bit	7	6	5	4	3	2	1	0
	Octet(4n+1)(7:0)							

Cell Transmit Data Transfer Register

Octet(4n)(7:0) **Payload data Octet (4n)**

Octet(4n+1)(7:0) **Payload data Octet (4n+1)**

The payload data octets of a cell to be inserted in either upstream or downstream direction are written by consecutive write accesses to registers **UTXDAT0/DTXDAT0** and **UTXDAT1/DTXDAT1** in alternating manner until end of packet:
cycle n=0: Octet 0 and 1: write to **UTXDAT0/DTXDAT0**
cycle n=0: Octet 2 and 3: write to **UTXDAT1/DTXDAT1**
cycle n=1: Octet 4 and 5: write to **UTXDAT0/DTXDAT0**
cycle n=1: Octet 6 and 7: write to **UTXDAT1/DTXDAT1**
...

Register 6 UA5TXDAT1/DA5TXDAT1
Upstream/Downstream AAL5 Transmit Data 1 Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **UA5TXDAT1 08_H** **DA5TXDAT1 18_H**

Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	Octet(4n+2)(7:0)							

Bit	7	6	5	4	3	2	1	0
	Octet(4n+3)(7:0)							

Cell Transmit Data Transfer Register

Octet(4n+2)(7:0) **Payload data Octet (4n+2)**

Octet(4n+3)(7:0) **Payload data Octet (4n+3)**

The payload data octets of a cell to be inserted in either upstream or downstream direction are written by consecutive write accesses to registers **UTXDAT0/DTXDAT0** and **UTXDAT1/DTXDAT1** in alternating manner until end of packet:
cycle n=0: Octet 0 and 1: write to **UTXDAT0/DTXDAT0**
cycle n=0: Octet 2 and 3: write to **UTXDAT1/DTXDAT1**
cycle n=1: Octet 4 and 5: write to **UTXDAT0/DTXDAT0**
cycle n=1: Octet 6 and 7: write to **UTXDAT1/DTXDAT1**
...

Register 7 UA5TXTR/DA5TXTR
Upstream/Downstream AAL5 Transmit Trailer Registers

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**UA5TXTR**	**09_H**	**DA5TXTR**	**19_H**
Typical Usage:	Written by CPU			

Bit	15	14	13	12	11	10	9	8
	CPCSUU(7:0)							

Bit	7	6	5	4	3	2	1	0
	CPI(7:0)							

CPCS-UU(7:0) **Common Part Convergence Sublayer User to User Indication**

The CPCS-UU bit field is copied transparently into the CPCS-PDU trailer in the last cell of an AAL5 segmented packet.

CPI(7:0) **Common Part Indication**

The CPI bit field is copied transparently into the CPCS-PDU trailer in the last cell of an AAL5 segmented packet.

Register 8 UA5TXCMD/DA5TXCMD
Upstream/Downstream AAL5 Transmit Command Registers

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**UA5TXCMD**	**$0A_H$**	**DA5TXCMD**	**$1A_H$**
Typical Usage:	Written by CPU (write only, read always returns 0000)			

Bit	15	14	13	12	11	10	9	8
	AAL5EN	PLENGTH(14:8)						

Bit	7	6	5	4	3	2	1	0
	PLENGTH(7:0)							

AAL5EN **AAL5 Segmentation Enable**

This bit enables AAL5 segmentation process accompanied by the payload length octet counter PLENGTH:

’0’ AAL5 segmentation is disabled. Payload data octets written to the cell transmit data registers are ignored.

Note: Setting AAL5EN=’0’ during an active packet segmentation process leads to an abort of the packet, i.e. the current cell is inserted with PT(0)=’1’ (End of Packet indication) and CPCS-SDU Length field of the trailer set to 0.
To abort it is recommended to write all 0 to the register: AAL5EN | PLENGTH(14:0) = 0000_H

’1’ AAL5 segmentation is enabled. Payload data octets written to the cell transmit data registers are processed and the CPCS-PDU trailer is automatically appended in the last cell controlled by the payload length octet counter.

PLENGTH(14:0) **Payload Length Octet Counter**

This bit field represents the number of PDU payload octets for the current packet and is equal to the CPCS-SDU length field which is automatically inserted in the PDU trailer (last cell of the packet). The ABM-3G uses this counter value to control the AAL5 segmentation process.

Note: The maximum supported CPCS-SDU length is 32767 octets.

Register 9 UA5RXHD0/DA5RXHD0
Upstream/Downstream AAL5 Receive Header 0 Registers

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**UA5RXHD0 $0B_H$** **DA5RXHD0 $1B_H$**
Typical Usage:	Read by CPU

Bit	15	14	13	12	11	10	9	8
	LCI(11:4), VPI(11:4) or GFC(3:0) | VPI(7:4), LCI(11:4), VPI(11:4) or GFC(3:0) | VPI(7:4),							

Bit	7	6	5	4	3	2	1	0
	LCI(3:0), VPI(3:0), LCI(3:0), VPI(3:0)				VCI(15:12), LCI(15:12), VCI(15:12), VCI(15:12)			

Header octets one and two of first ATM cell of packet.
The ABM-3G SAR unit does not interpret these bit fields, but copies them from ATM cells that are extracted during AAL5 packet reassembly process. Extracted cells are forwarded from the ABM-3G like any cell to be transmitted by the respective UTOPIA Interface. Thus, the bit field usage depends on the selected LCI mapping mode in the particular application. From scheduler point of view the reassembly unit is addressed as UTOPIA port number 30_H.

VPI(11:0) **or** **GFC(3:0) |** **VPI(7:0)** **or** **LCI(11:0)**	The meaning of this bit field depends on the selected LCI mapping mode in **Register 110: MODE1**: MODE1->LCIMOD(1:0): '00' VPI Address translated mode: LCI(11:0) '01' VPI transparent mode: • NNI cell format: 12 bit VPI field • UNI cell format: 4 bit GFC field and 8 bit VPI field '10' VPI Address translated mode: LCI(11:0) '11' VPI transparent mode: • NNI cell format: 12 bit VPI field • UNI cell format: 4 bit GFC field and 8 bit VPI field *Note: If LCI mapping mode '10' is chosen LCI(13:12) are not given to the user.*
VCI(15:12) **or** **LCI(15:12)** **or** **VCI(15:12)**	The meaning of this bit field depends on the selected LCI mapping mode in **Register 110: MODE1**: MODE1->LCIMOD(1:0): '00' VCI transparent mode: VCI(15:12) '01' VCI Address translated mode: LCI(15:12) '10' VCI transparent mode: VCI(15:12) '11' VCI transparent mode: VCI(15:12)

Register 10 UA5RXHD1/DA5RXHD1
Upstream/Downstream AAL5 Receive Header 1 Registers

CPU Accessibility:	**Read/Write**		
Reset Value:	**0000_H**		
Offset Address:	**UA5RXHD1 $0C_H$**	**DA5RXHD1 $1C_H$**	
Typical Usage:	Read by CPU		

Bit	15	14	13	12	11	10	9	8
	VCI(11:4), LCI(11:4), VCI(11:4), VCI(11:4)							

Bit	7	6	5	4	3	2	1	0
	VCI(3:0), LCI(3:0), VCI(3:0), VCI(3:0)				PT(2:0)			CLP

Header octets three and four of first ATM cell of AAL5 packet.
The ABM-3G SAR unit does not interpret these bit fields, but copies them from ATM cells that are extracted during AAL5 packet reassembly process. Extracted cells are forwarded from the ABM-3G like any cell to be transmitted by the respective UTOPIA Interface. Thus, the bit field usage depends on the selected LCI mapping mode in the particular application. From scheduler point of view the reassembly unit is addressed as UTOPIA port number 30_H.

VCI(11:0) or LCI(11:0) The meaning of this bit field depends on the selected LCI mapping mode in **Register 110: MODE1**:
MODE1->LCIMOD(1:0):

'00'	VCI transparent mode: VCI(11:0)
'01'	VCI Address translated mode: LCI(11:0)
'10'	VCI transparent mode: VCI(11:0)
'11'	VCI transparent mode: VCI(11:0)

PT(2:0) **Payload Type Field in ATM cell Header**

PT(0) is automatically handled by the ABM-3G (End of Packet detection).

Note: OAM or RM cells detected with PT(2)='1' are discarded by the reassembly unit and ignored for the packet reassembly process. Thus packet reassembly is not disturbed by inserted OAM cells.

CLP **Cell Loss Priority Bit in ATM cell Header**

The CLP bit is copied transparently from the ATM cell.

Register 11 UA5RXDAT0/DA5RXDAT0
Upstream/Downstream AAL5 Receive Data 0 Registers

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **UA5RXDAT0 $0D_H$** **DA5RXDAT0 $1D_H$**
Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	Octet(4n)(7:0)							

Bit	7	6	5	4	3	2	1	0
	Octet(4n+1)(7:0)							

Cell Receive Data Transfer Register

Octet(4n)(7:0) **Payload data Octet (4n)**

Octet(4n+1)(7:0) **Payload data Octet (4n+1)**

The payload data octets of a cell extracted from either upstream or downstream direction are read by consecutive read accesses to registers **URXDAT0/DRXDAT0** and **URXDAT1/DRXDAT1** in alternating manner until end of packet:
cycle n=0: Octet 0 and 1: read from **URXDAT0/DRXDAT0**
cycle n=0: Octet 2 and 3: read from **URXDAT1/DRXDAT1**
cycle n=1: Octet 4 and 5: read from **URXDAT0/DRXDAT0**
cycle n=1: Octet 6 and 7: read from **URXDAT1/DRXDAT1**
...
After EOP is found, CPCS-UU, CPI and Status is read.

Register 12 UA5RXDAT1/DA5RXDAT1
Upstream/Downstream AAL5 Receive Data 1 Registers

CPU Accessibility:	**Read/Write**	
Reset Value:	**0000_H**	
Offset Address:	**UA5RXDAT1 $0E_H$**	**DA5RXDAT1 $1E_H$**
Typical Usage:	Read by CPU	

Bit	15	14	13	12	11	10	9	8
	Octet(4n+2)(7:0)							

Bit	7	6	5	4	3	2	1	0
	Octet(4n+3)(7:0)							

Cell Receive Data Transfer Register

Octet(4n)(7:0) **Payload data Octet (4n)**

Octet(4n+1)(7:0) **Payload data Octet (4n+1)**

The payload data octets of a cell extracted from either upstream or downstream direction are read by consecutive read accesses to registers **URXDAT0/DRXDAT0** and **URXDAT1/DRXDAT1** in alternating manner until end of packet:
cycle n=0: Octet 0 and 1: read from **URXDAT0/DRXDAT0**
cycle n=0: Octet 2 and 3: read from **URXDAT1/DRXDAT1**
cycle n=1: Octet 4 and 5: read from **URXDAT0/DRXDAT0**
cycle n=1: Octet 6 and 7: read from **URXDAT1/DRXDAT1**
...
After EOP is found, CPCS-UU, CPI and Status is read.

Register 13 UA5SARS/DA5SARS
Upstream/Downstream AAL5 SAR Status Registers

CPU Accessibility: **Read/Write**

Reset Value: **0080_H**

Offset Address: **UA5SARS $0F_H$** **DA5SARS $1F_H$**

Typical Usage: Read and written by CPU

Bit	15	14	13	12	11	10	9	8
	PE	CRC ERR	ILEN	MFLE	RAB	OV(1:0)		RXS

Bit	7	6	5	4	3	2	1	0
	WAIT	SP	SAB	SE	unused(3:0)			

PE **Packet End**

A '1' indicates that with the preceding read to register **UA5RXDAT0/ DA5RXDAT0** or **UA5RXDAT1/DA5RXDAT1,** the last two bytes of the current packet have been read.

CRCERR **CRC Error**

A '1' indicates that the CRC32 of the current packet is erroneous.

ILEN **Illegal Length**

A '1' indicates that the length of the current packet is erroneous, i.e the number of octets does not match the length field in the AAL5 trailer or exceeds the maximum supported packet length of 65536 octets.

MFLE **Maximum Frame Length Exceeded**

A '1' indicates that the length of the current packet exceeds the maximum supported packet length of 65536 octets.

RAB **Receive Abort**

A '1' indicates that the length field of the current packet is 0, indicating an aborted or corrupted packet.

OV(1:0) **Octets Valid**

This bit field indicates the number of valid octets in registers **UA5RXDAT0** and **UA5RXDAT1** or **DA5RXDAT0** and **DA5RXDAT1** respectively.

RXS **Receive Packet Start**

A '1' indicates that the first octets of a new packet are available in registers **UA5RXDAT0** and **UA5RXDAT1** or **DA5RXDAT0** and **DA5RXDAT1** respectively.

WAIT **Wait**

A '1' indicates that no valid octets are available in registers **UA5RXDAT0** and **UA5RXDAT1** or **DA5RXDAT0** and **DA5RXDAT1** respectively. Read access to any read register while WAIT is asserted results into an error interrupt.

SP **Segmentation Pending**

A '1' indicates that a cell is ready to be transmitted towards the ABM-3G core. A cell is ready either when 48 octets have been written to **UA5TXDAT0** and **UA5TXDAT1** or **DA5TXDAT0** and **DA5TXDAT1** respectively or when the last cell is being built.
Bit 'SP' is set when the 48-byte transmit buffer is full and it is reset as soon as at least 4-octet space is available for new octets. The microprocessor has to poll this bit before writing the next 48-octet bunch or beginning a new packet. If the microprocessor attempts to write to **UA5TXDAT0** and **UA5TXDAT1** or **DA5TXDAT0** and **DA5TXDAT1** respectively while 'SP' is set, an interrupt is generated and the write access is delayed by the READY signal.

SAB **Segmentation Abort**

A '1' indicates that the transmission of a packet has been aborted because the enable bit EN was reset by the microprocessor before the transmission was completed. The AAL5 unit automatically closed the packet with an abort sequence in the last cell (length field set to 0).

Note: Status bit 'SE' is not set in this case.

SE **Segmentation Ended**

A '1' indicates that the transmission of a packet has been completed successfully.

Note: Status bits SP, SAB, SE are used for transmit, the others for receive.

7.2.4 Buffer Occupation Counter Registers

Register 14 UBufferOcc/DBufferOcc
Upstream/Downstream Buffer Occupation Registers

CPU Accessibility:	**Read only**	
Reset Value:	**0000_H**	
Offset Address:	**UBufferOcc 20_H**	**DBufferOcc 21_H**
Typical Usage:	Read by CPU	

Bit	15	14	13	12	11	10	9	8
	UBufferOcc/DBufferOcc(17:10)							

Bit	7	6	5	4	3	2	1	0
	UBufferOcc/DBufferOcc(9:2)							

UBufferOcc(17:2) Upstream Buffer Occupation Counter

DBufferOcc(17:2) Downstream Buffer Occupation Counter

These bit fields represent the most significant 16 bits of the internal 18-bit wide counters reflecting the number of cells currently stored in the upstream/downstream cell storage RAM.
The CPU determines the buffer fill level with a granularity of 4 by reading register UBufferOcc/DBufferOcc and left shifting the value by 2:
fill_level(17:0):= (xBufferOcc(17:2) << 2)

Register 15 UBufferOccNg/DBufferOccNg
Up-/Downstream Non-Guaranteed Buffer Occupation Registers

CPU Accessibility:	**Read only**		
Reset Value:	**0000_H**		
Offset Address:	**UBufferOccNg 22_H**	**DBufferOccNg 23_H**	
Typical Usage:	Read by CPU		

Bit	15	14	13	12	11	10	9	8
	UBufferOccNg/DBufferOccNg(17:10)							

Bit	7	6	5	4	3	2	1	0
	UBufferOccNg/DBufferOccNg(9:2)							

UBufferOccNg(17:2) Upstream Non-Guaranteed Buffer Occupation Counter

DBufferOccNg(17:2) Downstream Non-Guaranteed Buffer Occupation Counter

These bit fields represent the most significant 16 bits of the internal 18-bit wide counters reflecting the number of **non-guaranteed** cells currently stored in the upstream/downstream cell storage RAM.
The CPU determines the number of cells with a granularity of 4 by reading register UBufferOccNg/DBufferOccNg and left shifting the value by 2:
fill_level(17:0):= (xBufferOccNg(17:2) << 2)
"Non-Guaranteed" cell count refers to cells, that are accepted (stored) because of shared buffer availability although the guaranteed minimum per queue buffer size is already occupied by the specific queue.
The sum of all per queue guaranteed buffer sizes virtually divides the global buffer space into a "guaranteed" part and a "non-guaranteed" (shared) part.

Note: This counter function has been modified from ABM v1.1 since minimum per queue buffer reservation was introduced in ABM-3G v1.1.
In ABM v1.1 these counters represented the number stored "non-real-time" cells belonging to traffic classes with the real-time indication bit 'RTind' cleared in the traffic class table.

7.2.5 Buffer Threshold and Occupation Capture Registers

Register 16 UBufMax/DBufMax
Upstream/Downstream Buffer Maximum Threshold Registers

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**UBufMax**	**24_H**	**DBufMax**	**25_H**
Typical Usage:	Written by CPU			

Bit	15	14	13	12	11	10	9	8
	UBufMax/DBufMax(17:10)							

Bit	7	6	5	4	3	2	1	0
	UBufMax/DBufMax(9:2)							

UBufMax(17:2) **Upstream Buffer Maximum Threshold**

DBufMax(17:2) **Downstream Buffer Maximum Threshold**

These bit fields determine a maximum limit for the total upstream and downstream buffer size with a granularity of 4 cells. The values depend on:

- The size of the external cell pointer RAM,
- Whether the downstream cell storage RAM is connected.

See **Table 7-3** for recommended values.
The CPU programs the maximum number of cells with a granularity of 4 by right shifting the value by 2:
xBufMax(17:2):= (maximum_cells(17:0) >> 2)

Table 7-3 provides typical values and related RAM sizes:

Table 7-3 External RAM Sizes

Cell Pointer SSRAM	Min. Required Upstream Cell SDRAM	Min. Required Downstream Cell SDRAM	UBufMax	Up-stream Buffer	DBufMax	Down-stream Buffer
e.g. 512 k x 32 bit	128 Mb e.g. 2*(4Mb*16)	128 Mb e.g. 2*(4Mb*16)	$3FFFF_H$	256k cells	$3FFFF_H$	256k cells
e.g. 256 k x 32 bit	64 Mb e.g. 1*(2Mb*32)	64 Mb e.g. 1*(2Mb*32)	$1FFFF_H$	128k cells	$1FFFF_H$	128k cells
e.g. 128 k x 32 bit	32 Mb	32 Mb	$0FFFF_H$	64k cells	$0FFFF_H$	64k cells
e.g. 256 k x 32 bit	128 Mb e.g. 2*(4Mb*16)	none	$3FFFF_H$	256k cells	00000_H	0
e.g. 128 k x 32 bit	64 Mb e.g. 1*(2Mb*32)	none	$1FFFF_H$	128k cells	00000_H	0
e.g. 64 k x 32 bit	32 Mb	none	$0FFFF_H$	64k cells	00000_H	0

Note: The upstream cell storage RAM must always be connected.

Note: The size of the cell storage RAMs need not to be specified. Its minimum size is determined by the setting of UBufMax/DbufMax.

Register 17 UMAC/DMAC
Upstream/Downstream Maximum Occupation Capture Registers

CPU Accessibility: **Read only, self-clearing on Read**

Reset Value: **0000_H**

Offset Address: **UMAC** **26_H** **DMAC** **27_H**

Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	UMAC/DMAC(17:10)							

Bit	7	6	5	4	3	2	1	0
	UMAC/DMAC(9:2)							

UMAC(17:2) **Upstream Maximum Occupation Capture Counter**

DMAC(17:2) **Downstream Maximum Occupation Capture Counter**

These bit fields represent the most significant 16 bits of the internal 18-bit wide counters reflecting the absolute maximum number of cells stored in the respective external cell buffer since the last Read access (peak cell filling level within measurement interval).

The CPU determines the maximum number of cells with a granularity of 4 by reading register UMAC/DMAC and left shifting the value by 2:
max_level(17:0):= (xMAC(17:2) << 2)
The counter value is automatically cleared to 0000_H after Read.

Register 18 UMIC/DMIC
Upstream/Downstream Minimum Occupation Capture Registers

CPU Accessibility: **Read only, self-clearing on Read**

Reset Value: **$FFFF_H$**
(modified by chip logic immediately after reset)

Offset Address: **UMIC** **28_H** **DMIC** **29_H**

Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	UMIC/DMIC(17:10)							

Bit	7	6	5	4	3	2	1	0
	UMIC/DMIC(9:2)							

UMIC(17:2) **Upstream Minimum Occupation Capture Counter**

DMIC(17:2) **Downstream Minimum Occupation Capture Counter**

These bit fields represent the most significant 16 bits of the internal 18-bit wide counters reflecting the absolute minimum number of cells stored in the respective external cell buffer since the last Read access (minimum cell filling level within measurement interval).

The CPU determines the minimum number of cells with a granularity of 4 by reading register UMIC/DMIC and left shifting the value by 2:
min_level(17:0):= (xMIC(17:2) << 2)
The counter value is automatically cleared to 0000_H after Read.

Note: The reset value is modified by chip logic immediately after reset or clearing read and thus shall not be included in register reset value test programs.

Register 19 CLP1DIS
CLP1 Discard Global Threshold Registers

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **CLP1DIS** **$2A_H$**
Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	DCLP1DIS(13:6)							

Bit	7	6	5	4	3	2	1	0
	UCLP1DIS(13:6)							

UCLP1DIS(13:6) **Upstream CLP1 Discard Threshold value**

DCLP1DIS(13:6) **Downstream CLP1 Discard Threshold value**

These 8-bit values determine a global 14-bit threshold value (granularity of 64 cells) that enables discard of low-priority (CLP='1') cells.

The threshold values are compared with the per scheduler low priority cell counter SBOccLP (Scheduler Block Low Priority Occupancy) (see **Internal Table 4: Scheduler Block Occupancy Table Transfer Registers SBOC0..SBOC4**) and enables all CLP1 related discard thresholds, i.e.:

TCT1.BufCiCLP1(7:0) (**Register 34: TCT1**)

TCT2.SBCiCLP1(7:0) (**Register 35: TCT2**)

TCT0.QueueCiCLP1(11:0) (**Register 33: TCT0**)

As a second condition, CLP1 related discard thresholds are only effective, if the specific queue that is asked to accept the cell is associated to a traffic class that has EPD function disabled (EPDen='0', see **"Traffic Class Table Transfer Registers TCT0, TCT1, TCT2, TCT3" on Page 195**).

The CPU programs the threshold with a granularity of 64 cells by right shifting the value by 6:
xCLP1DIS(13:6):= (threshold_value(13:0) >> 6)

7.2.6 Configuration Register

Register 20 CONFIG
Configuration Register

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **$2B_H$**
Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	Unused(13:6)							

Bit	7	6	5	4	3	2	1	0
	Unused(5:0)						Reserved1	Unused

Reserved1 **this bit is for internal use only** and must be set to 0 during normal operation.

7.2.7 Backpressure Control Registers

Register 21 UUBPTH0
Upstream UTOPIA Backpressure Threshold Register 0

CPU Accessibility: **Read/Write**
Reset Value: **$FFFF_H$**
Offset Address: **UUBPTH0** **$2C_H$**
Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	UUBPTH0(17:10)							

Bit	7	6	5	4	3	2	1	0
	UUBPTH0(9:2)							

UUBPTH0(17:2) **Upstream UTOPIA Backpressure Threshold 0**
This bit field determines the backpressure threshold for the Upstream UTOPIA Receive Interface Group 0 (see **Chapter 5.1.1**) with a granularity of 4 cells.
The CPU programs the threshold with a granularity of 4 by right shifting the value by 2:
UUBPTH0(17:2):= (maximum_cells(17:0) >> 2)

Register 22 UUBPTH1
Upstream UTOPIA Backpressure Threshold Register 1

CPU Accessibility:	**Read/Write**
Reset Value:	**FFFF$_H$**
Offset Address:	**UUBPTH1** **2D$_H$**
Typical Usage:	Written by CPU

Bit	15	14	13	12	11	10	9	8
	UUBPTH1(17:10)							

Bit	7	6	5	4	3	2	1	0
	UUBPTH1(9:2)							

UUBPTH1(17:2) **Upstream UTOPIA Backpressure Threshold 1**
This bit field determines the backpressure threshold for the Upstream UTOPIA Receive Interface Group 1 (see **Chapter 5.1.1**) with a granularity of 4 cells.
The CPU programs the threshold with a granularity of 4 by right shifting the value by 2:
UUBPTH1(17:2):= (maximum_cells(17:0) >> 2)

Register 23 UUBPTH2
Upstream UTOPIA Backpressure Threshold Register 2

CPU Accessibility:	**Read/Write**
Reset Value:	**FFFF$_H$**
Offset Address:	**UUBPTH2 2E$_H$**
Typical Usage:	Written by CPU

Bit	15	14	13	12	11	10	9	8
	UUBPTH2(17:10)							

Bit	7	6	5	4	3	2	1	0
	UUBPTH2(9:2)							

UUBPTH2(17:2) **Upstream UTOPIA Backpressure Threshold 2**
This bit field determines the backpressure threshold for the Upstream UTOPIA Receive Interface Group 2 (see **Chapter 5.1.1**) with a granularity of 4 cells.
The CPU programs the threshold with a granularity of 4 by right shifting the value by 2:
UUBPTH2(17:2):= (maximum_cells(17:0) >> 2)

Register 24 UUBPTH3
Upstream UTOPIA Backpressure Threshold Register 3

CPU Accessibility: **Read/Write**
Reset Value: **$FFFF_H$**
Offset Address: **UUBPTH3 $2E_H$**
Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	UUBPTH3(17:10)							

Bit	7	6	5	4	3	2	1	0
	UUBPTH3(9:2)							

UUBPTH3(17:2) **Upstream UTOPIA Backpressure Threshold 3**
This bit field determines the backpressure threshold for the Upstream UTOPIA Receive Interface Group 3 (see **Chapter 5.1.1**) with a granularity of 4 cells.
The CPU programs the threshold with a granularity of 4 by right shifting the value by 2:
UUBPTH3(17:2):= (maximum_cells(17:0) >> 2)

Register 25 UBPEI
UTOPIA Backpressure Exceed Indication Register

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**UBPEI** **30_H**
Typical Usage:	Read by CPU

Bit	15	14	13	12	11	10	9	8
	Unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	DUBPEI(3:0)				UUBPEI(3:0)			

DUBPEI(3:0) **Downstream UTOPIA Backpressure Exceed Indication (3:0)**

UUBPEI(3:0) **Upstream UTOPIA Backpressure Exceed Indication (3:0)**

These bits indicate the respective UTOPIA backpressure threshold status.

Bit i (i = 0..3) active indicates, that the backpressure threshold for group i is exceeded (bit = ‘H’) and the UTOPIA Receive Interface backpressures the respective UTOPIA ports.

Register 26 DUBPTH0
Downstream UTOPIA Backpressure Threshold Register 0

CPU Accessibility: **Read/Write**
Reset Value: **$FFFF_H$**
Offset Address: **DUBPTH0** **31_H**
Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	DUBPTH0(17:10)							

Bit	7	6	5	4	3	2	1	0
	DUBPTH0(9:2)							

DUBPTH0(17:2) **Downstream UTOPIA Backpressure Threshold 0**
This bit field determines the backpressure threshold for the Downstream UTOPIA Receive Interface Group 0 (see **Chapter 5.2.1**) with a granularity of 4 cells.
The CPU programs the threshold with a granularity of 4 by right shifting the value by 2:
DUBPTH0(17:2):= (maximum_cells(17:0) >> 2)

Register 27 DUBPTH1
Downstream UTOPIA Backpressure Threshold Register 1

CPU Accessibility: **Read/Write**
Reset Value: **$FFFF_H$**
Offset Address: **DUBPTH1** **32_H**
Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	DUBPTH1(17:10)							

Bit	7	6	5	4	3	2	1	0
	DUBPTH1(9:2)							

DUBPTH1(17:2) **Downstream UTOPIA Backpressure Threshold 1**
This bit field determines the backpressure threshold for the Downstream UTOPIA Receive Interface Group 1 (see **Chapter 5.2.1**) with a granularity of 4 cells.
The CPU programs the threshold with a granularity of 4 by right shifting the value by 2:
DUBPTH1(17:2):= (maximum_cells(17:0) >> 2)

Register 28 DUBPTH2
Downstream UTOPIA Backpressure Threshold Register 2

CPU Accessibility: **Read/Write**
Reset Value: **$FFFF_H$**
Offset Address: **DUBPTH2** **33_H**
Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	DUBPTH2(17:10)							

Bit	7	6	5	4	3	2	1	0
	DUBPTH2(9:2)							

DUBPTH2(17:2) **Downstream UTOPIA Backpressure Threshold 2**
This bit field determines the backpressure threshold for the Downstream UTOPIA Receive Interface Group 2 (see **Chapter 5.2.1**) with a granularity of 4 cells.
The CPU programs the threshold with a granularity of 4 by right shifting the value by 2:
DUBPTH2(17:2):= (maximum_cells(17:0) >> 2)

Register 29 DUBPTH3
Downstream UTOPIA Backpressure Threshold Register 3

CPU Accessibility: **Read/Write**
Reset Value: **$FFFF_H$**
Offset Address: **DUBPTH3 34_H**
Typical Usage: Written by CPU

Bit	15	14	13	12	11	10	9	8
	DUBPTH3(17:10)							

Bit	7	6	5	4	3	2	1	0
	DUBPTH3(9:2)							

DUBPTH3(17:2) **Downstream UTOPIA Backpressure Threshold 3**
This bit field determines the backpressure threshold for the Downstream UTOPIA Receive Interface Group 3 (see **Chapter 5.2.1**) with a granularity of 4 cells.
The CPU programs the threshold with a granularity of 4 by right shifting the value by 2:
DUBPTH3(17:2):= (maximum_cells(17:0) >> 2)

7.2.8 LCI Table Transfer Registers

Internal Table 1: LCI Table Transfer Registers LCI0, LCI1, LCI2

These registers are used to access the internal Local Connection Identifier (LCI) table containing 16384 entries (one entry serves for upstream and downstream direction). **Table 7-4** shows an overview of the registers involved.

Table 7-4 Registers for LCI Table Access

47		0	
LCI RAM entry			RAM select:
15 0	15 0	15 0	15 0
LCI2	LCI1	LCI0	MAR=00_H
			LCI select:
15 0	15 0	15 0	15 0
MASK2	MASK1	MASK0	WAR (0..16383_D)

LCI0, LCI1 and LCI2 are the transfer registers for one 48-bit LCI table entry. The LCI value representing the table entry which needs to be read or written must be written to the Word Address Register (WAR). The dedicated LCI table entry is read into the LCI0/LCI1/LCI2 Registers or modified by the LCI0/LCI1/LCI2 Register values with a write mechanism. The associated Mask Registers MASK0 to MASK2 allow a bit-wise masking for Write operation (0 - unmasked, 1 - masked). In case of Read operation, the dedicated LCI0/LCI1/LCI2 register bit will be overwritten by the respective LCI table entry bit value. In case of Write operation, the dedicated LCI0/LCI1/LCI2 register bit will modify the respective LCI table entry bit value.

The Read or Write process is controlled by the Memory Address Register (MAR). The 5 LSBs (= Bit 4..0) of the MAR select the memory/table that will be accessed; to select the LCI table bit field MAR(4:0) must be set to 0. Bit 5 of the MAR starts the transfer and is automatically cleared after execution.

Table 7-5 WAR Register Mapping for LCI Table Access

Bit	15	14	13	12	11	10	9	8
	Unused(2:0)		LCISel(13:8)					

Bit	7	6	5	4	3	2	1	0
	LCISel(7:0)							

LCISel(13:0) Selects an LCI entry within the range (0..16383).

Register 30 LCI0
LCI Transfer Register 0

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **LCI0** **$3B_H$**

Typical Usage: Written and Read by CPU to maintain the LCI table

Bit	15	14	13	12	11	10	9	8
	Unused(13:6)							

Bit	7	6	5	4	3	2	1	0
	Unused(5:0)						CLPT	ABM core

CLPT **CLP Transparent**:
Specifies whether the CLP bit of cells belonging to this connection is evaluated or not in threshold checks. Valid for both upstream and downstream cores. Does not affect SBOC counters.

0 CLP bit is evaluated.

1 CLP bit is not evaluated; all cells are treated as high priority cells assuming CLP=0.

ABMcore **ABM-3G Core Selection**:
This bit is valid in Uni-directional Mode only and specifies the core responsible for cells of this LCI.

0 Scheduler Blocks 0..127 are selected (core 0).

1 Scheduler Blocks 128..255 are selected (core 1).

Register 31 LCI1
LCI Transfer Register 1

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **LCI1** **$3C_H$**

Typical Usage: Written and Read by CPU to maintain the LCI table

Bit	15	14	13	12	11	10	9	8
	DnQID(12:5)							

Bit	7	6	5	4	3	2	1	0
	DnQID(4:0)					Dnflags(2:0)		

DnQID(12:0) **Downstream Queue Identifier**.
Specifies the queue (0..8191) in which the cells of the connection are stored.

Dnflag 2 **Last cell of packet flag for downstream direction**;
This bit is autonomously used by the EPD function of the ABM-3G.
Initialize to 1 at connection setup.
Do not Write during normal operation.

Dnflag 1 **Discard packet flag in downstream direction**;
This bit is autonomously used by the EPD function of the ABM-3G.
Initialize to 0 at connection setup.
Do not Write during normal operation.

Dnflag 0 **Discard rest of packet flag in downstream direction**;
This bit is autonomously used by the EPD function of the ABM-3G.
Initialize to 0 at connection setup.
Do not Write during normal operation.

Register 32 LCI2
LCI Transfer Register 2

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **LCI1** **$3D_H$**
Typical Usage: Written and Read by CPU to maintain the LCI table

Bit	15	14	13	12	11	10	9	8
	UpQID(12:5)							

Bit	7	6	5	4	3	2	1	0
	UpQID(4:0)					Upflags(2:0)		

UpQID(12:0) **Upstream Queue Identifier**.
Specifies the queue (0..8191) in which the cells of the connection are stored.

Upflag 2 **Last cell of packet flag for upstream direction**;
This bit is autonomously used by the EPD function of the ABM-3G.
Initialize to 1 at connection setup.
Do not Write during normal operation.

Upflag 1 **Discard packet flag in upstream direction**;
This bit is autonomously used by the EPD function of the ABM-3G.
Initialize to 0 at connection setup.
Do not Write during normal operation.

Upflag 0 **Discard rest of packet flag in upstream direction**;
This bit is autonomously used by the EPD function of the ABM-3G.
Initialize to 0 at connection setup.
Do not Write during normal operation.

7.2.9 Traffic Class Table Transfer Registers

Internal Table 2: Traffic Class Table Transfer Registers TCT0, TCT1, TCT2, TCT3

The Traffic Class Table Transfer Registers are used to access the internal Traffic Class Table (TCT) containing 2*16 entries of 4*64 bits each (16 traffic classes per ABM-3G core, 4 words of 64 bits per entry). **Table 7-6** shows an overview of the registers involved.

Table 7-6 Registers for TCT Table Access

63			0	
TCT RAM entry				RAM select:
15 0	15 0	15 0	15 0	15 0
TCT3	TCT2	TCT1	TCT0	MAR=01_H
				TCT entry select:
15 0	15 0	15 0	15 0	15 0
MASK3	MASK2	MASK1	MASK0	WAR (0..127_D)

TCT0, TCT1, TCT2 and TCT3 are the transfer registers used to access the 4*64 bit TCT table entries.

Core selection, traffic class number, and 64-bit word selection of the table entry which needs to be read or written must be programmed to the Word Address Register (WAR). The dedicated TCT table entry 64-bit word is read into the TCT3/TCT2/TCT1/TCT0 registers or modified by the TCT3/TCT2/TCT1/TCT0 register values with a write mechanism. The associated Mask Registers MASKi (i=3..0) allow a bit-wise masking for Write operation (0 - unmasked, 1 - masked). In case of Read operation, the dedicated TCTi (i=3..0) register bit will be overwritten by the respective TCT table entry bit value. In case of Write operation, the dedicated TCTi (i=3..0) register bit will modify the respective TCT table entry bit value.

The Read or Write process is controlled by the Memory Address Register (MAR). The 5 LSBs (= Bit 4..0) of the MAR select the memory/table that will be accessed; to select the TCT table bit field MAR(4:0) must be set to 1. Bit 5 of MAR starts the transfer and is automatically cleared after execution.

Table 7-7 WAR Register Mapping for TCT Table Access

Bit	15	14	13	12	11	10	9	8
	Unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	Unused	CoreSel	TCID(3:0)				word64Sel(1:0)	

CoreSel **Selects the ABM-3G core for TCT table access**:

0 Upstream core selected (Core 0)

1 Downstream core selected (Core 1)

TCID(3:0) **Selects The Traffic Class** for the TCT table access in the range (0..15).

word64Sel(1:0) **Selects The 64-Bit Word** of the 256-bit TCT table entry for access:

00 Bit field (63..0) of traffic class entry is selected.

01 Bit field (127..64) of traffic class entry is selected.

10 Bit field (191..128) of traffic class entry is selected.

11 Bit field (255..192) of traffic class entry is selected.

The meaning of registers TCTi (i=3..0) depends on the word selection bit field 'word64Sel(1:0)' in the WAR, because 256-bit TCT entries are mapped to 64 bits of registers TCTi (i=3..0) by this selection:

<table>
<tr><th>WAR modulo 4</th><th colspan="4">63</th><th colspan="4">56</th><th colspan="4">55</th><th colspan="4">48</th><th colspan="4">47</th><th colspan="4">40</th><th colspan="4">39</th><th colspan="4">32</th></tr>
<tr><td>3</td><td colspan="32">LostCellsTotal(31:0)[1]</td></tr>
<tr><td>2</td><td colspan="32">AcceptedCells/Packets(31:0)[1]</td></tr>
<tr><td>1</td><td colspan="8">TrafClassMax(7:0)</td><td colspan="8">SBMax(7:0)</td><td colspan="4">unused(3:0)</td><td colspan="12">SBCiCLP1(11:0)</td></tr>
<tr><td>0</td><td colspan="3">DH (2:0)</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td colspan="4">unused(3:0)</td><td colspan="16">unused(15:0)</td></tr>
<tr><td></td><td colspan="16">TCT3(15:0)</td><td colspan="16">TCT2(15:0)</td></tr>
</table>

[1] All 5 statistical counters stop at their maximum value. Counters must be set to 0 after read.

<table>
<tr><th>WAR modulo 4</th><th colspan="4">31</th><th colspan="4">24</th><th colspan="4">23</th><th colspan="4">16</th><th colspan="4">15</th><th colspan="4">8</th><th colspan="4">7</th><th colspan="4">0</th></tr>
<tr><td>3</td><td colspan="8">unused(7:0)</td><td colspan="4">LostCellsBuffer (3:0)[1]</td><td colspan="4">LostCellsSB(3:0) [1]</td><td colspan="16">LostPackets/CLP1Cells(15:0)[1]</td></tr>
<tr><td>2</td><td colspan="14">unused(13:0)</td><td colspan="18">TrafClassOccNg(17:0)</td></tr>
<tr><td>1</td><td colspan="8">unused(7:0)</td><td colspan="8">QueueMax(7:0)</td><td colspan="4">unused(3:0)</td><td colspan="12">QueueCiCLP1(11:0)</td></tr>
<tr><td>0</td><td colspan="8">unused(7:0)</td><td colspan="8">BufCiCLP1(7:0)</td><td colspan="8">BufMaxNg(7:0)</td><td colspan="8">BufEPDNg(7:0)</td></tr>
<tr><td></td><td colspan="16">TCT1(15:0)</td><td colspan="16">TCT0(15:0)</td></tr>
</table>

[1] All 5 statistical counters stop at their maximum value. Counters must be set to 0 after read.

Note: - grey fields are 'unused', it is recommended to mask them for write access
- green fields must be configured (written) by the CPU
- blue fields are statistical counter values optionally read by CPU

Register 33 TCT0
TCT Transfer Register 0

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**TCT0** **$3E_H$**
Typical Usage:	Written and Read by CPU to maintain the TCT table; the meaning of register TCT0 depends on the bit field 'Word64Sel' in WAR;

Register WAR.Word64Sel(1:0) ='00':

Bit	15	14	13	12	11	10	9	8
	BufMaxNg(7:0)							

Bit	7	6	5	4	3	2	1	0
	BufEPDNg(7:0)							

BufMaxNg(7:0) **Maximum Buffer Fill Threshold for a non-real-time traffic class configuration** (register TCT1, DwordSel=00).
The first cell exceeding this threshold is discarded and if also PPD is enabled for this traffic class (register TCT1, DwordSel=00, PPDen=1) PPD is applied on a per connection (LCI) basis.
The threshold is defined with a granularity of 1024 cells:
Threshold = BufMaxNg(7:0) * 1024 Cells

BufEPDNg(7:0) **EPD threshold for a non-real-time traffic class configuration** (register TCT1, DwordSel='00').
If the buffer fill exceeds this threshold and EPD is enabled for this traffic class (register TCT1, DwordSel=00, EPDen=1) EPD is applied on a per connection (LCI) basis.
The threshold is defined with a granularity of 1024 cells:
Threshold = BufEPDNg(7:0) * 1024Cells

Register WAR.Word64Sel(1:0) ='01':

Bit	15	14	13	12	11	10	9	8
	unused(3:0)				QueueCiCLP1(11:8)			

Bit	7	6	5	4	3	2	1	0
	QueueCiCLP1(7:0)							

QueueCiCLP1 (11:0) **Combined Queue Threshold of this Traffic Class** for the following cases:

a) if CLPT=0 (CLP transparent bit is not true) and EPDen=0
⇒ CLP1 queue threshold for CLP=1 cells
(cells with CLP=1 are discarded)

b) if CLPT=0 and EPDen=1
⇒ EPD GFR queue threshold. If that threshold and additionally BufNrtEPD (of the respective traffic class) is exceeded then EPD is triggered.

The threshold is defined with a granularity of 4:
Threshold = QueueCiCLP1(7:0) * 4 Cells

Register WAR.Word64Sel(1:0) ='10':

Bit	15	14	13	12	11	10	9	8
	TrafClassOccNg(15:8)							

Bit	7	6	5	4	3	2	1	0
	TrafClassOccNg(7:0)							

TrafClassOccNg (15:0) **Current Buffer Occupation** in number of cells for this traffic class.
Do not Write in normal operation.

Register WAR.Word64Sel(1:0) ='11':

Bit	15	14	13	12	11	10	9	8
	LostPackets/CLP1Cells(15:8)							

Bit	7	6	5	4	3	2	1	0
	LostPackets/CLP1Cells(7:0)							

LostPackets/ CLP1Cells (15:0)	**Count of Lost Packets due to EPD Overflow** for this traffic class or count of lost CLP=1 cells due to CLP threshold overflow. Automatically reset after Read access.

Register 34 TCT1
TCT Transfer Register 1

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**TCT1** **$3F_H$**
Typical Usage:	Written and Read by CPU to maintain the TCT table; the meaning of register TCT1 depends on the bit field 'Word64Sel' in WAR;

Register WAR.Word64Sel(1:0) ='00':

Bit	15	14	13	12	11	10	9	8
	unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	BufCiCLP1(17:10)							

BufCiCLP1 (17:10) **Buffer EPD CLP1 Threshold**

This 8-bit value determines a global cell filling level threshold with a granularity of 1024 cells that triggers early packet discard (EPD) for CLP=1 tagged frames used by GFR traffic class service (low watermark).

The threshold values are compared with the non guaranteed Buffer Occupancy counters UBufferOccNg, DBufferOccNg respectively.

The CPU programs the threshold with a granularity of 1024 cells by right shifting the value by 10:

BufCiCLP1(17:10):= (threshold_value(17:0) >> 10)

Note: In ABM v1.1 this threshold was determined by registers UEC and DEC.

Register WAR.Word64Sel(1:0) ='01':

Bit	15	14	13	12	11	10	9	8
	unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	QueueMax(7:0)							

QueueMax (7:0)
This 8-bit value determines the maximum queue length with a granularity of 64 cells.
The CPU programs the maximum queue length with a granularity of 64 cells by right shifting the value by 6:

QueueMax(7:0):= queuelength >> 6

The maximum length of any queue is limited to (255*64) = 16320 cells.

Register WAR.Word64Sel(1:0) ='10':

Bit	15	14	13	12	11	10	9	8
	unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	unused(5:0)						TrafClassOccNg (17:16)	

TrafClassOccNg (17:16)
MSBs of Current Buffer Occupation Counter
TrafClassOccNg(17:0) counts the number of cells stored for this traffic class.
Do not Write in normal operation.

Register WAR.Word64Sel(1:0) ='11':

Bit	15	14	13	12	11	10	9	8
	unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	LostCellsBuffer(3:0)				LostCellsSB(3:0)			

LostCellsBuffer (3:0)	**Count of Lost Cells due to Buffer Overflow** for this traffic class. Automatically reset after Read access.
LostCellsSB (3:0)	**Count of Lost Cells due to Scheduler Block Overflow** for this traffic class. Automatically reset after Read access.

Register 35 TCT2
TCT Transfer Register 2

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**TCT2** **40_H**
Typical Usage:	Not used by CPU; the meaning of register TCT2 depends on the bit field 'Word64Sel' in WAR;

Register WAR.Word64Sel(1:0) ='00':

Bit	15	14	13	12	11	10	9	8
	unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	unused(7:0)							

Register WAR.Word64Sel(1:0) ='01':

Bit	15	14	13	12	11	10	9	8
	unused(3:0)				SBCiCLP1(11:8)			

Bit	7	6	5	4	3	2	1	0
	SBCiCLP1(7:0)							

SBCiCLP1(11:0) **Scheduler Block Ci/CLP1 Threshold**
This threshold determines a maximum number of low priority cells allowed to be stored per scheduler block with a granularity of 64 cells.
The CPU programs the threshold with a granularity of 64 cells by right shifting the value by 6:

SBCiCLP1(11:0):= threshold >> 6

Register WAR.Word64Sel(1:0) ='10':

Bit	15	14	13	12	11	10	9	8
	AcceptedCells/Packets(15:8)							

Bit	7	6	5	4	3	2	1	0
	AcceptedCells/Packets(7:0)							

AcceptedCells/ Packets (15:0) **Count of Accepted Cells or AAL5 Units** within this traffic class, depending on flag **SCNT** in **TCT3**.
If **SCNT** = 0:
This counter is incremented when a user data cell with AAL_ indication=1 is accepted (Packet end indication in AAL5: PTI= xx1).
If **SCNT** = 1 all accepted cells are counted
Do not Write in normal operation.
Must be reset after Read access.

Register WAR.Word64Sel(1:0) ='11':

Bit	15	14	13	12	11	10	9	8
	LostCellsTotal(15:8)							

Bit	7	6	5	4	3	2	1	0
	LostCellsTotal(7:0)							

LostCellsTotal (15:0)	Count of all lost cells for this traffic class. Do not Write in normal operation. Must be reset after Read access.

Register 36 TCT3
TCT Transfer Register 3

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**TCT3** **41_H**
Typical Usage:	Written and Read by CPU to maintain the TCT table; the meaning of register TCT3 depends on the bit field 'Word64Sel' in WAR;

Register WAR.Word64Sel(1:0) ='00':

Bit	15	14	13	12	11	10	9	8
	DH(2:0)			unused	0	0	EPDen	PPDen

Bit	7	6	5	4	3	2	1	0
	SCNT	0	GFRen	0	unused(3:0)			

DH (2:0)

DeltaHysteresis for threshold evaluations with hysteresis applied:

This value is per traffic class, but is evaluated individually for each effected threshold TH relative to the threshold size. The hysteresis determines a lower threshold TL with
$TL_i := TH_i - Delta_i$

The $Delta_i$ value is determined by bit field DH(2:0) and TH_i with:
$Delta_i := TH_i >> [DH(2:0) +1]$

The following table shows the operation and resulting TL_i values for the example of a threshold programmed to 256 cells:

DH(2:0):	$Delta_i$:=		Example:
0d	0	(hysteresis disabled)	TL_i:= 256
1d	TH_i >>2		TL_i:= 192
2d	TH_i >>3		TL_i:= 224
3d	TH_i >>4		TL_i:= 240

4d	TH_i >>5		TL_i:= 248
5d	TH_i >>6		TL_i:= 252
6d	TH_i >>7		TL_i:= 254
7d	TH_i >>8	(hysteresis ineffective)	TL_i:= 256

EPDen **EPD for the individual traffic class**. EPD is used for every connection (LCI) within that traffic class (see **Chapter 3.4.1.6.3**):

0	EPD is disabled.
1	EPD is enabled.

PPDen **PPD for the individual traffic class**. PPD is used for every connection (LCI) within that traffic class (see **Chapter 3.4.1.6.3**):

0	PPD is disabled
1	PPD is enabled

SCNT **Counter Function Select**
This bit selects the function of counter 'AcceptedCells/Packets(31:0)':

0	Accepted Packets are counted
1	Accepted Cells are counted

GFRen **GFR Enable**:
This bit enables a modified EPD threshold evaluation for GFR traffic (see **Chapter 3.4.1.6.3**).

0	Modified EPD threshold evaluation for GFR disabled
1	Modified EPD threshold evaluation for GFR enabled

Register WAR.Word64Sel(1:0) ='01':

Bit	15	14	13	12	11	10	9	8
	TrafClassMax(7:0)							

Bit	7	6	5	4	3	2	1	0
	SBMax(7:0)							

TrafClassMax (7:0) — **Maximum Traffic Class Fill Threshold** (determines the maximum number of cells in all queues associated with this traffic class). The threshold is defined with a granularity of 1024:
Threshold = TrafClassMax(7:0) * 1024 Cells

SBMax(7:0) — **Combined Threshold of the Maximum Number of Buffered Cells** in the Scheduler Block; that is, all cells which are in the traffic classes (= cells in the corresponding queues) of the Scheduler Block for the following cases:
a) If EPDen=0
⇒ Maximum Scheduler Block fill threshold for CLP='0/1' cells
b) If EPDen=1
⇒ EPD Scheduler Block threshold
The threshold is defined with a granularity of 1024:
Threshold = SBMax(7:0) * 1024 Cells

Register WAR.Word64Sel(1:0) ='10':

Bit	15	14	13	12	11	10	9	8
	AcceptedCells/Packets(31:24)							

Bit	7	6	5	4	3	2	1	0
	AcceptedCells/Packets(23:16)							

AcceptedCells/ Packets (31:16) — **Count of Accepted Cells or AAL5 Units** within this traffic class, depending on flag **SCNT** in **TCT3**.
If **SCNT** = 0:
This counter is incremented when a user data cell with AAL_ indication=1 is accepted (Packet end indication in AAL5: PTI= xx1).
If **SCNT** = 1 all accepted cells are counted
Do not Write in normal operation.
Must be reset after Read access.

Register WAR.Word64Sel(1:0) ='11':

Bit	15	14	13	12	11	10	9	8
	LostCellsTotal(31:24)							

Bit	7	6	5	4	3	2	1	0
	LostCellsTotal(23:16)							

LostCellsTotal (31:16)	Count of all lost cells for this traffic class. Do not Write in normal operation. Must be reset after Read access.

7.2.10 Queue Configuration Table Transfer Registers

Internal Table 3: Queue Configuration Table Transfer Registers QCT0..6

Queue Configuration Table Transfer Registers are used to access the internal Queue Configuration Table (QCT) containing 2*8192 entries. The lower 8K entries control the upstream core queues and the upper 8K entries control the downstream core queues. **Table 7-8** shows an overview of the registers involved. Some fields are not used for entry 0 (common real time bypass)

Table 7-8 Registers for Queue Configuration Table Access

111						0	
QCT RAM entry							RAM select:
15 0	15 0	15 0	15 0	15 0	15 0	15 0	15 0
QCT6	QCT5	QCT4	QCT3	QCT2	QCT1	QCT0	MAR=02_H
							Queue select:
15 0	15 0	15 0	15 0	15 0	15 0	15 0	15 0
MASK6 =$FFFF_H$	MASK5 =$FFFF_H$	MASK4 =$FFFF_H$	MASK3 =$FFFF_H$	MASK2	MASK1	MASK0 =$FFFF_H$	WAR ($0..16383_D$)

QCT0...QCT6 are the transfer registers for one 112 bit QCT table entry. The core selection and queue number representing the table entry which needs to be read or written must be written to the Word Address Register (WAR). The dedicated QCT table entry is read into the QCT0..QCT6 registers or modified by the QCT0..QCT6 register values with a write mechanism. The associated Mask Registers MASK0..MASK6 allow a bit-wise Write operation (0 - unmasked, 1 - masked). In case of Read operation, the dedicated QCT0..QCT6 register bit will be overwritten by the respective QCT table entry bit value. In case of Write operation, the dedicated QCT0..QCT6 register bit will modify the respective QCT table entry bit value.

Note: It is recommended not to Write to bit fields (111:64) and (15:0) of the QCT table entries; i.e. registers MASK0, MASK6, MASK5, MASK4 and MASK3 should always be programmed with $FFFF_H$.

The 13 LSBs (= Bit 12..0) of the WAR register select the queue-specific entry that will be accessed and bit ’CoreSel’ the ABM-3G core.

The Read or Write process is controlled by the Memory Address Register (MAR). The 5 LSBs (= Bit 4..0) of the MAR select the memory/table that will be accessed; to select the QCT table, bit field MAR(4:0) must be set to 2. Bit 5 of MAR starts the transfer and is automatically cleared after execution.

Table 7-9 WAR Register Mapping for LCI Table Access

Bit	15	14	13	12	11	10	9	8
	unused(1:0)		CoreSel	QSel(12:8)				

Bit	7	6	5	4	3	2	1	0
	QSel(7:0)							

CoreSel **Selects an ABM-3G Core**:

0 Upstream core selected

1 Downstream core selected

QSel(12:0) **Selects a Queue Entry** within the range (0..8191).

Register 37 QCT0
Queue Configuration Transfer Register 0

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**QCT0** **42_H**
Typical Usage:	Read by CPU

Bit	15	14	13	12	11	10	9	8
	Unused(1:0)		QueueLength(13:8)					

Bit	7	6	5	4	3	2	1	0
	QueueLength(7:0)							

QueueLength (13:0)	Represents the **Current Number of Cells Stored in this Queue**. Do not Write in normal operation.

Register 38 QCT1
Queue Configuration Transfer Register 1

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**QCT1** **43_H**
Typical Usage:	Written and Read by CPU to maintain the LCI table

Bit	15	14	13	12	11	10	9	8
	DQac	RSall	0	0	TCID(3:0)			

Bit	7	6	5	4	3	2	1	0
	QIDvalid	SBID(6:0)						

DQac **Dummy Queue Action**

This bit is a command bit that must always be set when a dummy queue is activated or deactivated.

Note: Read access to this command bit will always return '0'.

RSall **ReSchedule Always**

This bit determines the queue scheduling process:

'0' The queue is only scheduled/re-scheduled with its specific rate while the queue is not empty (normal operation).

’1’ The queue is always scheduled/re-scheduled with its specific rate independent of the queue filling level. Scheduling an empty queue results in an ’empty cell cycle’ (no cell is emitted during this cycle).
A so called ’dummy queue’ is used for generating empty cell cycles.

*Note: ’**RSall**’ can be set with connection setup (together with **QIDvalid**=’1’) or anytime while the queue is enabled.*
*After setting bit ’**RSall**’, the ABM-3G will automatically set bit ’**MGconf/DQsch**’ to acknowledge the first dummy schedule event.*
*The ’**RSall**’ information is internally conveyed to the scheduler. This process is acknowledged by an interrupt (Bit ’**UDQRD/DDQRD**’ in **Register 103: ISRC**). It is recommended not to select any other table or table entry while waiting for this acknowledge.*

*Note: ’**RSall**’ can be reset anytime while the queue is enabled. In response to resetting ’**RSall**’ the ABM-3G will generate an interrupt (Bit ’**UDQRD/DDQRD**’ in **Register 103: ISRC**) and reset bit ’**MGconf/DQsch**’ in this table.*

*Note: To activate or deactivate a dummy queue, command bit ’**DQac**’ must be set in conjunction with setting or resetting bit ’**RSall**’.*

QIDvalid **Queue Enable**:

	0	Queue disabled. An attempt to store a cell to a disabled queue leads to discard of the cell and a **QIDINV** interrupt is generated. If a filled queue gets disabled, cells may still be in the queue. In this case the disabled queue is still scheduled, and cells are logically emitted from the queue but will not be transmitted. Actual filling of the queue can be obtained via QueueLength(13:0) parameter in the QCT entry. *Note: To disable an active VC-merge group, bit ’**QIDvalid** must be reset. Deactivating the queue by setting **QIDvalid**=’0’ automatically starts an internal process to delete the queue from the VC-merge group. In response to resetting ’**QIDvalid**’ the ABM-3G will generate an interrupt (Bit ’**UQVCMGD**/**DQVCMGD**’ in **Register 103: ISRC**) and reset bit ’**MGconf/DQsch**’ in this table.*
	1	Queue enabled. Cells are allowed to enter the queue.
TCID(3:0)	**Traffic Class Number** (0..15) Assigns the queue to one of the 16 traffic classes defined in the traffic class table TCT for this core.	
SBID(6:0)	**Scheduler Block Number** (0..127) Assigns the queue to one of the 128 schedulers of this core.	

Register 39 QCT2
Queue Configuration Transfer Register 2

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**QCT2** **44_H**
Typical Usage:	Written by CPU to configure VC-Merge operation

Bit	15	14	13	12	11	10	9	8
	MGconf/ DQsch	MGID(6:0)						

Bit	7	6	5	4	3	2	1	0
	MinBG(7:0)							

MGconf/DQsch **Merge Group Configured/ Dummy Queue Scheduled**

The meaning of this flag depends on bit ’**RSall**’:

RSall=’0’
The queue is not configured as a ’dummy queue’ and may be configured as a VC-merge group member:
MGconf

0 The queue is neither a dummy queue, nor member of a VC-merge group.

1 The queue is member of a VC-merge group. The VC-merge group is determined by bit field ’MGID(6:0).

*Note: To disable an active VC-merge group, bit ’**QIDvalid**’ must be reset. Deactivating the queue by setting **QIDvalid**=’0’ automatically starts an internal process to delete the queue from the VC-merge group. In response to resetting ’**QIDvalid**’ the ABM-3G will generate an interrupt (Bit ’**UQVCMGD**/**DQVCMGD**’ in **Register 103: ISRC**) and reset bit ’**MGconf/DQsch**’ in this table.*

RSall=’1’
The queue is configured as a ’dummy queue’:
DQsch

0	The queue is activated as a 'dummy queue', but no first dummy schedule event has occurred.
1	The queue is activated as a 'dummy queue' and at least one first dummy schedule event has occurred.

*Note: '**RSall**' can be reset anytime while the queue is enabled. In response to resetting '**RSall**' the ABM-3G will generate an interrupt (Bit '**UDQRD/ DDQRD**' in **Register 103: ISRC**) and reset bit '**MGconf/DQsch**' in this table.*

MGID(6:0) **Merge Group Number** (0..127)
Assigns the queue to one of 128 merge groups of this core.

MinBG(7:0) **Minimum Buffer Guarantee**
This bit field determines a minimum buffer reservation for this particular queue. The sum of all minimum buffer reservations virtually divides the total buffer into a 'Guaranteed' part and a shared 'Non-Guaranteed' part.
The minimum buffer reservation offers to granularities depending on MSB of MinBG(7):

MinBG(7) := 0	Granularity of 1 cell for short queues (e.g. real-time queues): The minimum reserved buffer in number of cells is *reserved_buffer = MinBG(6:0) = {0,1,2,..127}*
MinBG(7) := 1	Granularity of 8 cells for long queues (e.g. non-real-time queues): The minimum reserved buffer in number of cells is *reserved_buffer = MinBG(6:0) << 3 = {0,8,16,..1016}*

Register 40 QCT3

Queue Configuration Transfer Register 3

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **QCT3** **45_H**

Typical Usage: Not used by CPU

Bit	15	14	13	12	11	10	9	8
	unused(11:4)							

Bit	7	6	5	4	3	2	1	0
	unused(3:0)				EOP	reserved	reserved	reserved

EOP **EOP-Flag:**

Do not Write during normal operation.

Register 41 QCT4
Queue Configuration Transfer Register 4

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **QCT4** **46_H**
Typical Usage: Not used by CPU

Bit	15	14	13	12	11	10	9	8
	Reserved(15:8)							

Bit	7	6	5	4	3	2	1	0
	Reserved(7:0)							

Reserved(15:0) Do not Write in normal operation.

Register 42 QCT5
Queue Configuration Transfer Register 5

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **QCT5** **47_H**
Typical Usage: Not used by CPU

Bit	15	14	13	12	11	10	9	8
	Reserved(15:8)							

Bit	7	6	5	4	3	2	1	0
	Reserved(7:0)							

reserved(15:0) Do not Write in normal operation.

Register 43 QCT6
Queue Configuration Transfer Register 6

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **QCT6** **48_H**
Typical Usage: Not used by CPU

Bit	15	14	13	12	11	10	9	8
	Reserved(15:8)							

Bit	7	6	5	4	3	2	1	0
	Reserved(7:0)							

reserved(15:0) Do not Write in normal operation.

7.2.11 Scheduler Block Occupancy Table Transfer Registers

Internal Table 4:
Scheduler Block Occupancy Table Transfer Registers SBOC0..SBOC4

The Scheduler Block Occupancy Table Transfer Registers are used to access the internal Scheduler Block Occupancy Table (SBOC) containing 2*128 entries of 80 bit each. **Table 7-10** shows an overview of the registers involved.

Note: The SBOC table information is typically not required by the CPU. The SBOC maintains global counters that are internally used for threshold evaluation.
For statistical purposes, reading the SBOC entries provides a snap shot of the respective scheduler occupation situation distinguished by priorities and also the current number of discarded low priority cells.

Table 7-10 Registers for SBOC Table Access

79				0	
SBOC RAM entry					RAM Select:
15 0	15 0	15 0	15 0	15 0	15 0
SBOC4	SBOC3	SBOC2	SBOC1	SBOC0	MAR=03_H
					Entry select:
15 0	15 0	15 0	15 0	15 0	15 0
MASK4	MASK3	MASK2	MASK1	MASK0	WAR (0..255_D)

SBOC0..SBOC4 are the transfer registers for one 80-bit SBOC table entry. The Scheduler Block number representing the table entry which needs to be read or written must be written to the Word Address Register (WAR). The dedicated SBOC table entry is read into the SBOC0..SBOC4 Registers or modified by the SBOC0..SBOC4 register values with a write mechanism. The associated Mask Registers MASK0..MASK4 allow a bit-wise Write operation (0 - unmasked, 1 - masked). In case of Read operation, the dedicated SBOC0..SBOC4 register bit will be overwritten by the respective SBOC table entry bit value. In case of Write operation, the dedicated SBOC0..SBOC4 register bit will modify the respective SBOC table entry bit value.

The Read or Write process is controlled by the Memory Address Register (MAR). The 5 LSBs (= Bit 4..0) of the MAR register select the memory/table that will be accessed; to select the SBOC table, bit field MAR(4:0) must be set to 3. Bit 5 of MAR starts the transfer and is automatically cleared after execution.

Table 7-11 WAR Register Mapping for SBOC Table Access

Bit	15	14	13	12	11	10	9	8
	Unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	CoreSel	SchedSel(6:0)						

CoreSel **Selects an ABM-3G core**:

0	Upstream core selected
1	Downstream core selected

SchedSel(6:0) **Selects one of the 128 core-specific Scheduler Blocks**.

Register 44 SBOC0
SBOC Transfer Register 0

CPU Accessibility:	**Read only**
Reset Value:	**0000**$_H$
Offset Address:	**SBOC0** **49**$_H$
Typical Usage:	Read by CPU

Bit	15	14	13	12	11	10	9	8
	SBOccNg(1:0)		SBOccHP(1:0)		SBOccLP(1:0)		SBOccLPd(1:0)	

Bit	7	6	5	4	3	2	1	0
	Reserved(7:0)							

Register 45 SBOC1
SBOC Transfer Register 1

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **SBOC1** **$4A_H$**
Typical Usage: Read by CPU (for debug purposes or statistics)

Bit	15	14	13	12	11	10	9	8
	SBOccLPd(17:10)							

Bit	7	6	5	4	3	2	1	0
	SBOccLPd(9:2)							

SBOccLPd (17:2) **Scheduler Block Occupancy Counter Low Priority Discarded Cells**
The Counter is reset if both SBOccLP and SBOccHP are equal 0.
Note: The LSBs SBOccLPd(1:0) are mapped to transfer register SBOC0.

Register 46 SBOC2
SBOC Transfer Register 2

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **SBOC1** **$4B_H$**

Typical Usage: Read by CPU (for debug purposes or statistics)

Bit	15	14	13	12	11	10	9	8
	SBOccLP(17:10)							

Bit	7	6	5	4	3	2	1	0
	SBOccLP(9:2)							

SBOccLP(17:2) **Scheduler Block Occupancy Counter Low Priority**

Note: The LSBs SBOccLP(1:0) are mapped to transfer register SBOC0.

Register 47 SBOC3
SBOC Transfer Register 3

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **SBOC3** **$4C_H$**

Typical Usage: Read by CPU (for debug purposes or statistics)

Bit	15	14	13	12	11	10	9	8
	SBOccHP(17:10)							

Bit	7	6	5	4	3	2	1	0
	SBOccHP(9:2)							

SBOccHP(17:2) **Scheduler Block Occupancy Counter High Priority**

Note: The LSBs SBOccHP(1:0) are mapped to transfer register SBOC0.

Register 48 SBOC4
SBOC Transfer Register 4

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**SBOC4** **$4D_H$**
Typical Usage:	Read by CPU (for debug purposes or statistics)

Bit	15	14	13	12	11	10	9	8
	SBOccNg(17:10)							

Bit	7	6	5	4	3	2	1	0
	SBOccNg(9:2)							

SBOccNg(17:2) **Scheduler Block Occupancy Counter Non Guaranteed**

Note: The LSBs SBOccNg(1:0) are mapped to transfer register SBOC0.

7.2.12 Merge Group Table Transfer Registers

Internal Table 5: Merge Group Table Transfer Registers MGT0..MGT2

The Merge Group Table Transfer Registers are used to access the internal Merge Group Table (MGT) containing 2*128 entries of 48 bit each. **Table 7-10** shows an overview of the registers involved.

Table 7-12 Registers for MGT Table Access

47 … 0				
MGT RAM entry				RAM Select:
15 … 0	15 … 0	15 … 0		15 … 0
MGT2	MGT1	MGT0		$MAR=07_H$
				Entry select:
15 … 0	15 … 0	15 … 0		15 … 0
MASK2	MASK1	MASK0		$WAR (0..255_D)$

MGT0..MGT2 are the transfer registers for one 48-bit MGT table entry. The Scheduler Block number representing the table entry which needs to be read or written must be written to the Word Address Register (WAR). The dedicated MGT table entry is read into the MGT0..MGT2 Registers or modified by the MGT0..MGT2 register values with a write mechanism. The associated Mask Registers MASK0..MASK2 allow a bit-wise Write operation (0 - unmasked, 1 - masked). In case of read operation, the dedicated MGT0..MGT2 register bit will be overwritten by the respective MGT table entry bit value. In case of Write operation, the dedicated MGT0..MGT2 register bit will modify the respective MGT table entry bit value.

The Read or Write process is controlled by the Memory Address Register (MAR). The 5 LSBs (= Bit 4..0) of the MAR register select the memory/table that will be accessed; to select the MGT table, bit field MAR(4:0) must be set to 6. Bit 5 of MAR starts the transfer and is automatically cleared after execution.

Table 7-13 WAR Register Mapping for MGT Table Access

Bit	15	14	13	12	11	10	9	8
	Unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	CoreSel	GroupSel(6:0)						

CoreSel **Selects an ABM-3G core**:

0	Upstream core selected
1	Downstream core selected

GroupSel(6:0) **Selects one of the 128 Merge Groups**.

Register 49 MGT0
MGT Transfer Register 0

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **MGT0** **$4E_H$**
Typical Usage: Not used by CPU

Bit	15	14	13	12	11	10	9	8
	Reserved(15:8)							

Bit	7	6	5	4	3	2	1	0
	Reserved(7:0)							

Reserved(15:0)

Register 50 MGT1

MGT Transfer Register 1

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **MGT1** **$4F_H$**

Typical Usage: Not used by CPU

Bit	15	14	13	12	11	10	9	8
	Reserved(15:13)			Head_Pointer(12:8)				

Bit	7	6	5	4	3	2	1	0
	Head_Pointer(7:0)							

Reserved(15:13)

Head_Pointer(12:0) When setting up a merge group, this pointer must be set to point to any of the queues contained in the merge group.

Register 51 MGT2
MGT Transfer Register 2

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **MGT2** **50_H**

Typical Usage: Written by CPU to maintain the MGT table

Bit	15	14	13	12	11	10	9	8
	unused	LCIOen	LCI(13:8)					

Bit	7	6	5	4	3	2	1	0
	LCI(7:0)							

LCIOen **LCI Overwrite Enable**:

This bit enables the LCI overwrite function for cells/packets emitted by the VC-Merge Group.

0 Disable LCI overwrite

1 Enable LCI overwrite

LCI(13:0) **LCI**

In case LCI overwrite function is enabled, this value overwrites the original LCI of any cell emitted by this VC-Merge Group.
The cell field that is overwritten depends on the selected LCI mapping mode.

7.2.13 Mask Registers

Register 52 MASK0/MASK1
Table Access Mask Registers 0/1

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **MASK0 55_H** **MASK1 56_H**
Typical Usage: Written by CPU to control internal table Read/Write access

Bit	15	14	13	12	11	10	9	8
	MASK(15:8)							

Bit	7	6	5	4	3	2	1	0
	MASK(7:0)							

MASK0(15:0) **Mask Register 0**

MASK1(15:0) **Mask Register 1**

Mask Registers 0..6 control the Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers (LCI0..LCI2, TCT0..TCT3, QCT0..6, SBOC0..SBOC4, MGT0..MGT2):

0 The dedicated bit of the transfer register overwrites the table entry during Write.
Does not affect Read access.

1 The dedicated bit of the transfer register does *not* overwrite the table entry during Write.
Does not affect Read access.

Register 53 MASK2/MASK3
Table Access Mask Registers 2/3

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **MASK2** **57_H** **MASK3** **58_H**
Typical Usage: Written by CPU to control internal table Read/Write access

Bit	15	14	13	12	11	10	9	8
	MASK(15:8)							

Bit	7	6	5	4	3	2	1	0
	MASK(7:0)							

MASK2(15:0) **Mask Register 2**
MASK3(15:0) **Mask Register 3**

Mask Registers 0..6 control the Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers (LCI0..LCI2, TCT0..TCT3, QCT0..6, SBOC0..SBOC4, MGT0..MGT2):

0 The dedicated bit of the transfer register overwrites the table entry during Write.
Does not affect Read access.

1 The dedicated bit of the transfer register does *not* overwrite the table entry during Write.
Does not affect Read access.

Register 54 MASK4/MASK5

Table Access Mask Registers 4/5

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**MASK4** **59_H** **MASK5** **$5A_H$**
Typical Usage:	Written by CPU to control internal table Read/Write access

Bit	15	14	13	12	11	10	9	8
	MASK(15:8)							

Bit	7	6	5	4	3	2	1	0
	MASK(7:0)							

MASK4(15:0) **Mask Register 4**

MASK5(15:0) **Mask Register 5**

Mask Registers 0..6 control the Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers (LCI0..LCI2, TCT0..TCT3, QCT0..6, SBOC0..SBOC4, MGT0..MGT2):

0	The dedicated bit of the transfer register overwrites the table entry during Write. Does not affect Read access.
1	The dedicated bit of the transfer register does *not* overwrite the table entry during Write. Does not affect Read access.

Register 55 MASK6
Table Access Mask Registers 6

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **MASK6** **$5B_H$**
Typical Usage: Written by CPU to control internal table Read/Write access

Bit	15	14	13	12	11	10	9	8
	MASK(15:8)							

Bit	7	6	5	4	3	2	1	0
	MASK(7:0)							

MASK6(15:0) **Mask Register 6**

Mask Registers 0..6 control the Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers (LCI0..LCI2, TCT0..TCT3, QCT0..6, SBOC0..SBOC4, MGT0..MGT2):

0 The dedicated bit of the transfer register overwrites the table entry during Write.
Does not affect Read access.

1 The dedicated bit of the transfer register does *not* overwrite the table entry during Write.
Does not affect Read access.

7.2.14 Rate Shaper CDV Registers

Register 56 UCDV/DCDV
Upstream/Downstream Rate Shaper CDV Registers

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**UCDV**	**62_H**	**DCDV**	**82_H**
Typical Usage:	Written by CPU			

Bit	15	14	13	12	11	10	9	8
	Unused(6:0)							CDV Max(8)

Bit	7	6	5	4	3	2	1	0
	CDVMax(7:0)							

CDVMax(8:0) Maximal Cell Delay Variation (without notice)

This bit field determines a maximum CDV value for peak rate limited queues that can be introduced without notice.

The CDVMax is measured in multiples of 16-cell cycles.

If this maximum CDV is exceeded, a CDVOV (see registers ISRU/ISRD) interrupt is generated to indicate an unexpected CDV value. This can occur if multiple peak rate limited queues are scheduled to emit a cell in the same Scheduler time slot.

No cells are discarded due to this event.

7.2.15 Queue Parameter Table Mask Registers

Register 57 UQPTM0/DQPTM0
Upstream/Downstream Queue Parameter Table Mask Registers 0

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**UQPTM0**	**65_H**	**DQPTM0**	**85_H**
Typical Usage:	Written by CPU to control internal table Read/Write access			

Bit	15	14	13	12	11	10	9	8
	xQPTM0(15:8)							

Bit	7	6	5	4	3	2	1	0
	xQPTM0(7:0)							

UQPTM0(15:0) **Upstream QPT Mask Register 0**

DQPTM0(15:0) **Downstream QPT Mask Register 0**

UQPTM0/DQPTM0 control the Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers (UQPT1T0/UQPT2T0, DQPT1T0/DQPT2T0):

0 The dedicated bit of the transfer register overwrites the table entry during Write.
Does not affect Read access.

1 The dedicated bit of the transfer register does *not* overwrite the table entry during Write.
Does not affect Read access.

Register 58 UQPTM1/DQPTM1
Upstream/Downstream Queue Parameter Table Mask Registers 1

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**UQPTM1**	**66_H**	**DQPTM1**	**86_H**
Typical Usage:	Written by CPU to control internal table Read/Write access			

Bit	15	14	13	12	11	10	9	8
	xQPTM1(15:8)							

Bit	7	6	5	4	3	2	1	0
	xQPTM1(7:0)							

UQPTM1(15:0) **Upstream QPT Mask Register 1**

DQPTM1(15:0) **Downstream QPT Mask Register 1**

UQPTM1/DQPTM1 control the Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers (UQPT1T1/UQPT2T1, DQPT1T1/DQPT2T1):

0 The dedicated bit of the transfer register overwrites the table entry during Write.
Does not affect Read access.

1 The dedicated bit of the transfer register does *not* overwrite the table entry during Write.
Does not affect Read access.

Register 59 UQPTM2/DQPTM2
Upstream/Downstream Queue Parameter Table Mask Registers 2

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**UQPTM2**	**67_H**	**DQPTM2**	**87_H**
Typical Usage:	Written by CPU to control internal table Read/Write access			

Bit	15	14	13	12	11	10	9	8
	xQPTM2(15:8)							

Bit	7	6	5	4	3	2	1	0
	xQPTM2(7:0)							

UQPTM2(15:0) **Upstream QPT Mask Register 2**

DQPTM2(15:0) **Downstream QPT Mask Register 2**

UQPTM2/DQPTM2 control the Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers (UQPT2T2, DQPT2T2):

0 The dedicated bit of the transfer register overwrites the table entry during Write.
Does not affect Read access.

1 The dedicated bit of the transfer register does *not* overwrite the table entry during Write.
Does not affect Read access.

Register 60 UQPTM3/DQPTM3
Upstream/Downstream Queue Parameter Table Mask Registers 3

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**UQPTM3** **68_H** **DQPTM3** **88_H**
Typical Usage:	Written by CPU to control internal table Read/Write access

Bit	15	14	13	12	11	10	9	8
	xQPTM3(15:8)							

Bit	7	6	5	4	3	2	1	0
	xQPTM3(7:0)							

UQPTM3(15:0) **Upstream QPT Mask Register 3**

DQPTM3(15:0) **Downstream QPT Mask Register 3**

UQPTM3/DQPTM3 control the Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers (UQPT2T3, DQPT2T3):

0	The dedicated bit of the transfer register overwrites the table entry during Write. Does not affect Read access.
1	The dedicated bit of the transfer register does *not* overwrite the table entry during Write. Does not affect Read access.

Register 61 UQPTM4/DQPTM4
Upstream/Downstream Queue Parameter Table Mask Registers 4

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **UQPTM4** **69_H** **DQPTM4** **89_H**
Typical Usage: Not used for user-accessible tables.

Bit	15	14	13	12	11	10	9	8
	xQPTM4(15:8)							

Bit	7	6	5	4	3	2	1	0
	xQPTM4(7:0)							

UQPTM4(15:0) **Upstream QPT Mask Register 4**
DQPTM4(15:0) **Downstream QPT Mask Register 4**

UQPTM4/DQPTM4 control the Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers:

0 The dedicated bit of the transfer register overwrites the table entry during Write.
Does not affect Read access.

1 The dedicated bit of the transfer register does *not* overwrite the table entry during Write.
Does not affect Read access.

Register 62 UQPTM5/DQPTM5
Upstream/Downstream Queue Parameter Table Mask Registers 5

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **UQPTM5 $6A_H$** **DQPTM5 $8A_H$**

Typical Usage: Not used for user-accessible tables.

Bit	15	14	13	12	11	10	9	8
	xQPTM5(15:8)							

Bit	7	6	5	4	3	2	1	0
	xQPTM5(7:0)							

UQPTM5(15:0) **Upstream QPT Mask Register 5**

DQPTM5(15:0) **Downstream QPT Mask Register 5**

UQPTM5/DQPTM5 control the Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers:

0 The dedicated bit of the transfer register overwrites the table entry during Write.
Does not affect Read access.

1 The dedicated bit of the transfer register does *not* overwrite the table entry during Write.
Does not affect Read access.

7.2.16 Scheduler Configuration Register

Register 63 USCONF/DSCONF
Upstream/Downstream Scheduler Configuration Registers

CPU Accessibility:	**Read/Write**
Reset Value:	**0004_H**
Offset Address:	**USCONF** **$6B_H$** **DSCONF** **$8B_H$**
Typical Usage:	Written by CPU during global initialization

Bit	15	14	13	12	11	10	9	8
	unused(12:5)							

Bit	7	6	5	4	3	2	1	0
	unused(4:0)					TstepC(2:0)		

TstepC(2:0) **Time Base for the Rate Shaper**
Refer to **Section 4.2.2.5 “Programming the PCR Limiter” on Page 109**

7.2.17 Queue Parameter Table Transfer Registers

Internal Table 6: Queue Parameter Table 1 Transfer Registers

Queue Parameter Table Transfer Registers are used to access the internal Upstream and Downstream Queue Parameter Table 1 (QPT1) containing 8192 entries each. In both **Table 7-14** and **Table 7-15** provide an overview of the registers involved. Each QPT1 entry consists of 32 bits.

Note: The QPT1 table information is not used by the CPU beside during queue initialization.

Table 7-14 Registers for QPT1 Upstream Table Access

31	0		RAM Select:
QPT1 RAM entry (**Up**stream)			15 0
15 0	15 0		$MAR=10_H$
UQPT1T1	UQPT1T0		Entry Select:
15 0	15 0		15 0
UQPTM1	UQPTM0		WAR ($0..8191_D$)

Table 7-15 Registers for QPT1 Downstream Table Access

31	0		RAM Select:
QPT1 RAM entry (**Down**stream)			15 0
15 0	15 0		$MAR=18_H$
DQPT1T1	DQPT1T0		Entry Select:
15 0	15 0		15 0
DQPTM1	DQPTM0		WAR ($0..8191_D$)

UQPT1T0 and UQPT1T1 are the transfer registers for the 32-bit entry of the upstream QPT1 table. DQPT1T0 and DQPT1T1 are the transfer registers for the 32-bit entry of the downstream QPT1 table. Access to high and low word are both controlled by mask registers UQPTM0/UQPTM1 and DQPTM0/DQPTM1 respectively. The Mask registers are shared for access to both tables QPT1 and QPT2, whereas, the transfer registers are unique for each table.

The queue number representing the table entry which needs to be read or written must be written to the Word Address Register (WAR). The dedicated QPT1 table entry is read into the xQPT1T0/xQPT1T1 transfer registers (x=U,D) or modified by the xQPT1T0/xQPT1T1 transfer register values with a write mechanism. The associated mask registers xQPTM0 and xQPTM1 allow a bit-wise Write operation (0 - unmasked, 1 - masked). In case of Read operation, the dedicated xQPT1T0/xQPT1T1 register bit will be overwritten by the respective QPT1 table entry bit value. In case of Write operation, the dedicated xQPT1T0/xQPT1T1 register bit will modify the respective QPT1 table entry bit value.

The Read or Write process is controlled by the Memory Address Register (MAR). The 5 LSBs (= Bit 4..0) of the MAR register select the memory/table that will be accessed; to select the QPT table bit field MAR(4:0) must be set to:

10_H for QPT1 upstream table,

18_H for QPT1 downstream table.

Bit 5 of MAR starts the transfer and is cleared automatically after execution.

Table 7-16 WAR Register Mapping for QPT Table Access

Bit	15	14	13	12	11	10	9	8
	Unused(2:0)			QueueSel(12:8)				

Bit	7	6	5	4	3	2	1	0
	QueueSel(7:0)							

QueueSel(12:0) Selects one of the 8192 queue parameter table entries.

Register 64 UQPT1T0/DQPT1T0
Upstream/Downstream QPT1 Table Transfer Register 0

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**UQPT1T0**	**70_H**	**DQPT1T0**	**90_H**
Typical Usage:	Written by CPU during queue initialization			

Bit	15	14	13	12	11	10	9	8
	Reserved(13:6)							

Bit	7	6	5	4	3	2	1	0
	Reserved(5:0)						flags(1:0)	

Reserved(13:0) These bits are used by the device logic. Do not Write to this field as that could lead to complete malfunctioning of the ABM-3G which can be corrected by chip reset only.

flags(1:0) These bits must be written to 0 when initializing the queue. Do not Write during normal operation.

Register 65 UQPT1T1/DQPT1T1
Upstream/Downstream QPT1 Table Transfer Register 1

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000$_H$**			
Offset Address:	**UQPT1T1**	**71$_H$**	**DQPT1T0**	**91$_H$**
Typical Usage:	Not used by CPU			

Bit	15	14	13	12	11	10	9	8
	Reserved(15:8)							

Bit	7	6	5	4	3	2	1	0
	Reserved(7:0)							

Reserved(15:0) These bits are used by the device logic. Do not Write to this field as that could lead to complete malfunctioning of the ABM-3G which can be corrected by chip reset only.

Internal Table 7: Queue Parameter Table 2 Transfer Registers

Queue Parameter Table Transfer Registers are used to access the internal Upstream and Downstream Queue Parameter Table 2 (QPT2) containing 8192 entries each. In both **Table 7-17** and **Table 7-18** provide an overview of the registers involved. Each QPT2 entry consists of 64 bits.

Table 7-17 Registers for QPT2 Upstream Table Access

63			0	
QPT2 RAM entry (**Up**stream)				RAM Select:
15 0	15 0	15 0	15 0	15 0
UQPT2T3	UQPT2T2	UQPT2T1	UQPT2T0	MAR=11_H
				Entry Select:
15 0	15 0	15 0	15 0	15 0
UQPTM3	UQPTM2	UQPTM1	UQPTM0	WAR (0..8191_D)

Table 7-18 Registers for QPT2 Downstream Table Access

63			0	
QPT2 RAM entry (**Down**stream)				RAM Select:
15 0	15 0	15 0	15 0	15 0
DQPT2T3	DQPT2T2	DQPT2T1	DQPT2T0	MAR=19_H
				Entry Select:
15 0	15 0	15 0	15 0	15 0
DQPTM3	DQPTM2	DQPTM1	DQPTM0	WAR (0..8191_D)

UQPT2T0..UQPT2T3 are the transfer registers for the 64-bit entry of the upstream QPT2 table. DQPT2T0..DQPT2T3 are the transfer registers for the 64-bit entry of the downstream QPT2 table. Access to the RAM entry is controlled by mask registers UQPTM0..UQPTM3 and DQPTM0..DQPTM3, respectively. The Mask registers are shared for access to both tables QPT1 and QPT2 whereas the transfer registers are unique for each table.

The queue number representing the table entry which needs to be read or written must be written to the Word Address Register (WAR). The dedicated QPT2 table entry is read into the xQPT2T0..xQPT2T3 transfer registers (x=U,D) or modified by the xQPT2T0..xQPT2T3 transfer register values with a write mechanism. The associated mask registers xQPTM0..xQPTM3 allow a bit-wise Write operation (0 - unmasked, 1 -

masked). In case of Read operation, the dedicated xQPT2T0..xQPT2T3 register bit will be overwritten by the respective QPT1 table entry bit value. In case of Write operation, the dedicated xQPT2T0..xQPT2T3 register bit will modify the respective QPT1 table entry bit value.

The Read or Write process is controlled by the Memory Address Register (MAR). The 5 LSBs (= Bit 4..0) of the MAR register select the memory/table that will be accessed; to select the QPT table bit field MAR(4:0) must be set to:

11_H for QPT2 upstream table,

19_H for QPT2 downstream table.

Bit 5 of MAR starts the transfer and is cleared automatically after execution.

Table 7-19 WAR Register Mapping for QPT Table Access

Bit	15	14	13	12	11	10	9	8
	Unused(2:0)			QueueSel(12:8)				

Bit	7	6	5	4	3	2	1	0
	QueueSel(7:0)							

QueueSel(12:0) Selects one of the 8192 queue parameter table entries.

Register 66 UQPT2T0/DQPT2T0
Upstream/Downstream QPT2 Table Transfer Register 0

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **UQPT2T0 72_H** **DQPT2T0 92_H**
Typical Usage: Written by CPU during queue initialization

Bit	15	14	13	12	11	10	9	8
	RateFactor(15:8)							

Bit	7	6	5	4	3	2	1	0
	RateFactor(7:0)							

RateFactor(15:0) Controls the Peak Cell Rate of the queue. It is identical to the Rate factor TP described in **Section 4.2.2.5 "Programming the PCR Limiter" on Page 109**. The value 0 disables the PCR limiter, that is, the cells from this queue bypass the shaper circuit.
For VBR shaping, this parameter is not used (overridden by the parameter TP of the AVT table). However, it must be set unequal to 0 to enable VBR shaping.

Register 67 UQPT2T1/DQPT2T1
Upstream/Downstream QPT2 Table Transfer Register 1

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**UQPT2T1**	**73_H**	**DQPT2T1**	**93_H**
Typical Usage:	Written by CPU during queue initialization			

Bit	15	14	13	12	11	10	9	8
	Unused(1:0)		WFQFactor(13:8)					

Bit	7	6	5	4	3	2	1	0
	WFQFactor(7:0)							

WFQFactor (13:0)

Determines the weight factor T_{WFQ} of the queue at the WFQ scheduler input to which it is connected. Refer to **Section 4.2.2.7 "Guaranteed Cell Rates and WFQ Weight Factors" on Page 114**.
The value WFQ Factor = 0 connects the queue to the high priority Round Robin Scheduler.
The value WFQFactor = 16383 (all ones) connects the queue to the low priority Round Robin Scheduler.

Modifying the WFQFactor during operation:
- If one of the Round Robin Schedulers (WFQFactor=0 or WFQFactor=16383) is used the WFQFactor must not be changed
- If the WFQ Scheduler (WFQFactor=1..16320) is used the WFQ-Factor may be varied in a range 1 to 16320.

Register 68 UQPT2T2/DQPT2T2
Upstream/Downstream QPT2 Table Transfer Register 2

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **UQPT2T2 74_H** **DQPT2T2 94_H**
Typical Usage: Not used by CPU

Bit	15	14	13	12	11	10	9	8
	Reserved(15:8)							

Bit	7	6	5	4	3	2	1	0
	Reserved(7:0)							

Reserved(15:0) These bits are used by the device logic. Do not Write to this field as that could lead to complete malfunctioning of the ABM-3G, which can be corrected by chip reset only.

Register 69 UQPT2T3/DQPT2T3
Upstream/Downstream QPT2 Table Transfer Register 3

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **UQPT2T3 75_H** **DQPT2T3 95_H**
Typical Usage: Not used by CPU

Bit	15	14	13	12	11	10	9	8
	Reserved(15:8)							

Bit	7	6	5	4	3	2	1	0
	Reserved(7:0)							

Reserved(15:0) These bits are used by the device logic. Do not Write to this field as that could lead to complete malfunctioning of the ABM-3G, which can be corrected by chip reset only.

7.2.18 Scheduler Block Configuration Table Transfer/Mask Registers SDRAM Refresh Registers UTOPIA Port Select of Common Real Time Queue Registers

Internal Table 8: Scheduler Configuration Table Integer Transfer Registers

The Scheduler Configuration Table Integer Transfer Registers are used to access the internal Upstream/Downstream Scheduler Configuration Tables Integer Part (SCTI) containing 128 entries each.

These tables are not addressed by the MAR and WAR registers, but are addressed via dedicated address registers (USADR/DSADR) and data registers (USCTI/DSCTI).

Table 7-20 and **Table 7-21** show an overview of the registers involved.

Table 7-20 Registers SCTI Upstream Table Access

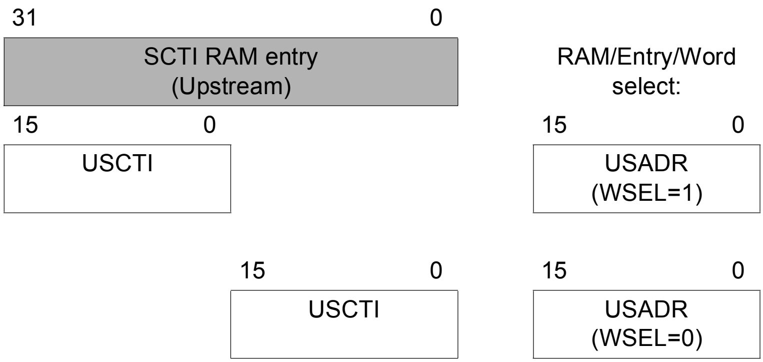
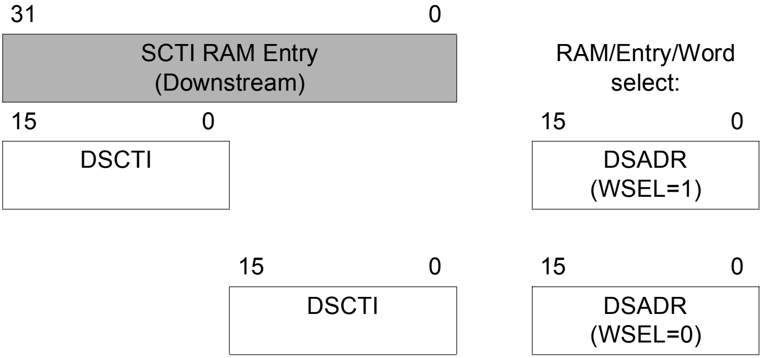


Table 7-21 Registers SCTI Downstream Table Access



USCTI and DSCTI are the transfer registers for the 32-bit SCTI upstream/downstream table entries. The upstream and downstream Schedulers use different tables (internal RAM) addressed via dedicated registers, USADR/DSADR. The address registers select the scheduler-specific entry as well as the high or low word of a 32-bit entry to be accessed. Further, there is no command bit, but transfers are triggered via Write access of the address registers and the data registers:

- To initiate a Read access, the Scheduler Block number must be written to the address register USADR (upstream) or to the address register DSADR (downstream). One system clock cycle later, the data can be Read from the respective transfer register USCTI or DSCTI.
- To initiate a Write access, it is sufficient to Write the desired Scheduler Block number to the address registers, USADR and DSADR, and then Write the desired data to the respective transfer register, USCTI or DSCTI, respectively. The transfer to the integer table is executed one system clock cycle after the Write access to USCTI or DSCTI. Thus, consecutive Write cycles may be executed by the microprocessor.

The SCTI table entries are either read or written. Thus, no additional mask registers are provided for bit-wise control of table entry accesses.

Register 70 USADR/DSADR
Upstream/Downstream SCTI Address Registers

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**USADR**	**$A0_H$**	**DSADR**	**$B8_H$**
Typical Usage:	Written and Read by CPU to maintain the SCTI tables			

Bit	15	14	13	12	11	10	9	8
	unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	WSel	SchedNo(6:0)						

WSel SCTI table entry **Word Select**

1	Selects the high word (bit 31..16) for next access via register SCTIU/SCTID
0	Selects the low word (bit 15..0) for next access via register SCTIU/SCTID

SchedNo(6:0) **Scheduler Block Number**
Selects one of the 128 core-specific Scheduler Blocks for next access via register USCTI/DSCTI.

Register 71 USCTI/DSCTI
Upstream/Downstream SCTI Transfer Registers

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **USCTI** **$A1_H$** **DSCTI** **$B9_H$**
Typical Usage: Written by CPU to maintain the SCTI tables

Register SADRx.WSel = 0:

Bit	15	14	13	12	11	10	9	8
	unused(1:0)		IntRate(13:8)					

Bit	7	6	5	4	3	2	1	0
	IntRate(7:0)							

IntRate(13:0) **Integer Rate**
This value determines the integer part of the Scheduler Block output rate.

Note: Recommendation for changing the UTOPIA port number or scheduler rate during operation:
Disable specific scheduler by read-modify-write operation to corresponding bit in registers USCEN0/DSCEN0... USCEN7/DSCEN7.
Modify scheduler specific UTOPIA port number and rates via ***Table 8 "Scheduler Configuration Table Integer Transfer Registers" on Page 257****, registers USCTI/DSCTI and* ***Table 9 "Scheduler Configuration Table Fractional Transfer Registers" on Page 267****, registers USCTFT/DSCTFT.*
Enable specific scheduler by read-modify-write operation to corresponding bit in registers USCEN0/DSCEN0... USCEN7/DSCEN7.

Note: Read access to bit field IntRate(13:0) is not supported and will return undefined values.

Refer to **Section 4.2.2.2 "Programming the Scheduler Block Rates" on Page 106** for the calculation of IntRate and FracRate

Register SADRx.WSel = 1:

Bit	15	14	13	12	11	10	9	8
	Init(9:2)							

Bit	7	6	5	4	3	2	1	0
	Init(1:0)		UTOPIAPort(5:0)					

Init(9:0) **Initialization Value**
It is recommended to Write this bit field to all 0s during Scheduler Block configuration/initialization (the note below provides the details).

UTOPIAPort(5:0) **UTOPIA Port Number**
Specifies one of the 48 UTOPIA ports to which the Scheduler Block is assigned to. Only values in the range 0..47_D are valid (0..3 for UTOPIA level 1). The UTOPIA port number value can be changed during operation (see note below). UTOPIA Port 48_D is used to select the AAL5 reassembly unit.

The UTOPIA port number can be modified during operation; (port) switch-over is e.g. used for ATM protection switching. The following Notes explain switch-over and rate adaptation during operation:

Note: This SCTI table entry should be programmed during Scheduler Block configuration/initialization. However the UTOPIA port number value can be modified during operation (e.g. for port switching). In this case the Init(9:0) value can be reset to 0. This bit field contains a 4-bit counter incrementing the number of unused scheduler cell cycles. Unused cell cycles occur whenever a scheduled event cannot be served, because a previously generated event is still in service (active cell transfer at UTOPIA Interface). This counter value is used (and decremented accordingly) to determine the allowed cell burst size for following scheduler events. Such bursts are treated as 'one event' to allow a near 100% scheduler rate utilization. The maximum burst size is programmed in registers UECRI/DECRI on page 7-263.

Thus, overwriting bit field Init(9:0) with 0 during operation may invalidate some stored cell cycles, only if maximum burst size is programmed >1 for this port.

Only saved scheduler cell cycles can get lost; in no way can stored cells be lost or discarded by these operations.

To minimize even this small impact, value Init(9:0) can be read and written back with the new UTOPIA port number.

Note: Recommendation for changing the UTOPIA port number or scheduler rate during operation:

Disable specific scheduler by read-modify-write operation to corresponding bit in registers USCEN0/DSCEN0... USCEN7/DSCEN7.

Modify scheduler specific UTOPIA port number and rates via ***Table 8 "Scheduler Configuration Table Integer Transfer Registers" on Page 257****, registers USCTI/DSCTI and* ***Table 9 "Scheduler Configuration Table Fractional Transfer Registers" on Page 267****, registers USCTFT/DSCTFT.*

Enable specific scheduler by read-modify-write operation to corresponding bit in registers USCEN0/DSCEN0... USCEN7/DSCEN7.

Register 72 UECRI/DECRI
Upstream/Downstream Empty Cycle Rate Integer Part Registers

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**UECRI**	**$A2_H$**	**DECRI**	**BA_H**
Typical Usage:	Written by CPU for global Scheduler configuration			

Bit	15	14	13	12	11	10	9	8
	MaxBurstS(3:0)				Unused(1:0)		ECIntRate(9:8)	

Bit	7	6	5	4	3	2	1	0
	ECIntRate(7:0)							

MaxBurstS(3:0) **Maximum Burst size for a Scheduler Block**
Refer to **Section 4.2.2.2 “Programming the Scheduler Block Rates” on Page 106**

ECIntRate(9:0) **Integer part of Empty Cycle Rate**
The empty cycles are required by internal logic to perform the refresh cycles of the SDRAMS.
Minimum value is 10_H and should be programmed during configuration.

Refer to **Section 4.2.2.4 “Programming the SDRAM Refresh Empty Cell Cycles” on Page 109** for the calculation of ECIntRate and ECFracRate

Register 73 UECRF/DECRF
Upstream/Downstream Empty Cycle Rate Fractional Part Registers

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**UECRF** **$A3_H$** **DECRF** **BB_H**
Typical Usage:	Written by CPU for global Scheduler configuration

Bit	15	14	13	12	11	10	9	8
	Unused(7:0)							

Bit	7	6	5	4	3	2	1	0
	ECFracRate(7:0)							

ECFracRate(7:0)	**Fractional part of Empty Cycle Rate** The empty cycles are required by internal logic to perform the refresh cycles of the SDRAMS. Recommended value is 00_H and should be programmed during configuration.

Refer to **Section 4.2.2.4 "Programming the SDRAM Refresh Empty Cell Cycles" on Page 109** for the calculation of ECIntRate and ECFracRate

Register 74 UCRTQ/DCRTQ

Upstream/Downstream Common Real Time Queue UTOPIA Port Select Registers

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**UCRTQ**	**$A4_H$**	**DCRTQ**	**BC_H**
Typical Usage:	Written by CPU for global Scheduler configuration			

Bit	15	14	13	12	11	10	9	8
	Unused(9:2)							

Bit	7	6	5	4	3	2	1	0
	Unused(1:0)		CrtqUTOPIA(5:0)					

CtrqUTOPIA(5:0) Common Real Time Queue UTOPIA Port Number.
Specifies one of the 48 UTOPIA ports to which the common real time queue is assigned. Only values in the range $0..47_D$ are valid.

Register 75 USCTFM/DSCTFM
Upstream/Downstream SCTF Mask Registers

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**USCTFM** **$A5_H$** **DSCTFM** **BD_H**
Typical Usage:	Written by CPU to control internal table Read/Write access

Bit	15	14	13	12	11	10	9	8
	SCTFM(15:8)							

Bit	7	6	5	4	3	2	1	0
	SCTFM(7:0)							

USCTFM(15:0) **Upstream SCTF Mask Register**

DSCTFM(15:0) **Downstream SCTF Mask Register**

USCTFM and DSCTFM control the Read or Write access from the respective transfer registers to the internal tables on a per-bit selection basis. The mask registers correspond to the respective transfer registers (USCTFT, DSCTFT):

0 The dedicated bit of the transfer register is *not* overwritten by the corresponding table entry bit during Read, but overwrites the table entry bit during the Write. This is a Write access to the internal table entry.

1 The dedicated bit of the transfer register is overwritten by the corresponding table entry bit during Read and is written back to the table entry bit during Write.
This is a Read access to the internal table entry.

Internal Table 9: Scheduler Configuration Table Fractional Transfer Registers

The Scheduler Configuration Table Fractional Transfer Registers are used to access the internal Upstream/Downstream Scheduler Configuration Tables Fractional Part (SCTF) containing 128 entries each. **Table 7-22** and **Table 7-23** summarize the registers.

Table 7-22 Registers SCTF Upstream Table Access

15 … 0		15 … 0
SCTF RAM Entry (Upstream)		RAM Select:
USCTFT		$MAR=17_H$
		Entry Select:
USCTFM		$WAR (0..127_D)$

Table 7-23 Registers SCTF Downstream Table Access

15 … 0		15 … 0
SCTF RAM Entry (Downstream)		RAM Select:
DSCTFT		$MAR=1F_H$
		Entry Select:
DSCTFM		$WAR (0..127_D)$

SCTFU and SCTFD are transfer registers for one 16-bit SCTF upstream/downstream table entry. The upstream and downstream Scheduler Blocks use different tables (internal RAM) addressed via the MAR. The Scheduler Block number representing the table entry which needs to be read or written must be written to the WAR (Word Address Register). The dedicated SCTFU/D table entry is read into the SCTFU/D registers or modified by the SCTFU/D register value with a write mechanism. The associated mask registers, SMSKU and SMSKD, allow a bit-wise Write operation (0 - unmasked, 1 - masked). In case of Read operation, the dedicated SCTFU/D register bit will be overwritten by the respective SCTFU/D table entry bit value. In case of Write operation, the dedicated SCTFU/D register bit will modify the value of the respective SCTFU/D table entry bit.

The Read or Write process is controlled by the MAR (Memory Address Register). The 5 LSBs (= Bit 4..0) of the MAR register select the memory/table that will be accessed; to select the SCTF Upstream table, bit field MAR(4:0) must be set to 17_H and $1F_H$ for the SCTF Downstream table respectively. Bit 5 of MAR starts the transfer and is automatically cleared after execution.

Table 7-24 WAR Register Mapping for SCTFU/SCTFD Table access

Bit	15	14	13	12	11	10	9	8
	Unused(9:2)							

Bit	7	6	5	4	3	2	1	0
	unused	SchedSel(6:0)						

SchedSel(6:0) Selects one of the 128 core specific Scheduler Blocks.

Register 76 USCTFT/DSCTFT
Upstream/Downstream SCTF Transfer Registers

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**USCTFT**	**$A6_H$**	**DSCTFT**	**BE_H**
Typical Usage:	Written and Read by CPU to maintain the SCTF tables			

Bit	15	14	13	12	11	10	9	8
	Init(7:0)							

Bit	7	6	5	4	3	2	1	0
	FracRate(7:0)							

Init(7:0) **Scheduler Block Initialization Value**
This bit field must be written to 00_H at the time of Scheduler configuration/initialization and should not be written during normal operation.

FracRate(7:0) **Fractional Rate**
This value determines the fractional part of the Scheduler Block output rate. Refer to **Section 4.2.2.2 "Programming the Scheduler Block Rates" on Page 106** for the calculation of FracRate

Note: Recommendation for changing the UTOPIA port number or scheduler rate during operation:
Disable specific scheduler by read-modify-write operation to corresponding bit in registers USCEN0/DSCEN0... USCEN7/DSCEN7.
*Modify scheduler specific UTOPIA port number and rates via **Table 8 "Scheduler Configuration Table Integer Transfer Registers" on Page 257**, registers USCTI/DSCTI and **Table 9 "Scheduler Configuration Table Fractional Transfer Registers" on Page 267**, registers USCTFT/DSCTFT.*
Enable specific scheduler by read-modify-write operation to corresponding bit in registers USCEN0/DSCEN0... USCEN7/DSCEN7.

7.2.19 Scheduler Block Enable Registers

Register 77 USCEN0/DSCEN0
Upstream/Downstream Scheduler Block Enable 0 Registers

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**USCEN0**	**$A8_H$**	**DSCEN0**	**$C0_H$**
Typical Usage:	Written by CPU for global Scheduler configuration			

Bit	15	14	13	12	11	10	9	8
	SchedEn(15:8)							

Bit	7	6	5	4	3	2	1	0
	SchedEn(7:0)							

SchedEn(15:0) **Scheduler Block Enable**
Each bit position enables/disables the respective Scheduler Block (15..0):

1	Scheduler Block enabled
0	Scheduler Block disabled

Register 78 USCEN1/DSCEN1
Upstream/Downstream Scheduler Block Enable 1 Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **USCEN0** **$A9_H$** **DSCEN0** **$C1_H$**

Typical Usage: Written by CPU for global Scheduler configuration

Bit	15	14	13	12	11	10	9	8
	SchedEn(31:24)							

Bit	7	6	5	4	3	2	1	0
	SchedEn(23:16)							

SchedEn(31:16) **Scheduler Block Enable**

Each bit position enables/disables the respective Scheduler Block (31..16):

1	Scheduler Block enabled
0	Scheduler Block disabled

Register 79 USCEN2/DSCEN2
Upstream/Downstream Scheduler Block Enable 2 Registers

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**USCEN2** **AA_H** **DSCEN2** **$C2_H$**
Typical Usage:	Written by CPU for global Scheduler configuration

Bit	15	14	13	12	11	10	9	8
	SchedEn(47:40)							

Bit	7	6	5	4	3	2	1	0
	SchedEn(39:32)							

SchedEn(47:32) **Scheduler Block Enable**
Each bit position enables/disables the respective Scheduler Block (47..32):

1	Scheduler Block enabled
0	Scheduler Block disabled

Register 80 USCEN3/DSCEN3 Upstream/Downstream Scheduler Block Enable 3 Registers

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**USCEN3**	**AB_H**	**DSCEN3**	**$C3_H$**
Typical Usage:	Written by CPU for global Scheduler configuration			

Bit	15	14	13	12	11	10	9	8
	SchedEn(63:56)							

Bit	7	6	5	4	3	2	1	0
	SchedEn(55:48)							

SchedEn(63:48) **Scheduler Block Enable**

Each bit position enables/disables the respective Scheduler Block (63..48):

1	Scheduler Block enabled
0	Scheduler Block disabled

Register 81 USCEN4/DSCEN4
Upstream/Downstream Scheduler Block Enable 4 Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **USCEN4** **AC_H** **DSCEN4** **$C4_H$**

Typical Usage: Written by CPU for global Scheduler configuration

Bit	15	14	13	12	11	10	9	8
	SchedEn(79:72)							

Bit	7	6	5	4	3	2	1	0
	SchedEn(71:64)							

SchedEn(79:64) **Scheduler Block Enable**
Each bit position enables/disables the respective Scheduler Block (79..64):

1	Scheduler Block enabled
0	Scheduler Block disabled

Register 82 USCEN5/DSCEN5
Upstream/Downstream Scheduler Block Enable 5 Registers

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**USCEN5**	**AD_H**	**DSCEN5**	**$C5_H$**
Typical Usage:	Written by CPU for global Scheduler configuration			

Bit	15	14	13	12	11	10	9	8
	SchedEn(95:88)							

Bit	7	6	5	4	3	2	1	0
	SchedEn(87:80)							

SchedEn(95:80) **Scheduler Block Enable**
Each bit position enables/disables the respective Scheduler Block (95..80):

1	Scheduler Block enabled
0	Scheduler Block disabled

Register 83 USCEN6/DSCEN6
Upstream/Downstream Scheduler Block Enable 6 Registers

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**USCEN6**	**AE_H**	**DSCEN6**	**$C6_H$**
Typical Usage:	Written by CPU for global Scheduler configuration			

Bit	15	14	13	12	11	10	9	8
	SchedEn(111:104)							

Bit	7	6	5	4	3	2	1	0
	SchedEn(103:96)							

SchedEn (111:96)

Scheduler Block Enable

Each bit position enables/disables the respective Scheduler Block (111..96):

1	Scheduler Block enabled
0	Scheduler Block disabled

Register 84 USCEN7/DSCEN7
Upstream/Downstream Scheduler Block Enable 7 Registers

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **USCEN7** **AF_H** **DSCEN7** **$C7_H$**

Typical Usage: Written by CPU for global Scheduler configuration

Bit	15	14	13	12	11	10	9	8
	SchedEn(127:120)							

Bit	7	6	5	4	3	2	1	0
	SchedEn(119:112)							

SchedEn (127:112)

Scheduler Block Enable

Each bit position enables/disables the respective Scheduler Block (127..112):

1	Scheduler Block enabled
0	Scheduler Block disabled

7.2.20 Common Real Time Queue Rate Registers

Register 85 UCRTRI/DCRTRI
Upstream/Downstream CRT Rate Integer Registers

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**UCRTRI**	**$B0_H$**	**DCRTRI**	**$C8_H$**
Typical Usage:	Written by CPU for global Scheduler configuration			

Bit	15	14	13	12	11	10	9	8
	Unused(5:0)						CRTIntRate(9:8)	

Bit	7	6	5	4	3	2	1	0
	CRTIntRate(7:0)							

CRTIntRate(9:0) Integer part of CRT Queue Rate

Refer to **Section 4.2.2.3 "Programming the Common Real-Time Bypass" on Page 109** for the calculation of CRTIntRate and CRTFracRate

Register 86 UCRTRF/DCRTRF
Upstream/Downstream CRT Rate Fractional Registers

CPU Accessibility:	**Read/Write**			
Reset Value:	**0000_H**			
Offset Address:	**UCRTRF**	**$B1_H$**	**DCRTRF**	**$C9_H$**
Typical Usage:	Written and Read by CPU			

Bit	15	14	13	12	11	10	9	8
	Init(7:0)							

Bit	7	6	5	4	3	2	1	0
	CRTFracRate(7:0)							

Init(7:0) **Scheduler Initialization Value**
This bit field must be written to 00_H at the time of Scheduler configuration/initialization and should not be written during normal operation.

CRTFracRate (7:0) **CRT Fractional Rate**
This value determines the fractional part of the CRT Queue output rate. Refer to **Section 4.2.2.3 "Programming the Common Real-Time Bypass" on Page 109** for the calculation of CRTIntRate and CRTFracRate

7.2.21 AVT Table Registers

Internal Table 10: VBR Table Transfer Registers

VBR Context Table Transfer Registers are used to access the VBR Context Table (AVT).

Refer to **Chapter 3.5.9.1** for the RAM organization of this table.

Table 7-25 provides an overview of the registers involved. Each AVT word consists of 32 bits.

Table 7-25 Registers for AVT Table Access

31 … 0		RAM Select:
AVT RAM word		
15 … 0	15 … 0	15 … 0
ERCT1	ERCT0	MAR=$0A_H$
		Entry Select:
15 … 0	15 … 0	15 … 0
ERCM1	ERCM0	WAR: EntrySel(9:0) = (0..1023_D) WordSel(2:0) = (0..7_D)

ERCT0 and ERCT1 are the transfer registers for one 32-bit word of the AVT table. Access to words are controlled by mask registers ERCM0/ERCM1.

The context entry number and the corresponding word number representing the table word which needs to be read or written must be written to the Word Address Register (WAR). The dedicated AVT table word is read into the ERCT0/ERCT1 transfer registers or modified by the ERCT0/ERCT1 transfer register values with a write mechanism. The associated mask registers ERCM0 and ERCM1 allow a bit-wise Write operation (0 - unmasked, 1 - masked). In case of Read operation, the dedicated ERCT0/ERCT1 register bit will be overwritten by the respective AVT table entry bit value. In case of Write operation, the dedicated ERCT0/ERCT1 register bit will modify the respective AVT table entry bit value.

The Read or Write process is controlled by the Memory Address Register (MAR). The 5 LSBs (= Bit 4..0) of the MAR register select the memory/table that will be accessed; to select the AVT table bit field MAR(4:0) must be set to 08_H.

Bit 5 of MAR starts the transfer and is cleared automatically after execution.

Table 7-26 WAR Register Mapping for AVT Table Access

Bit	15	14	13	12	11	10	9	8
	Unused(2:0)			EntrySel(9:5)				

Bit	7	6	5	4	3	2	1	0
	EntrySel(4:0)					WordSel(2:0)		

EntrySel(9:0) Selects one of the 1024 AVT table context entries.

WordSel(2:0) Selects one of the 8 DWORDs per AVT table context entries.

Register 87 ERCT0
AVT Table Transfer Register 0

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **ERCT0** **CA_H**
Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	Word0(15:8)							

Bit	7	6	5	4	3	2	1	0
	Word0(7:0)							

Word0(15:0) The meaning of the 'Word0' depends on:
– The selected context entry word (WordSel(2:0))
– The mode of this particular context entry

For detailed description of the context entry fields refer to **"AVT Context RAM Organization and Addressing" on Page 95** f.

Register 88 ERCT1
AVT Table Transfer Register 1

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **ERCT1** **CB_H**

Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	Word1(31:24)							

Bit	7	6	5	4	3	2	1	0
	Word1(23:16)							

Word1(31:16) The meaning of the 'Word1' depends on
- The selected context entry word (WordSel(2:0))
- The mode of this particular context entry

For detailed description of the context entry fields refer to **"AVT Context RAM Organization and Addressing" on Page 95** f.

Register 89 ERCM0
AVT Table Access Mask Register 0

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **ERCM0** **CC_H**
Typical Usage: Written by CPU to control internal table Read/Write access

Bit	15	14	13	12	11	10	9	8
	ERCM0(15:8)							

Bit	7	6	5	4	3	2	1	0
	ERCM0(7:0)							

ERCM0(15:0) **ERC Mask Register 0**

ERC Mask Registers 0..1 control the Write access from transfer registers ERCT0 and ERCT1 to the internal AVT table on a per-bit selection basis. The mask register bit positions correspond to the respective transfer registers ERCT0 and ERCT1:

0	The dedicated bit of the transfer register overwrites the table entry during Write. Does not affect Read access.
1	The dedicated bit of the transfer register does *not* overwrite the table entry during Write. Does not affect Read access.

Register 90 ERCM1
AVT Table Access Mask Register 1

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**ERCM0** **CD_H**
Typical Usage:	Written by CPU to control internal table Read/Write access

Bit	15	14	13	12	11	10	9	8
	ERCM1(31:24)							

Bit	7	6	5	4	3	2	1	0
	ERCM1(23:16)							

ERCM1(31:16) **ERC Mask Register 1**

ERC Mask Registers 0..1 control the Write access from transfer registers ERCT0 and ERCT1 to the internal AVT table on a per-bit selection basis. The mask register bit positions correspond to the respective transfer registers ERCT0 and ERCT1:

0	The dedicated bit of the transfer register overwrites the table entry during Write. Does not affect Read access.
1	The dedicated bit of the transfer register does *not* overwrite the table entry during Write. Does not affect Read access.

Register 91 ERCCONF0
ERC Configuration Register 0

CPU Accessibility:	**Read/Write**
Reset Value:	**0061_H**
Offset Address:	**ERCCONF0 $D5_H$**
Typical Usage:	Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	unused	unused(3:0)				unused	unused	SCAND

Bit	7	6	5	4	3	2	1	0
	unused	SCANP(6:0)						

SCAND **SCAN Disable**

0	SCAN enabled
1	SCAN disabled

SCANP(6:0) **SCAN Period**

Refer to **"Scan Unit" on Page 90** for a description

7.2.22 PLL Control Registers

Register 92 PLL1CONF
PLL1 Configuration Register

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **PLL1CONF $D7_H$**
Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	Locked1	Div2En1	Div1En1	BYPASS1	PU1	RES1	M1(3:2)	

Bit	7	6	5	4	3	2	1	0
	M1(1:0)		N1(5:0)					

DPLL1 generates a clock that is an alternative clock source for the ABM-3G. The DPLL1 is fed by clock input signal ‘SYSCLK’. Signal ‘SYSCLKSEL’ determines the clock source of the ABM-3G. **Section 3.2.5 “Clocking System” on Page 52** provides the details.

Locked1 **DPLL1 Locked**
(read only)

1 DPLL1 is locked based on the current parameter setting.

0 DPLL1 is in transient status.

Div2En1 **Division Factor 2 Enable for DPLL1**
This bit enables one of the additional divide by 2 factors subsequent to the DPLL1 output.

0 Division Factor 2 disabled.

1 Division Factor 2 enabled.

Div1En1 **Division Factor 1 Enable for DPLL1**
This bit enables one of the additional divide by 2 factors subsequent to the DPLL1 output.

	0	Division Factor 1 disabled.
	1	Division Factor 1 enabled.

BYPASS1 **DPLL1 Bypass**
Switching between bypass and non-bypass mode is glitch-free with respect to the internal clock output. The DPLL1 is bypassed after power-on reset and can be switched to non-bypass mode by software during device configuration.

0	DPLL1 is internally bypassed, i.e. DPLL1 clock input connected to DPLL1 clock output
1	DPLL1 is not bypassed, i.e. DPLL1 clock output is generated by DPLL1 depending on its parameter configuration

PU1 **Power Up DPLL1**

0	DPLL1 is in power-down mode. (The analog part of DPLL1 is switched-off for power saving.)
1	DPLL1 is in power on (operational) mode.

RES1 **Reset DPLL1**

0	DPLL1 is in operational mode.
1	DPLL1 is in reset mode.

Note: The result of reset mode is identical to bypass mode, but switching between reset and non-reset status is not glitch-free with respect to the internal clock output.

M1(3:0) **M1 Parameter of DPLL1**
This parameter determines the first stage division factor of DPLL1. The effective division factor is (M1 + 1) in the range 1..16.

N1(5:0) **N1 Parameter of DPLL1**
This parameter determines the second stage multiplication factor of DPLL1. The effective multiplication factor is (N1 + 1) in the range 1..64.

Register 93 PLLTST
PLL Test Register

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**PLLTST** **$D9_H$**
Typical Usage:	Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	Reserved(15:8)							

Bit	7	6	5	4	3	2	1	0
	Reserved(7:0)							

7.2.23 External RAM Test Registers

Register 94 EXTRAMD0
External RAM Test Data Register 0

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**EXTRAMD0 DC_H**
Typical Usage:	Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	Data(31:24)							

Bit	7	6	5	4	3	2	1	0
	Data(23:16)							

Data(31:16) Upper part of data to be read from or to be written to the external RAM

Note: Only the lower 20 bits of each Cell Pointer RAM entry can be accessed. Read access to the upper bits will always return 0.

Register 95 EXTRAMD1
External RAM Test Data Register 1

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **EXTRAMD1 DD_H**
Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	Data(15:8)							

Bit	7	6	5	4	3	2	1	0
	Data(7:0)							

Data(15:0) Lower part of data to be read from or to be written to the external RAM

Register 96 EXTRAMA0
External RAM Test Address Register Low

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **EXTRAMA0 DE_H**
Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	Address(15:8)							

Bit	7	6	5	4	3	2	1	0
	Address(7:0)							

Address(15:0) Lower bits of the Address

The Address field selects an entry within the external RAM, selected by the EXTRAMC register.

The range depends on the size of the selected external RAM (see **Table 7-27**).

Table 7-27 Extended RAM Address Range for Test Access

RAM Type	Size	Address Range
SSRAM	64 k x 32 bit	0 .. 65536
SSRAM	128 k x 32 bit	0 .. 131072
SSRAM	256 k x 32 bit	0 .. 262144
SSRAM	512 k x 32 bit	0 .. 524288
SDRAM	32 Mbit per core	0 .. 1048576
SDRAM	64 Mbit per core	0 .. 2097152
SDRAM	128 Mbit per core	0 .. 4194304

Register 97 EXTRAMA1
External RAM Test Address Register High

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **EXTRAMA0 DF_H**
Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	Unused(11:4)							

Bit	7	6	5	4	3	2	1	0
	Unused(3:0)				Address(19:16)			

Address(19:16) Upper bits of the Address

The Address field selects an entry within the external RAM, selected by the EXTRAMC register.

The range depends on the size of the selected external RAM (see **Table 7-27**).

Register 98 EXTRAMC
External RAM Test Command Register

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **EXTRAMA0 $E0_H$**
Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	Unused(13:2)							

Bit	7	6	5	4	3	2	1	0
	Unused(1:0)		CSRDW	CSRDR	CSRUW	CSRUR	CPRW	CPRR

Setting a command bit starts the Read or Write procedure from/to the selected external RAM. The corresponding bit is automatically cleared after completion of the Read/Write procedure.
The address to be read or to be written is provided in registers EXTRAMA0 and EXTRAMA1. The 32-bit wide data is transferred via registers EXTRAMD0 and EXTRAMD1.

Note: Access to external RAM is only allowed before first cell flow.

CSRDW Cell Storage RAM downstream write
CSRDR Cell Storage RAM downstream read
CSRUW Cell Storage RAM upstream write
CSRUR Cell Storage RAM upstream read
CPRW Cell Pointer RAM write
CPRR Cell Pointer RAM read

7.2.24 ABM-3G Version Code Registers

Register 99 VERL
Version Number Low Register

CPU Accessibility:	**Read**	
Reset Value:	**F083$_H$**	
Offset Address:	**VERL**	**E1$_H$**
Typical Usage:	Read by CPU to determine device version number	

Bit	15	14	13	12	11	10	9	8
	VERL(15..8)							

Bit	7	6	5	4	3	2	1	0
	VERL(7..0)							

VERL(15..0) **F083$_H$**

Register 100 VERH

Version Number High Register

CPU Accessibility:	**Read**
Reset Value:	**1007_H**
Offset Address:	**VERH** **$E2_H$**
Typical Usage:	Read by CPU to determine device version number

Bit	15	14	13	12	11	10	9	8
	VERH(15..8)							

Bit	7	6	5	4	3	2	1	0
	VERH(7..0)							

VERH(15..0) **1007_H**

7.2.25 Interrupt Status/Mask Registers

Register 101 ISRU

Interrupt Status Register Upstream

CPU Accessibility:	**Read/Write**	
Reset Value:	**0000_H**	
Offset Address:	**ISRU**	**$E3_H$**
Typical Usage:	Read by CPU to evaluate interrupt events related to the upstream core. Interrupt indications must be cleared by writing a 1 to the respective bit locations; writing a 0 has no effect;	

Bit	15	14	13	12	11	10	9	8
	Unused	BCFGE	QIDINV	BUFER 1	LCI INVAL	PARITY ER	SOCER	BUFER 2

Bit	7	6	5	4	3	2	1	0
	BUFER 3	CDVOV	MUXOV	AAL5 COL	RMCER	BIP8ER	BUFER 4	reserve d

BCFGE Buffer Configuration Error upstream

QIDINV This interrupt is generated if the ABM-3G tries to write a cell into a disabled queue. The cell is discarded in this case.
(Typically occurs on queue configuration errors.)

BUFER1 Unexpected buffer error number 1. Should never occur in normal operation. Immediate reset of the chip recommended.

LCIINVAL Error when performing the internal address reduction
The cell is discarded.

PARITYER Parity error at UTOPIA Receive Upstream (PHY) Interface detected.

SOCER	Start of Cell Error at UTOPIA Receive Upstream (PHY) Interface detected.
BUFER2	Unexpected Buffer Error number 2. Should never occur in normal operation. Immediate reset of the chip is recommended.
BUFER3	Unexpected Buffer Error number 3. Should never occur in normal operation. Immediate reset of the chip is recommended.
CDVOV	The maximum upstream CDV value for shaped connections given in CDVU register has been exceeded. This interrupt is a notification only; that is, no cells are discarded due to this event.
MUXOV	Indicates that a Scheduler Block lost a serving time slot. (Can indicate a static backpressure on one port). The 'MUXOV' interrupt is generated when the number of lost serving time slots exceeds the number specified in bit field MaxBurstS(3:0) (see register UECRI/DECRI). No further action is required upon this interrupt.
AAL5COL	Indicates that an interrupt event occurred in the upstream AAL5 unit. The interrupt reason must be read from the AAL5 status register **"UA5SARS/DA5SARS" on Page 172** (upstream).
RMCER	RM Cell received with corrupted CRC-10.
BIP8ER	BIP-8 error detected when reading a cell from the upstream external SDRAM. BIP-8 protects the cell header of each cell. The cell is discarded. One single sporadic event can be ignored. Hardware should be taken out of service when the error rate exceeds 10^{-10}.

BUFER4	Unexpected Buffer Error number 4. Should never occur in normal operation. Immediate reset of the chip recommended. For consistency check the ABM-3G stores the queue ID with each cell written to the respective queue within the cell storage RAM. When reading a cell from the cell storage RAM, the queue ID is compared to the stored queue ID. A queue ID mismatch would indicate a global buffering/pointer problem.

Note: Several mechanisms are implemented in the ABM-3G to check for consistency of pointer operation and internal/external memory control. The interrupt events BUFER1..BUFER4 indicate errors detected by these mechanisms.
It is recommended that these interrupts be classified as "fatal device errors."

Register 102 ISRD

Interrupt Status Register Downstream

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **ISRD** **$E4_H$**

Typical Usage: Read by CPU to evaluate interrupt events related to the downstream core. Interrupt indications must be cleared by writing a 1 to the respective bit locations; writing a 0 has no effect;

Bit	15	14	13	12	11	10	9	8
	Unused	BCFGE	QIDINV	BUFER 1	LCI INVAL	PARITY ER	SOCER	BUFER 2

Bit	7	6	5	4	3	2	1	0
	BUFER 3	CDVOV	MUXOV	AAL5 COL	RMCER	BIP8ER	BUFER 4	reserve d

BCFGE Buffer Configuration Error downstream

QIDINV This interrupt is generated if the ABM-3G tries to Write a cell into a disabled queue. The cell is discarded.
(Typically occurs on queue configuration errors.)

BUFER1 Unexpected Buffer Error number 1. Should never occur in normal operation. Immediate reset of the chip is recommended.

LCIINVAL Error when performing the internal address reduction
The cell is discarded.

PARITYER Parity Error at UTOPIA Receive Downstream (PHY) Interface detected.

SOCER Start of Cell Error at UTOPIA Receive Downstream (PHY) Interface detected.

BUFER2	Unexpected Buffer Error number 2. Should never occur in normal operation. Immediate reset of the chip is recommended.
BUFER3	Unexpected Buffer Error number 3. Should never occur in normal operation. Immediate reset of the chip recommended.
CDVOV	The maximum downstream CDV value for shaped connections given in CDVU register has been exceeded. This interrupt is a notification only; that is, no cells are discarded due to this event.
MUXOV	Indicates that a Scheduler Block lost a serving time slot. (Can indicate a static backpressure on one port). The 'MUXOV' interrupt is generated when the number of lost serving time slots exceeds the number specified in bit field MaxBurstS(3:0) (see register UECRI/DECRI). No further action is required upon this interrupt.
AAL5COL	Indicates that an interrupt event occurred in the downstream AAL5 unit. The interrupt reason must be read from the AAL5 status register **"UA5SARS/DA5SARS" on Page 172** (downstream).
RMCER	RM cell received with corrupted CRC-10.
BIP8ER	BIP-8 error detected when reading a cell from the downstream external SDRAM. BIP-8 protects the cell header of each cell. The cell is discarded. One single sporadic event can be ignored. Hardware should be taken out of service when the error rate exceeds 10^{-10}.

BUFER4	Unexpected Buffer Error number 4. Should never occur in normal operation. Immediate reset of the chip is recommended. For consistency check the ABM-3G stores the queue ID with each cell written to the respective queue within the cell storage RAM. When reading a cell from the cell storage RAM, the queue ID is compared to the stored queue ID. A queue ID mismatch would indicate a global buffering/pointer problem.

Note: Several mechanisms are implemented in the ABM-3G to check for consistency of pointer operation and internal/external memory control. The interrupt events BUFER1..BUFER4 indicate errors detected by these mechanisms.
It is recommended that these interrupts be classified as “fatal device errors.”

Register 103 ISRC

Interrupt Status Register Common

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**ISRC** **$E5_H$**
Typical Usage:	Read by CPU to evaluate interrupt events related to both cores. Interrupt indications must be cleared by writing a 1 to the respective bit locations; writing a 0 has no effect;

Bit	15	14	13	12	11	10	9	8
	Unused(10:3)							

Bit	7	6	5	4	3	2	1	0
	Unused(2:0)			RAMER	DDQRD	UDQRD	DQ VCMGD	UQ VCMGD

RAMER Configuration of common Cell Pointer RAM has been changed after cells have been received (see Register MODE1, bit field CPR).

DDQRD **Downstream Dummy Queue Relogged/Deactivated**
This interrupt confirms the dummy queue operation being activated and deactivated. (see **Register 38: QCT1**)

UDQRD **Upstream Dummy Queue Relogged/Deactivated**
This interrupt confirms the dummy queue operation being activated and deactivated. (see **Register 38: QCT1**)

DQVCMGD **Downstream Queue VC-Merge Group Deactivated**
This interrupt confirms the VC-Merge group being deactivated.

UQVCMGD **Upstream Queue VC-Merge Group Deactivated**
This interrupt confirms the VC-Merge group being deactivated.

Register 104 IMRU
Interrupt Mask Register Upstream

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**IMRU** **$E6_H$**
Typical Usage:	Written by CPU to control interrupt signal effective events

Bit	15	14	13	12	11	10	9	8
	IMRU(15:8)							

Bit	7	6	5	4	3	2	1	0
	IMRU(7:0)							

IMRU(15:0) **Interrupt Mask Upstream**
Each bit controls whether the corresponding interrupt indication in register ISRU (same bit location) activates the interrupt signal:

1	Interrupt indication masked. The interrupt signal is not activated upon this event.
0	Interrupt indication unmasked. The interrupt signal is activated upon this event.

Register 105 IMRD

Interrupt Mask Register Downstream

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**IMRD** **$E7_H$**
Typical Usage:	Written by CPU to control interrupt signal effective events

Bit	15	14	13	12	11	10	9	8
	IMRD(15:8)							

Bit	7	6	5	4	3	2	1	0
	IMRD(7:0)							

IMRD(15:0) **Interrupt Mask Downstream**

Each bit controls whether the corresponding interrupt indication in register ISRD (same bit location) activates the interrupt signal:

1	Interrupt indication masked. The interrupt signal is not activated upon this event.
0	Interrupt indication unmasked. The interrupt signal is activated upon this event.

Register 106 IMRC

Interrupt Mask Register Common

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**IMRC** **$E8_H$**
Typical Usage:	Written by CPU to control interrupt signal effective events

Bit	15	14	13	12	11	10	9	8
	IMRC(15:8)							

Bit	7	6	5	4	3	2	1	0
	IMRC(7:0)							

IMRC(15:0) **Interrupt Mask Common**

Each bit controls whether the corresponding interrupt indication in register ISRC (same bit location) activates the interrupt signal:

1	Interrupt indication masked. The interrupt signal is not activated upon this event.
0	Interrupt indication unmasked. The interrupt signal is activated upon this event.

7.2.26 RAM Select Registers

Register 107 MAR

Memory Address Register

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**MAR** **EB_H**
Typical Usage:	Written by CPU to address internal RAM/tables for Read or Write operation via transfer registers

Bit	15	14	13	12	11	10	9	8
	Unused(9:2)							

Bit	7	6	5	4	3	2	1	0
	Unused	Start_W	Start_R	MAR(4:0)				

Start_W This command bit starts the Write procedure to the internal RAM/table addressed by bit field MAR(4:0). The specific data transfer and mask registers must be prepared appropriately in advance. This bit is automatically cleared after completion of the Write procedure.

Start_R Simplifies Read access without need to touch the mask registers

MAR(4:0) **Memory Address**
This bit field selects one of the internal RAM/tables for Read or Write operation:

00000	LCI: LCI Table RAM (see page 191)
00001	TCT: Traffic Class Table (see page 195)
00010	QCT: Queue Configuration Table (see page 211)
00011	SBOC: Scheduler Block Occupation Table (see page 223)
00111	MGT: Merge Group Table (see page 230)
01010	AVT: VBR Table (see page 280)
10000	QPT1 Upstream: Queue Parameter Table 1 Up (see page 247)

10001	QPT2 Upstream: Queue Parameter Table 2 Up (see page 251)
11000	QPT1 Downstream: Queue Parameter Table 1 Dn (see page 247)
11001	QPT2 Downstream: Queue Parameter Table 2 Dn (see page 251)
10111	SCTF Upstream: Scheduler Configuration Table Fractional Part (see page 257)
11111	SCTF Downstream: Scheduler Configuration Table Fractional Part (see page 267)

Note: The SCTI Table (Scheduler Configuration Table Integer Part) is addressed via dedicated address registers and thus not listed in bit field MAR(4:0) (see page 259).

Note: MAR(4:0) values not listed above are invalid and reserved. It is recommended to not use invalid/reserved values.

Register 108 WAR

Word Address Register

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**WAR** **EC_H**
Typical Usage:	Written by CPU to address entries of internal RAM/ tables for Read or Write operation via transfer registers.

Bit	15	14	13	12	11	10	9	8
	WAR(15:8)							

Bit	7	6	5	4	3	2	1	0
	WAR(7:0)							

WAR(15:0) **Word Address**

This bit field selects an entry within the internal RAM/table selected by the MAR register.
In general, it can address up to 64K entries.
The current range of supported values depends on the size and organization of the selected RAM/table.
Thus, the specific WAR register meaning is listed in the overview part of each internal RAM/table description:

LCI	LCI Table RAM (see page 191)
TCT	Traffic Class Table (see page 195)
QCT	Queue Configuration Table (see page 223)
SBOC	Scheduler Block Occupation Table (see page 223)
QPTHU	QPT High Word Upstream: Queue Parameter Table (see page 247f.)
QPTHD	QPT High Word Downstream: Queue Parameter Table (see page 247f.)
QPTLU	QPT Low Word Upstream: Queue Parameter Table(see page 247)
QPTLD	QPT Low Word Downstream: Queue Parameter Table (see page 247)

SCTFU SCTF Upstream:
Scheduler Configuration Table Fractional Part
(see page 267)

SCTFD SCTF Downstream:
Scheduler Configuration Table Fractional Part
(see page 267)

Note: The SCTI Table (Scheduler Configuration Table Integer Part) is addressed via dedicated address registers and, thus, is not listed in the MAR and WAR registers (see page 257).

7.2.27 Global ABM-3G Status and Mode Registers

Register 109 USTATUS

ABM-3G UTOPIA Status Register

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **USTATUS** **ED_H**

Typical Usage: Read by CPU

Bit	15	14	13	12	11	10	9	8
	unused	DUTFL(6:0)						

Bit	7	6	5	4	3	2	1	0
	unused	UUTFL(6:0)						

DUTFL(6:0) **Downstream UTOPIA Receive Buffer Fill Level**
This bit field indicates the current number of cells stored in the UTOPIA receive buffers (0..64 cells).

UUTFL(6:0) **Upstream UTOPIA Receive Buffer Fill Level**
This bit field indicates the current number of cells stored in the UTOPIA receive buffer (0..64 cells).

Register 110 MODE1

ABM-3G Mode 1 Register

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **MODE1** **EE_H**

Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	SWRES	0	CPR(1:0)		VC MERGE	INIT RAM	INIT SDRAM	CORE

Bit	7	6	5	4	3	2	1	0
	WGS	0	0	BIP8	CRC10	LCItog	LCIMOD(1:0)	

SWRES **Software Reset** (clears automatically after four cycles).
This bit is automatically cleared after execution.
'SWRES' controls reset of all ABM-3G units.

1 Starts internal reset procedure

(0) self-clearing

CPR(1:0) **Cell Pointer Ram Size configuration**
(see also **Table 7-3 "External RAM Sizes" on Page 177**)

00 256k pointer entries per direction
(corresponds to 256k cells in each cell storage RAM)

01 128k pointer entries per direction
(corresponds to 128k cells in each cell storage RAM)

10 64k pointer entries per direction
(corresponds to 64k cells in each cell storage RAM)

11 reserved

Note: The Cell Pointer RAM Size should be programmed during initialization and should not be changed during operation.

VCMerge — **VC Merge Enable**

This bit enables VC-Merge operation on a global basis. It determines the usage (required width) of the Cell Pointer RAM, since VC-Merge operation requires one additional flag 'EOP Mark' in the CPR.
(see also Table 5-10 "SSRAM Configuration Examples" on Page 139)

0	VC-Merge operation disabled.
1	VC-Merge operation enabled.

INITRAM — **Init RAM**

Start of Initialization of the internal RAM.
This bit is automatically cleared after execution.

1	Starts internal RAM initialization procedure. *Note: The internal RAM initialization process can be activated only once after hardware reset.*
(0)	self-clearing

INITSDRAM — **Init SDRAM**

Initialization and configuration of the external SDRAM. This bit must be set to 1 after reset (initial pause of at least 200 µs is necessary) and is automatically cleared by the ABM-3G after configuration of the SDRAM has been executed.

1	Starts SDRAM initialization procedure
(0)	self-clearing

CORE — **Downstream Core Disable**

This bit disables the downstream ABM-3G Core, which is necessary in some MiniSwitch configurations (Uni-Directional Mode using one core).
It is recommended to set CORE = 0 in Bi-directional operation modes.

1	Downstream ABM-3G core disabled
0	Downstream ABM-3G core enabled

WGS — **Work Group Switch Mode**

Selects MiniSwitch (Uni-directional) Mode if set to 1.

	1	MiniSwitch (Uni-directional) operation mode selected: upstream transmit UTOPIA Interface is disabled; downstream receive UTOPIA Interface is disabled.
	0	Normal (Bi-directional) operation mode
BIP8	Disables discard of cells with BIP-8 header error.	
	1	BIP-8 errored cells are not discarded
	0	BIP-8 errored cells are discarded
CRC10	Disables discard of RM cells with defect CRC10.	
	1	CRC10 errored RM cells are not discarded
	0	CRC10 errored RM cells are discarded
LCItog	Enables toggling of the LCI(0) bit in outgoing cells in MiniSwitch (uni-directional) mode.	
	1	LCI bit 0 is toggled in outgoing cells in case of MiniSwitch operation mode selected
	0	LCI bit 0 remains unchanged
	Note: Does not affect the cell header if Internal Address Reduction is used.	
LCIMOD(1:0)	Specifies the expected mapping of Local Connection Identifier (LCI) field to cell header:	
	00	LCI(13, 12) ='00', LCI(11:0) mapped to VPI(11:0) field
	01	LCI(15:0) mapped to VCI(15:0) field;
	10	LCI(15:14) mapped to UDF1(1:0) field; LCI(13:12) mapped to UDF1(7:6) field; LCI(11:0) mapped to VPI(11:0) field
	11	Internal Address reduction mode; The LCI is derived from programmable parts of the VPI, VCI and PN bit fields. The derived LCI is used by the ABM-3G, but nor written to the cell.

Register 111 MODE2

ABM-3G Mode 2 Register

CPU Accessibility: **Read/Write**

Reset Value: **0800_H**

Offset Address: **MODE** **EF_H**

Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	SD CAW	SDRR	unused	1	TUTS	DQSC	QS(1:0)	

Bit	7	6	5	4	3	2	1	0
	PNSRC	MNUM(3:0)				PNUM(2:0)		

SDCAW **SDRAM Column Address Width**

0 8 bit

1 9 bit

SDRR **SDRAM Refresh Rate**

0 Default Refresh Rate (4096 cycles/s)

1 Double Refresh Rate (8192 cycles/s)

TUTS **Tristate all UTOPIA Signals**

0 Normal mode

1 UTOPIA Signals in Tristate mode

DQSC **Disable Quarter Segment Check**

0 Normal mode

1 Quarter Segment Check disabled

QS(1:0) **Quarter Segment**

If Quarter Segment Check is enabled, the ABM-3G processes only cells matching the LCI segment:
LCI(15:14) = QS(1:0)
All other cells are forwarded depending on the value found in entry 0 of the LCT table. Default: send to the Common Real-Time Queue to be processed by a subsequent ABM-3G (cascading).

PNSRC	**Port Number Source** This bit determines which Port Number field is used for internal Address Reduction Mode:	
	0	PN field is taken from the UTOPIA Port number, that accepted the cell.
	1	PN field is taken from the UDF1(5:0) field of the cell
MNUM(3:0)	**M Parameter** This bit field determines the ranges of VPI and VCI cell header fields mapped into the LCI in internal Address Reduction mode. **Chapter 3.2.4** provides the details.	
PNUM(2:0)	**P Parameter** This bit field determines the number of port number bits mapped into the LCI in internal Address Reduction mode. **Chapter 3.2.4** provides the details.	

7.2.28 UTOPIA Configuration Registers

Register 112 UTRXCFG
Upstream/Downstream UTOPIA Receive Configuration Register

CPU Accessibility: **Read/Write**
Reset Value: **0001_H**
Offset Address: **UTRXCFG** **$F0_H$**
Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	DURD	DURUT	DURPD	DURPE	DURCFG(1:0)		DURBUS	DURM

Bit	7	6	5	4	3	2	1	0
	UURD	UURUT	UURPD	UURPE	UURCFG(1:0)		UURBUS	UURM

DURD **Downstream UTOPIA Receive Discard**
UURD **Upstream UTOPIA Receive Discard**

0 Normal operation
1 Discard all cells without notification

DURUT **Downstream UTOPIA Receive UDF2 Transparent**
UURUT **Upstream UTOPIA Receive UDF2 Transparent**

0 PN mapped to UDF2 (for internal processing)
1 UDF2 transparent (BIP8 checksum not usable)

DURPD **Downstream UTOPIA Receive Parity Error discard**
UURPD **Upstream UTOPIA Receive Parity Error discard**

0 No discarding of cells with Parity Error

	1	Discarding of cells with Parity Error
DURPE	**Downstream UTOPIA Receive Parity Check Enable**	
UURPE	**Upstream UTOPIA Receive Parity Check Enable**	
	0	Parity check disabled
	1	Parity check enabled
DURCFG(1:0)	**Downstream UTOPIA Receive Port Configuration**	
UURCFG(1:0)	**Upstream UTOPIA Receive Port Configuration**	
	00	4 x 12 ports
	01	4 x 12 ports
	10	4 x 12 ports
	11	Level 1 Mode (4 x 1 port)
DURBUS	**Downstream UTOPIA Receive Bus Width**	
UURBUS	**Upstream UTOPIA Receive Bus Width**	
	0	8-bit bus width
	1	16-bit bus width
DURM	**Downstream UTOPIA Receive Mode**	
UURM	**Upstream UTOPIA Receive Mode**	
	0	Slave Mode
	1	Master Mode

Register 113 UUTRXP0

Upstream UTOPIA Receive Port Register 0

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**UUTRXP0 $F1_H$**
Typical Usage:	Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	UURXPEnable(15..8)							

Bit	7	6	5	4	3	2	1	0
	UUTRXPEnable(7..0)							

UUTRXPEnable (15:0) — **Upstream UTOPIA Receive Port Enable**

Each bit enables or disables the respective UTOPIA port (15..0):

bit = 0 Port disabled.

bit = 1 Port enabled.

Register 114 UUTRXP1

Upstream UTOPIA Receive Port Register 1

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**UUTRXP1** **$F2_H$**
Typical Usage:	Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	UURXPEnable(31..24)							

Bit	7	6	5	4	3	2	1	0
	UUTRXPEnable(23..16)							

UUTRXPEnable (31:16) — **Upstream UTOPIA Receive Port Enable**

Each bit enables or disables the respective UTOPIA port (31..16):

bit = 0	Port disabled.
bit = 1	Port enabled.

Register 115 UUTRXP2
Upstream UTOPIA Receive Port Register 2

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**UUTRXP2 $F3_H$**
Typical Usage:	Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	UURXPEnable(47..40)							

Bit	7	6	5	4	3	2	1	0
	UUTRXPEnable(39..32)							

UUTRXPEnable (47:32) — **Upstream UTOPIA Receive Port Enable**
Each bit enables or disables the respective UTOPIA port (47..32):

bit = 0	Port disabled.
bit = 1	Port enabled.

Register 116 DUTRXP0

Downstream UTOPIA Receive Port Register 0

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**DUTRXP0 $F4_H$**
Typical Usage:	Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	DURXPEnable(15..8)							

Bit	7	6	5	4	3	2	1	0
	DUTRXPEnable(7..0)							

DUTRXPEnable (15:0) — **Downstream UTOPIA Receive Port Enable**

Each bit enables or disables the respective UTOPIA port (15..0):

bit = 0	Port disabled.
bit = 1	Port enabled.

Register 117 DUTRXP1

Downstream UTOPIA Receive Port Register 1

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **DUTRXP1** **$F5_H$**

Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	DURXPEnable(31..24)							

Bit	7	6	5	4	3	2	1	0
	DUTRXPEnable(23..16)							

DUTRXPEnable (31:16) — **Downstream UTOPIA Receive Port Enable**

Each bit enables or disables the respective UTOPIA port (31..16):

bit = 0 Port disabled.

bit = 1 Port enabled.

Register 118 DUTRXP2

Downstream UTOPIA Receive Port Register 2

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**DUTRXP2 $F6_H$**
Typical Usage:	Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	DURXPEnable(47..40)							

Bit	7	6	5	4	3	2	1	0
	DUTRXPEnable(39..32)							

DUTRXPEnable (47:32)

Downstream UTOPIA Receive Port Enable

Each bit enables or disables the respective UTOPIA port (47..32):

bit = 0	Port disabled.
bit = 1	Port enabled.

Register 119 UUTTXCFG
Upstream UTOPIA Transmit Configuration Register

CPU Accessibility: **Read/Write**
Reset Value: **0000_H**
Offset Address: **UUTTXCFG $F7_H$**
Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	unused(2:0)			UUTES	UUTUT	UUTCFG(1:0)		UUTBUS

Bit	7	6	5	4	3	2	1	0
	UUTQL(6:0)							UUTM

UUTM **Upstream UTOPIA Transmit Mode**

0	Slave Mode
1	Master Mode

UUTQL(6:0) **Upstream UTOPIA Transmit Queue Length**
Chapter 5.2.2 provides the details.
64 cells maximum

UURBUS **Upstream UTOPIA Transmit Bus Width**

0	8-bit bus width
1	16-bit bus width

UUTCFG(1:0) **Upstream UTOPIA Transmit Port Configuration**

00	4 x 12 ports
01	4 x 12 ports
10	4 x 12 ports

	11	Level 1 Mode (4 x 1 port)
UUTUT	**Upstream UTOPIA Transmit UDF2 Transparent**	
	0	Port number is mapped to UDF2
	1	UDF2 not modified at transmit Interface (UDF2 transparency if set together with UTRXCFG.UURUT)
UUTES	**Upstream UTOPIA Transmit Extended Slave**	
	0	1x4 or 4x12
	1	1x31 together with UUTM="0" (slave)

Register 120 DUTTXCFG
Downstream UTOPIA Transmit Configuration Register

CPU Accessibility:	**Read/Write**
Reset Value:	**0001_H**
Offset Address:	**DUTTXCFG $F8_H$**
Typical Usage:	Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	unused(2:0)			DUTES	DUTUT	DUTCFG(1:0)		DUTBUS

Bit	7	6	5	4	3	2	1	0
	DUTQL(6:0)							DUTM

DUTM **Downstream UTOPIA Transmit Mode**

0	Slave Mode
1	Master Mode

DUTQL(6:0) **Downstream UTOPIA Transmit Queue Length**
Chapter 5.1.2 provides the details.
64 cells maximum

DURBUS **Downstream UTOPIA Transmit Bus Width**

0	8-bit bus width
1	16-bit bus width

DUTCFG(1:0) **Downstream UTOPIA Transmit Port Configuration**

00	4 x 12 ports
01	4 x 12 ports
10	4 x 12 ports

	11	Level 1 Mode (4 x 1 port)
DUTUT	**Downstream UTOPIA Transmit UDF2 Transparent**	
	0	Port number is mapped to UDF2
	1	UDF2 not modified at transmit Interface (UDF2 transparency if set together with UTRXCFG.DURUT)
DUTES	**Downstream UTOPIA Transmit Extended Slave**	
	0	1x4 or 4x12
	1	1x31 together with UUTM="0" (slave)

Register 121 UUTTXP0
Upstream UTOPIA Transmit Port Register 0

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**UUTTXP0 $F9_H$**
Typical Usage:	Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	UUTXPEnable(15..8)							

Bit	7	6	5	4	3	2	1	0
	UUTTXPEnable(7..0)							

UUTTXPEnable (15:0) — **Upstream UTOPIA Transmit Port Enable**

Each bit enables or disables the respective UTOPIA port (15..0):

bit = 0 Port disabled.

bit = 1 Port enabled.

Note: If transmit port is disabled, cells assigned to this port are discarded without notification

Register 122 UUTTXP1
Upstream UTOPIA Transmit Port Register 1

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**UUTTXP1 FA_H**
Typical Usage:	Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	UUTTXPEnable(31..24)							

Bit	7	6	5	4	3	2	1	0
	UUTTXPEnable(23..16)							

UUTTXPEnable (31:16) — **Upstream UTOPIA Transmit Port Enable**

Each bit enables or disables the respective UTOPIA port (31..16):

bit = 0 Port disabled.

bit = 1 Port enabled.

Note: If transmit port is disabled, cells assigned to this port are discarded without notification

Register 123 UUTTXP2

Upstream UTOPIA Transmit Port Register 2

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **UUTTXP2** **FB_H**

Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	UUTTXPEnable(47..40)							

Bit	7	6	5	4	3	2	1	0
	UUTTXPEnable(39..32)							

UUTTXPEnable (47:32)

Upstream UTOPIA Transmit Port Enable

Each bit enables or disables the respective UTOPIA port (47..32):

bit = 0 Port disabled.

bit = 1 Port enabled.

Note: If transmit port is disabled, cells assigned to this port are discarded without notification

Register 124 DUTTXP0

Downstream UTOPIA Transmit Port Register 0

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**DUTTXP0 FC_H**
Typical Usage:	Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	DUTTXPEnable(15..8)							

Bit	7	6	5	4	3	2	1	0
	DUTTXPEnable(7..0)							

DUTTXPEnable (15:0) — **Downstream UTOPIA Transmit Port Enable**

Each bit enables or disables the respective UTOPIA port (15..0):

bit = 0 Port disabled.

bit = 1 Port enabled.

Note: If transmit port is disabled, cells assigned to this port are discarded without notification

Register 125 DUTTXP1

Downstream UTOPIA Transmit Port Register 1

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **DUTTXP1** **FD_H**

Typical Usage: Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	DUTTXPEnable(31..24)							

Bit	7	6	5	4	3	2	1	0
	DUTTXPEnable(23..16)							

DUTTXPEnable (31:16) **Downstream UTOPIA Transmit Port Enable**

Each bit enables or disables the respective UTOPIA port (31..16):

bit = 0 Port disabled.

bit = 1 Port enabled.

Note: If transmit port is disabled, cells assigned to this port are discarded without notification

Register 126 DUTTXP2
Downstream UTOPIA Transmit Port Register 2

CPU Accessibility:	**Read/Write**
Reset Value:	**0000_H**
Offset Address:	**DUTTXP2 FE_H**
Typical Usage:	Written and Read by CPU

Bit	15	14	13	12	11	10	9	8
	DUTTXPEnable(47..40)							

Bit	7	6	5	4	3	2	1	0
	DUTTXPEnable(39..32)							

DUTTXPEnable (47:32)

Downstream UTOPIA Transmit Port Enable

Each bit enables or disables the respective UTOPIA port (47..32):

bit = 0 Port disabled.

bit = 1 Port enabled.

Note: If transmit port is disabled, cells assigned to this port are discarded without notification

7.2.29 Test Registers/Special Mode Registers

Register 127 TEST
TEST Register

CPU Accessibility: **Read/Write**

Reset Value: **0000_H**

Offset Address: **TEST** **FF_H**

Typical Usage: Written and Read by CPU for device test purposes

Bit	15	14	13	12	11	10	9	8
	Unused(5:0)						Reserved(7:6)	

Bit	7	6	5	4	3	2	1	0
	CLKdelay(1:0)		Reserved(5:0)					

CLKDelay(1:0) This bit field adjusts the delay of RAMCLK output with respect to SYSCLK input. **"Test Interface" on Page 141** provides the details.

00	Delay 0
01	Delay 2
10	Delay 4
11	Delay 6

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Table 8-1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under biasPXF	T_A	-40 to 85	°C
Storage temperature	T_{stg}	-40 to 125	°C
IC supply voltage with respect to ground	V_{DD}	-0.3 to 3.6	V
Voltage on any pin with respect to ground	V_S	-0.4 to V_{DD} + 0.4	V
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	2000	V

1) According to MIL-Std 883D, method 3015.7 and ESD Association Standard EOS/ESD-5.1-1993. The RF Pins 20, 21, 26, 29, 32, 33, 34 and 35 are not protected against voltage stress > 300 V (versus V_S or GND). The high frequency performance prohibits the use of adequate protective structures.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8.2 Operating Range

Table 8-2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature under bias	T_A	-40	85	°C	
Junction temperature	T_J		125	°C	
Supply voltage 3.3V	V_{DD33}	3.0	3.6	V	
Supply voltage 1.8V	V_{DD18}	1.62	1.98	V	
Ground	V_{SS}	0	0	V	
Power dissipation	P		2.5	W	

Note: In the operating range, the functions given in the circuit description are fulfilled.

8.3 DC Characteristics

Table 8-3 DC Characteristics

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max		
Input low voltage	V_{IL}	–0.4		0.8	V	
Input high voltage	V_{IH}	2.0		V_{DD} + 0.3	V	LVTTL (3.3 V)
Output low voltage	V_{OL}		0.2	0.4	V	I_{OL} = 5 mA
Output high voltage	V_{OH}	2.4		V_{DD}	V	I_{OH} = – 5 mA all pins except TDO (TDO: I_{OH} = – 3 mA)
Average power supply current	I_{CC} (AV)		330		mA	V_{DD33} = 3.3 V, V_{DD18} = 1.8 V, T_A = 25 °C, SYSCLK = 52 MHz; URXCLKU = UTXCLKU = URXCLKD = UTXCLKD = 52 MHz;
Average power down supply current	I_{CCPD} (AV)			10	mA	V_{DD} = 3.3 V, T_A = 25 °C, no output loads, no clocks
Average power dissipation	P (AV)		1	1.3	W	V_{DD33} = 3.3 V, V_{DD18} = 1.8 V, T_A = 25 °C, SYSCLK = 52 MHz; URXCLKU = UTXCLKU = URXCLKD = UTXCLKD = 52 MHz;

Table 8-3 DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max		
Input current	I_{IIN}	-1		1	µA	$V_{IN} = V_{DD33}$ or V_{SS}
		4		8	µA	$V_{IN} = V_{DD33}$ for Inputs with internal Pull-Down resistor
		-4		-8	µA	$V_{IN} = V_{SS}$ for Inputs with internal Pull-Up resistor
Input leakage current	I_{IL}			1	µA	V_{DD33} = 3.3 V, V_{DD18} = 1.8 V, GND = 0 V; all other pins are floating
Output leakage current	I_{OZ}			1	µA	V_{DD33} = 3.3 V, V_{DD18} = 1.8 V, GND = 0 V; V_{OUT} = 0 V

8.4 AC Characteristics

T_A = -40 to 85 °C, V_{DD33} = 3.3 V ± 10%, V_{DD18} = 1.8 V ± 10%, V_{SS} = 0 V

All inputs are driven to V_{IH} = 2.4 V for a logical 1
and to V_{IL} = 0.4 V for a logical 0

All outputs are measured at V_H = 2.0 V for a logical 1
and at V_L = 0.8 V for a logical 0

The AC testing input/output waveforms are shown in **Figure 8-1**.

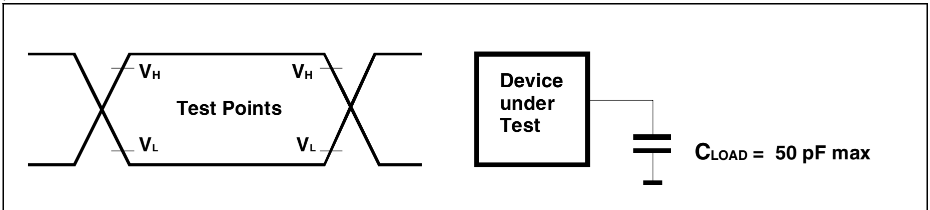


Figure 8-1 Input/Output Waveform for AC Measurements

Table 8-4 Clock Frequencies

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Core clock (internal)	$f_{int.coreclock}$	25	52	MHz
External core clock source	SYSCLK	25	52	MHz
UTOPIA clocks at PHY-side	UTRXCLKU	$f_{int.coreclock}/2$	MIN $\{f_{int.\ coreclock}$, 52 MHz$\}$	MHz
	UTTXCLKD	$f_{int.coreclock}/2$	MIN $\{f_{int.\ coreclock}$, 52 MHz$\}$	MHz
UTOPIA clock at Backplane-side	UTRXCLKD	$f_{int.coreclock}/2$	MIN $\{f_{int.\ coreclock}$, 52 MHz$\}$	MHz
	UTTXCLKU	$f_{int.coreclock}/2$	MIN $\{f_{int.\ coreclock}$, 52 MHz$\}$	MHz
Clock for external RAM	RAMCLK	$f_{int.coreclock}$	$f_{int.coreclock}$	

8.4.1 Microprocessor Interface Timing Intel Mode

8.4.1.1 Microprocessor Write Cycle Timing (Intel)

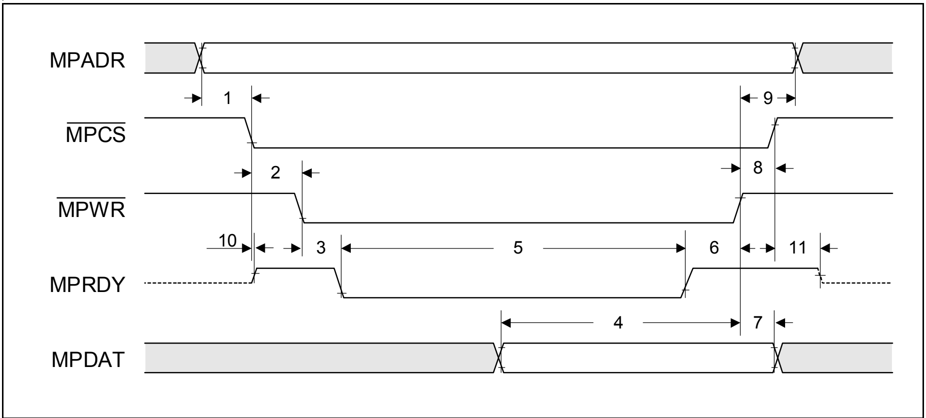


Figure 8-2 Microprocessor Interface Write Cycle Timing (Intel)

Table 8-5 Microprocessor Interface Write Cycle Timing (Intel)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	MPADR setup time before MPCS low	0			ns
2	MPCS setup time before MPWR low	0			ns
3	MPRDY low delay after MPWR low	0		20	ns
4	MPDAT setup time before MPWR high	5			ns
5	Pulse width MPRDY low	4 SYSCLK cycles		5 SYSCLK cycles	
6	MPRDY high to MPWR high	5			ns
7	MPDAT hold time after MPWR high	5			ns
8	MPCS hold time after MPWR high	5			ns
9	MPADR hold time after MPWR high	5			ns
10	MPCS low to MPRDY low impedance	0			ns
11	MPCS high to MPRDY high impedance			15	ns

8.4.1.2 Microprocessor Read Cycle Timing (Intel)

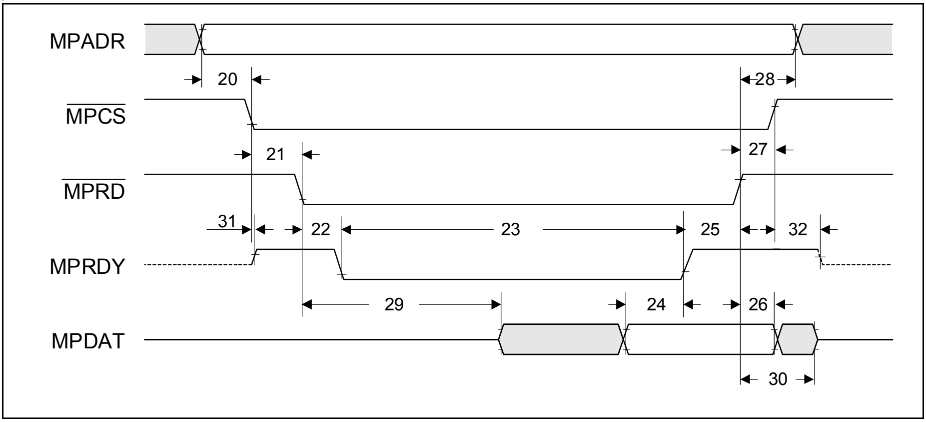


Figure 8-3 Microprocessor Interface Read Cycle Timing (Intel)

Table 8-6 Microprocessor Interface Read Cycle Timing (Intel)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
20	MPADR setup time before $\overline{MPCS}$ low	0			ns
21	$\overline{MPCS}$ setup time before $\overline{MPRD}$ low	0			ns
22	MPRDY low delay after $\overline{MPRD}$ low	0		20	ns
23	Pulse width MPRDY low	4 SYSCLK cycles		5 SYSCLK cycles	
24	MPDAT valid before MPRDY high	5			ns
25	MPRDY high to $\overline{MPRD}$ high	5			ns
26	MPDAT hold time after $\overline{MPRD}$ high	2			ns
27	$\overline{MPCS}$ hold time after $\overline{MPRD}$ high	5			ns
28	MPADR hold time after $\overline{MPRD}$ high	5			ns
29	$\overline{MPRD}$ low to MPDAT low impedance	0		15	ns
30	$\overline{MPRD}$ high to MPDAT high impedance	0		17	ns
31	$\overline{MPCS}$ low to MPRDY low impedance	0			ns
32	$\overline{MPCS}$ high to MPRDY high impedance			15	ns

8.4.2 Microprocessor Interface Timing Motorola Mode

8.4.2.1 Microprocessor Write Cycle Timing (Motorola)

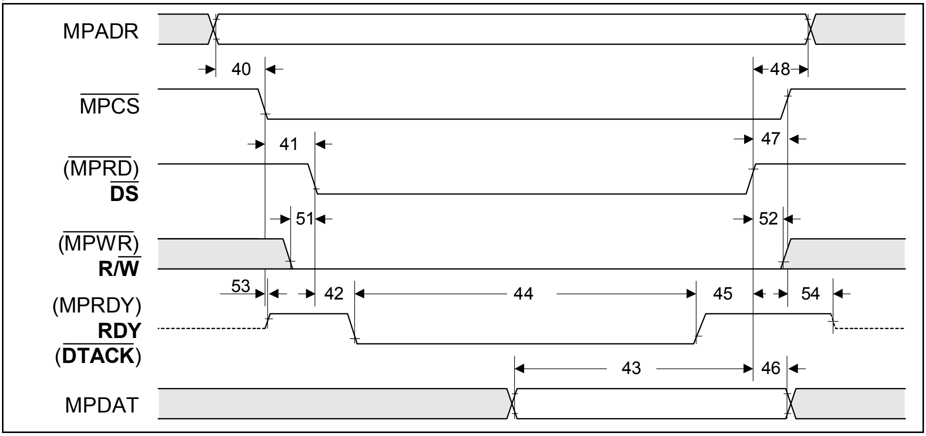


Figure 8-4 Microprocessor Interface Write Cycle Timing (Motorola)

Table 8-7 Microprocessor Interface Write Cycle Timing (Motorola)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
40	MPADR setup time before MPCS low	0			ns
41	MPCS setup time before DS low	0			ns
42	RDY low delay after DS low	0		20	ns
43	MPDAT setup time before DS high	5			ns
44	Pulse width RDY low	4 SYSCLK cycles		5 SYSCLK cycles	
45	RDY high to DS high	5			ns
46	MPDAT hold time after DS high	5			ns
47	MPCS hold time after DS high	5			ns
48	MPADR hold time after DS high	5			ns
51	R/W setup time before DS low	10			ns
52	R/W hold time after DS high	0			ns

Table 8-7 Microprocessor Interface Write Cycle Timing (Motorola) (cont'd)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
53	MPCS low to RDY low impedance	0			ns
54	MPCS high to RDY high impedance			15	ns

8.4.2.2 Microprocessor Read Cycle Timing (Motorola)

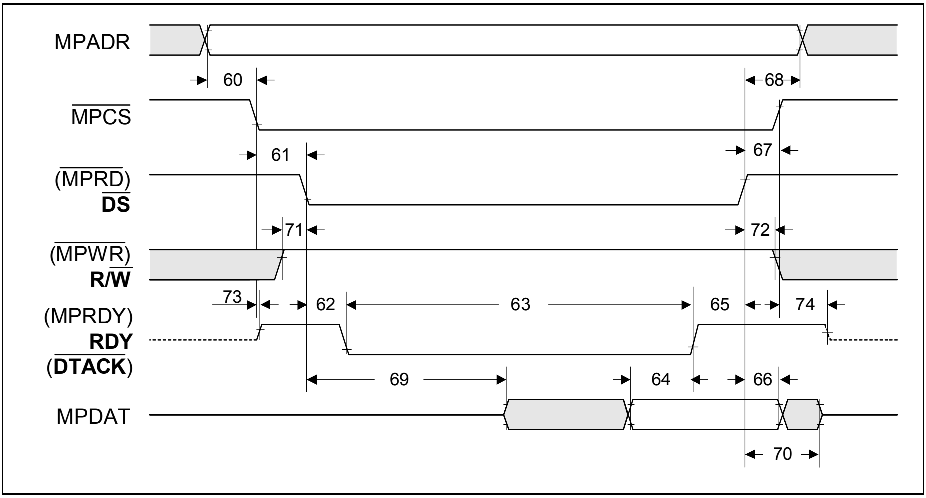


Figure 8-5 Microprocessor Interface Read Cycle Timing (Motorola)

Table 8-8 Microprocessor Interface Read Cycle Timing (Motorola)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
60	MPADR setup time before MPCS low	0			ns
61	MPCS setup time before DS low	0			ns
62	RDY low delay after DS low	0		20	ns
63	Pulse width RDY low	4 SYSCLK cycles		5 SYSCLK cycles	
64	MPDAT valid before RDY high	5			ns
65	RDY high to DS high	5			ns

Table 8-8 Microprocessor Interface Read Cycle Timing (Motorola) (cont'd)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
66	MPDAT hold time after $\overline{\text{DS}}$ high	2			ns
67	$\overline{\text{MPCS}}$ hold time after $\overline{\text{DS}}$ high	5			ns
68	MPADR hold time after $\overline{\text{DS}}$ high	5			ns
69	$\overline{\text{DS}}$ low to MPDAT low impedance	0		15	ns
70	$\overline{\text{DS}}$ high to MPDAT high impedance	0		17	ns
71	R/$\overline{\text{W}}$ setup time before $\overline{\text{DS}}$ low	10			ns
72	R/$\overline{\text{W}}$ hold time after $\overline{\text{DS}}$ high	0			ns
73	$\overline{\text{MPCS}}$ low to RDY low impedance	0			ns
74	$\overline{\text{MPCS}}$ high to RDY high impedance			15	ns

8.4.3 UTOPIA Interface

The AC characteristics of the UTOPIA Interface fulfill the standard of [3] and [4]. Setup and hold times of the 50 MHz UTOPIA Specification are valid. According to the UTOPIA Specification, the AC characteristics are based on the timing specification for the receiver side of a signal. The setup and the hold times are defined with regards to a positive clock edge, see **Figure 8-6**.

Taking into account the actual clock frequency (up to the maximum frequency), the corresponding (min. and max.) transmit side “clock to output” propagation delay specifications can be derived. The timing references (tT5 to tT12) are according to the data found in **Table 8-9** through **Table 8-12**.

Note: The UTOPIA Receive Interface backplane-side is optimized for operation up to 60 MHz UTOPIA clock frequency to achieve a speed-up factor of 1.25 in bandwidth accepted from the backplane (respective values provided in brackets).

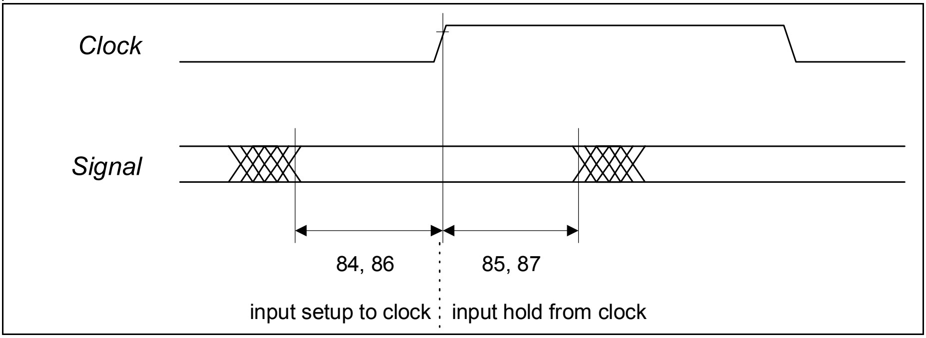


Figure 8-6 Setup and Hold Time Definition (Single- and Multi-PHY)

Figure 8-7 shows the tristate timing for the multi-PHY application (multiple PHY devices, multiple output signals are multiplexed together).

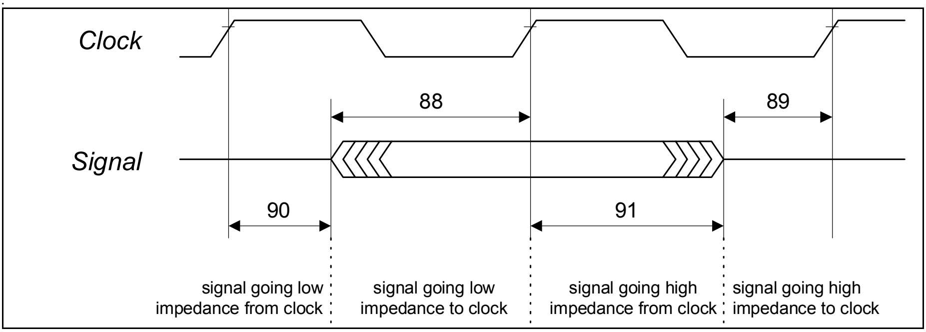


Figure 8-7 Tristate Timing (Multi-PHY, Multiple Devices Only)

In the following tables, A⇒P (column DIR, Direction) defines a signal from the ATM Layer (transmitter, driver) to the PHY Layer (receiver), A⇐P defines a signal from the PHY Layer (transmitter, driver) to the ATM Layer (receiver).

Both UTOPIA Interfaces (PHY-side and Backplane-side) can be configured in either Slave or Master Mode. If configured in Master Mode, the interface is considered to be the ATM Layer device (A) and if configured in Slave Mode, the interface is considered to be the PHY Layer device (P) respectively.

All timings also apply to UTOPIA Level 1 8-bit data bus operation.

.

Table 8-9 Transmit Timing (16-Bit Data Bus, 50 MHz Cell Mode, Single PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	UTXCLKD, UTXCLKU	A>P	TxClk frequency (nominal)	0	52	MHz
81			TxClk duty cycle	40	60	%
82			TxClk peak-to-peak jitter	-	5	%
83			TxClk rise/fall time	-	2	ns
84	UTXDATD, UTXDATU, UTXPRTYD, UTXPRTYU, UTXSOCD, UTXSOCU, $\overline{\text{UTXENBD}}$, $\overline{\text{UTXENBU}}$	A>P	Input setup to TxClk	4	-	ns
85			Input hold from TxClk	1	-	ns
86	UTXCLAVD, UTXCLAVU	A<P	Input setup to TxClk	4	-	ns
87			Input hold from TxClk	1	-	ns

.

Table 8-10 Receive Timing (16-Bit Data Bus, 50 MHz Cell Mode, Single PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	URXCLKD, URXCLKU	A>P	RxClk frequency (nominal) URXCLKD: URXCLKU:	 0 0	 52 52	MHz
81			RxClk duty cycle	40	60	%
82			RxClk peak-to-peak jitter	-	5	%
83			RxClk rise/fall time	-	2	ns

Table 8-10 Receive Timing (16-Bit Data Bus, 50 MHz Cell Mode, Single PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
84	URXENBD, URXENBU	A>P	Input setup to RxClk	4	-	ns
85			Input hold from RxClk	1	-	ns
86	URXDATD, URXDATU, URXPRTYD, URXPRTYU, URXSOCD, URXSOCU, URXCLAVD, URXCLAVU	A<P	Input setup to RxClk	4	-	ns
87			Input hold from RxClk	1	-	ns

.

Table 8-11 Transmit Timing (16-Bit Data Bus, 50 MHz Cell Mode, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	UTXCLKD, UTXCLKU	A>P	TxClk frequency (nominal)	0	52	MHz
81			TxClk duty cycle	40	60	%
82			TxClk peak-to-peak jitter	-	5	%
83			TxClk rise/fall time	-	2	ns
84	UTXDATD, UTXDATU, UTXPRTYD, UTXPRTYU, UTXSOCD, UTXSOCU, UTXENBD, UTXENBU, UTXADRD, UTXADRU	A>P	Input setup to TxClk	4	-	ns
85			Input hold from TxClk	1	-	ns

Table 8-11 Transmit Timing (16-Bit Data Bus, 50 MHz Cell Mode, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
86	UTXCLAVD,	A<P	Input setup to TxClk	4	-	ns
87	UTXCLAVU		Input hold from TxClk	1	-	ns
88			Signal going low impedance to TxCLK	4	-	ns
89			Signal going high impedance to TxCLK	0	-	ns
90			Signal going low impedance from TxCLK	1	-	ns
91			Signal going high impedance from TxCLK	1	-	ns

Table 8-12 Receive Timing (16-Bit Data Bus, 50 MHz Cell Mode, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
80	URXCLKD, URXCLKU	A>P	RxClk frequency (nominal) URXCLKD: URXCLKU:	 0 0	 52 52	MHz
81			RxClk duty cycle	40	60	%
82			RxClk peak-to-peak jitter	-	5	%
83			RxClk rise/fall time	-	2	ns
84	URXENBD,	A>P	Input setup to RxClk	4	-	ns
85	URXENBU, URXADRD, URXADRU		Input hold from RxClk	1	-	ns

Table 8-12 Receive Timing (16-Bit Data Bus, 50 MHz Cell Mode, Multi-PHY)

No.	Signal Name	DIR	Description	Limit Values		Unit
				Min	Max	
86	URXDATD, URXDATU, URXPRTYD, URXPRTYU, URXSOCD, URXSOCU, URXCLAVD, URXCLAVU	A<P	Input setup to RxClk	4	-	ns
87			Input hold from RxClk	1	-	ns
88			Signal going low impedance to RxCLK	4	-	ns
89			Signal going high impedance to RxCLK	0	-	ns
90			Signal going low impedance from RxCLK	1	-	ns
91			Signal going high impedance from RxCLK	1	-	ns

Note: The setup and hold times for receive Interfaces deviate for non-standard 60 MHz operation. Timings are provided on request.

8.4.4 CPR SSRAM Interface

Timing of the Synchronous Static RAM Interfaces is simplified as all signals are referenced to the rising edge of RAMCLK. In **Figure 8-8**, it can be seen that all signals output by the ABM-3G have identical delay times with reference to the clock. When reading from the RAM, the ABM-3G samples the data within a window at the rising clock edge.

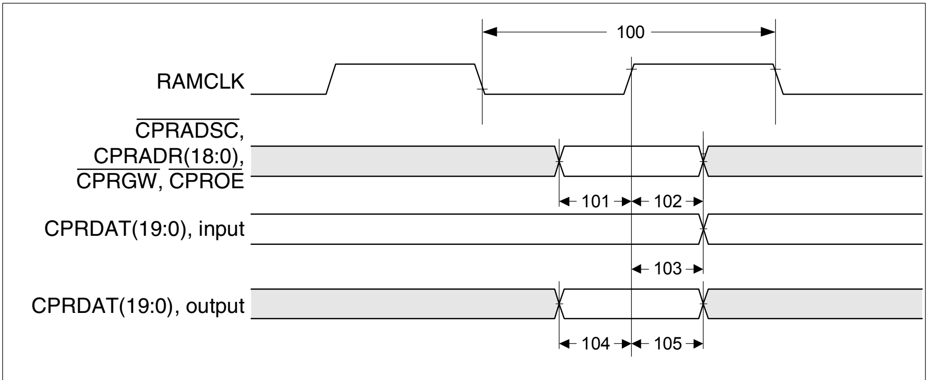


Figure 8-8 SSRAM Interface Generic Timing Diagram

Table 8-13 SSRAM Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
100	T_{RAMCLK}: Period RAMCLK	19.2			ns
100A	F_{RAMCLK}: Frequency RAMCLK			52	MHz
101	Setup time $\overline{\text{CPRADSC}}$, CPRADR(18:0), $\overline{\text{CPRGW}}$, $\overline{\text{CPROE}}$ before RAMCLK rising	2.5			ns
102	Hold time $\overline{\text{CPRADSC}}$, CPRADR(18:0), $\overline{\text{CPRGW}}$, $\overline{\text{CPROE}}$ after RAMCLK rising	1.5			ns
103	Delay CPRDAT Output after RAMCLK rising	2.5		11	ns
104	Setup time CPRDAT Input before CLK rising (Read cycles)	2.5			ns
105	Hold time CPRDAT Input after CLK rising (Read cycles)	1.5			ns

8.4.5 CSR SDRAM Interface(s)

Timing of the Synchronous Dynamic RAM (SDRAM) Interface is simplified as all signals are referenced to the rising edge of RAMCLK. In **Figure 8-9**, it can be seen that all signals output by the ABM-3G have identical delay times with reference to the clock. When reading from RAM, the ABM-3G samples the data within a window at the rising clock edge.

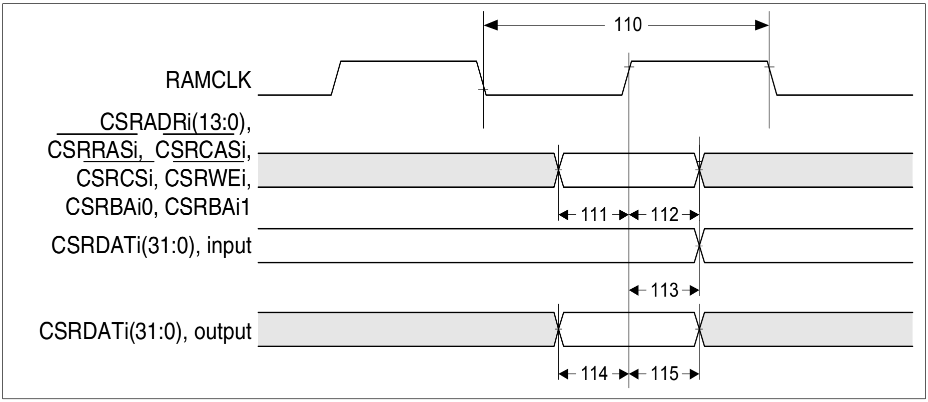


Figure 8-9 Generic SDRAM Interface Timing Diagram

Table 8-14 SDRAM Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
110	T_{RAMCLK}: Period RAMCLK	19.2			ns
110A	F_{RAMCLK}: Frequency RAMCLK			52	MHz
111	Setup time CSRADRi(13:0), CSRCSi, CSRRASi, CSRCASi, CSRWEi, CSRBAi0, CSRBAi1 before RAMCLK rising	2.5			ns
112	Hold time CSRADRi(13:0), CSRCSi, CSRRASi, CSRCASi, CSRWEi, CSRBAi0, CSRBAi1 after RAMCLK rising	1.5			ns
113	Delay CSRDATi Output after RAMCLK rising	3		6.5	ns

Table 8-14 SDRAM Interface AC Timing Characteristics (cont'd)

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
114	Setup time CSRDATi Input before RAMCLK rising (Read cycles)	2.5			ns
115	Hold time CSRDATi Input after RAMCLK rising (Read cycles)	1.5			ns

8.4.6 Reset Timing

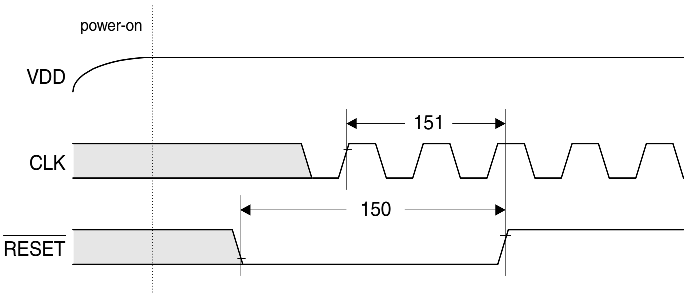


Figure 8-10 Reset Timing

Table 8-15 Reset Timing

No.	Parameter	Limit Values		Unit
		min.	**max.**	
150	RESET pulse width	120		ns
151	Number of SYSCLK cycles during $\overline{\text{RESET}}$ active	2		SYSCLK cycles

Note: $\overline{\text{RESET}}$ may be asynchronous to CLK when asserted or deasserted. $\overline{\text{RESET}}$ may be asserted during power-up or asserted after power-up. Nevertheless, deassertion must be at a clean, bounce-free edge.

8.4.7 Boundary-Scan Test Interface

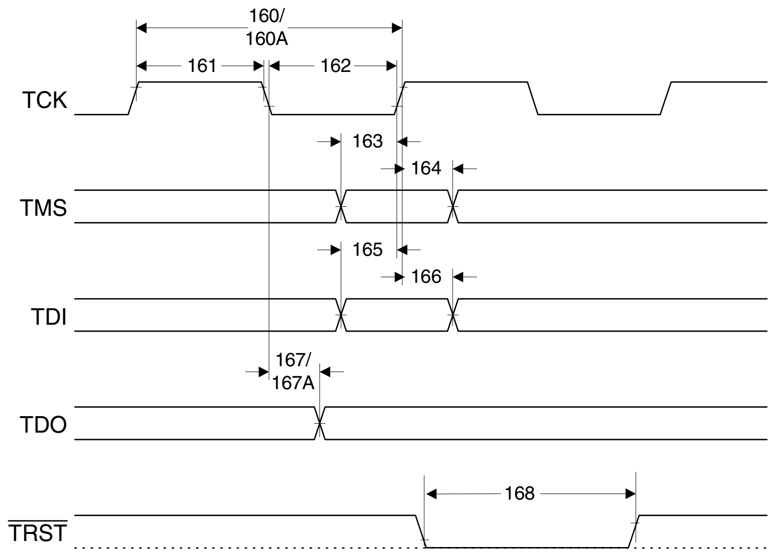


Figure 8-11 Boundary-Scan Test Interface Timing Diagram

Table 8-16 Boundary-Scan Test Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
160	T_{TCK}: Period TCK	100			ns
160A	F_{TCK}: Frequency TCK			10	MHz
161	TCK high time	40			ns
162	TCK low time	40			ns
163	Setup time TMS before TCK rising	10			ns
164	Hold time TMS after TCK rising	10			ns
165	Setup time TDI before TCK rising	10			ns
166	Hold time TDI after TCK rising	10			ns
167	Delay TCK falling to TDO valid			30	ns
167A	Delay TCK falling to TDO high impedance			30	ns
168	Pulse width $\overline{TRST}$ low	200			ns

8.5 Capacitances

Table 8-17 Capacitances

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input Capacitance	C_{IN}	2.5	5	pF
Output Capacitance	C_{OUT}	2	5	pF
Load Capacitance at:				
UTOPIA Outputs	C_{FO1}		40	pF
MPDAT(15:0), MPRDY	C_{FO2}		50	pF
other outputs	C_{FO3}		20	pF

8.6 Package Characteristics

Table 8-18 Thermal Package Characteristics

Parameter		Symbol	Value	Unit
Thermal Package Resistance Junction to Ambient				
Airflow	Ambient Temperature			
No airflow	T_A=25°C	$R_{JA(0,25)}$	21,1	°C/W
Airflow 200 lfpm = 1 m/s	T_A=25°C	$R_{JA(0,25)}$	17,7	°C/W
Airflow 500 lfpm = 2.5 m/s	T_A=25°C	$R_{JA(0,25)}$	16,3	°C/W

9 Test Mode

A Test Access Port (TAP) is implemented in the ABM-3G. The essential part of the TAP is a finite state machine (16 states) controlling the different operational modes of the boundary scan. Both the TAP controller and boundary scan meet the requirements given by the JTAG standard: IEEE 1149.1. **Figure 9-1** gives an overview about the TAP controller.

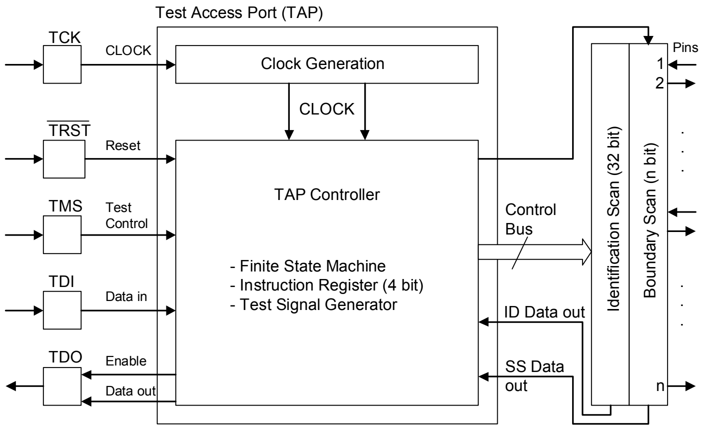


Figure 9-1 Block Diagram of Test Access Port and Boundary Scan Unit

If no boundary scan operation is planned, $\overline{\text{TRST}}$ must be connected with V_{SS}. TMS and TDI do not need to be connected since pull-up transistors ensure high input levels in this case. Nevertheless, it is good practice to set the unused inputs to defined levels.
In this case, if the JTAG is not used:
TMS = TCK = ‘1’ is recommended.

Test handling (boundary scan operation) is performed via the pins TCK (Test Clock), TMS (Test Mode Select), TDI (Test Data Input), and TDO (Test Data Output) when the TAP controller is not in its reset state; i.e., $\overline{\text{TRST}}$ is connected to V_{DD3} or it remains unconnected due to its internal pull up. Test data at TDI are loaded with a clock signal connected to TCK. ‘1’ or ‘0’ on TMS causes a transition from one controller state to another; constant ‘1’ on TMS leads to normal operation of the chip.

An Input pin (I) uses one boundary scan cell (data in); an Output pin (O) uses two cells (data out, enable); and an I/O-pin (I/O) uses three cells (data in, data out, enable). Note that most functional output and input pins of the ABM-3G are tested as I/O pins in boundary scan, thus using three cells. The boundary scan unit of the ABM-3G contains a total of n = 572 scan cells. The desired test mode is selected by serially loading a 4-bit instruction code into the instruction register via TDI (LSB first).

EXTEST is used to examine the interconnection of the devices on the board. In this test mode, at first all input pins capture the current level on the corresponding external interconnection line, whereas all output pins are held at constant values ('0' or '1'). Then, the contents of the boundary scan are shifted to TDO. At the same time the next scan vector is loaded from TDI. Subsequently all output pins are updated according to the new boundary scan contents and all input pins again capture the current external level afterwards, and so on.

INTEST supports internal testing of the chip; i.e., the output pins capture the current level on the corresponding internal line whereas all input pins are held on constant values ('0' or '1'). The resulting boundary scan vector is shifted to TDO. The next test vector is serially loaded via TDI. Then, all input pins are updated for the following test cycle.

SAMPLE/PRELOAD is a test mode which provides a snapshot of pin levels during normal operation.

IDCODE: A 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to '1'.

Standard Mode

The ID code field is set to:

Version : 1_H

Part Number : $07F0_H$

Manufacturer : 083_H (including LSB, which is fixed to '1')

Alternate Mode

The ID code field is set to

Version : 1_H

Part Number : $07F0_H$

Manufacturer : 083_H (including LSB, which is fixed to '1')

Note: Since in test logic reset state the code '0011' is automatically loaded into the instruction register, the ID code can easily be read out in shift DR state.

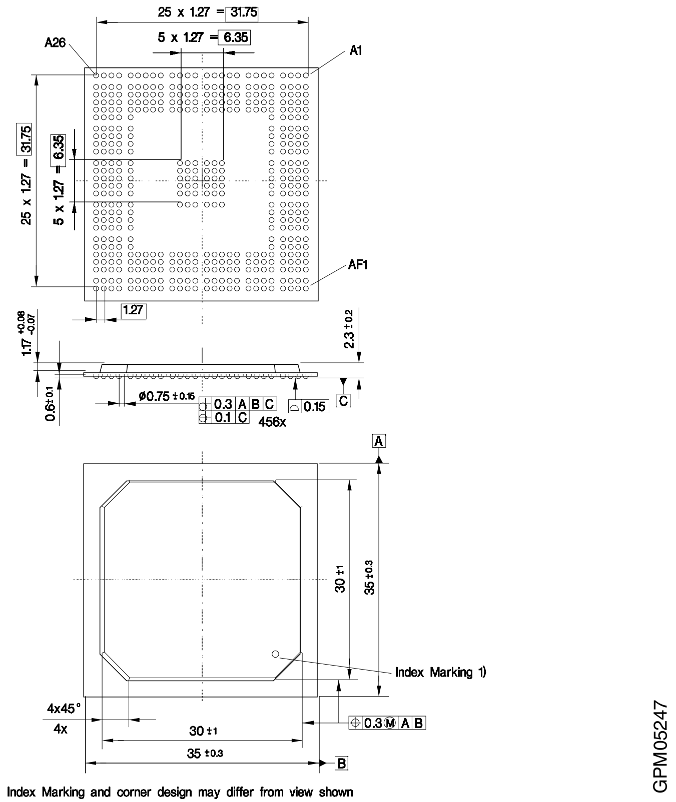
BYPASS: A bit entering TDI is shifted to TDO after one TCK clock cycle.

CLAMP allows the state of signals driven from component pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. Signals driven from the ABM-3G will not change while the CLAMP instruction is selected.

HIGHZ places all of the system outputs in an inactive drive state.

10 Package Outlines

P-BGA-456
(Plastic Ball Grid Array Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

11 Glossary

AAL	**A**TM **A**daptation **L**ayer
ABM	**A**TM **B**uffer **M**anager device, PXB 4330E
ABM-3G	**A**TM **B**uffer **M**anager device, PXF 4333
ABR	**A**vailable **B**it **R**ate
ALP	**A**TM **L**ayer **P**rocessor device, PXB 4350 E
AOP	**A**TM **O**AM **P**rocessor device, PXB 4340 E
ATM	**A**synchronous **T**ransfer **M**ode
BIST	**B**uilt-**I**n **S**elf **T**est
CAC	**C**onnection **A**cceptance **C**ontrol
CAME	**C**ontent **A**ddressable **M**emory **E**lement device, PXB 4360 E
CBR	**C**onstant **B**it **R**ate
CDV	**C**ell **D**elay **V**ariation
CLP	**C**ell **L**oss **P**riority of standardized ATM cell
CRC	**C**yclic **R**edundancy **C**heck
DSLAM	**D**igital **S**ubscriber **L**ine **A**ccess **M**ultiplexer
dword	double word (32 bits)
EPD	**E**arly **P**acket **D**iscard
FIFO	**F**irst-**I**n-**F**irst-**O**ut buffer
GFR	**G**uaranteed **F**rame **R**ate
I/O	**I**nput/**O**utput
ITU-T	**I**nternational **T**elecommunications **U**nion—**T**elecommunications standardization sector
LCI	**L**ocal **C**onnection **I**dentifier
LIC	**L**ine **I**nterface **C**ard or **L**ine **I**nterface **C**ircuit
LIFO	**L**ast-**I**n-**F**irst-**O**ut buffer
LSB	**L**east **S**ignificant **B**it
MBS	**M**aximum **B**urst **S**ize
MCR	**M**inimum **C**ell **R**ate
MSB	**M**ost **S**ignificant **B**it
OAM	**O**peration **A**nd **M**aintenance
PCR	**P**eak **C**ell **R**ate

PHY	**PHY**sical Line Port
PPD	**P**artial **P**acket **D**iscard
PTI	**P**ayload **T**ype **I**ndication field of standardized ATM cell
QID	**Q**ueue **ID**entifier
QoS	**Q**uality **o**f **S**ervice
RAM	**R**andom **A**ccess **M**emory
SCR	**S**ustainable **C**ell **R**ate
SDRAM	**S**ynchronous **D**ynamic **R**andom **A**ccess **M**emory
SID	**S**cheduler **ID**entifier
SSRAM	**S**ynchronous **S**tatic **R**andom **A**ccess **M**emory
TM	**T**raffic **M**anagement
UBR	**U**nspecified **B**it **R**ate
UTOPIA	**U**niversal **T**est and **OP**eration **I**nterface for **A**TM
VBR-nrt	**V**ariable **B**it **R**ate - **n**on **r**eal **t**ime
VBR-rt	**V**ariable **B**it **R**ate - **r**eal **t**ime
VC-	**V**irtual **C**hannel specific
VCC	**V**irtual **C**hannel **C**onnection
VCI	**V**irtual **C**hannel **I**dentifier of standardized ATM cell
VP-	**V**irtual **P**ath specific
VPC	**V**irtual **P**ath **C**onnection
VPI	**V**irtual **P**ath **I**dentifier of standardized ATM cell
WFQ	**W**eighted **F**air **Q**ueueing
word	16 bits

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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

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