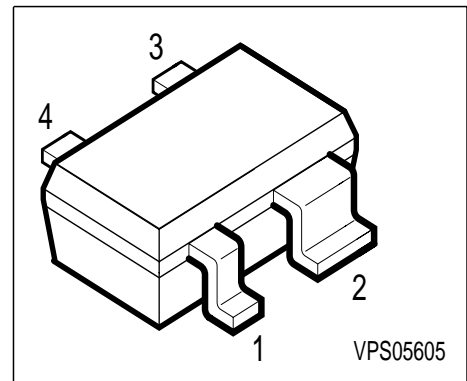


### Silicon N Channel MOSFET Tetrode

#### Target data sheet

- Short-channel transistor with high S/C quality factor
- For low-noise, gain-controlled input stages up to 1 GHz



Type	Marking	Ordering Code	Pin Configuration				Package
BF 2000W	NDs	Q62702-F1772	1 = D	2 = S	3 = G1	4 = G2	SOT-343

#### Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	$V_{DS}$	12	V
Continuous drain current	$I_D$	30	mA
Gate 1/gate 2 peak source current	$\pm I_{G1/2SM}$	10	
Total power dissipation, $T_S = 76^\circ\text{C}$	$P_{tot}$	200	mW
Storage temperature	$T_{stg}$	- 55 ... +150	°C
Channel temperature	$T_{ch}$	150	

#### Thermal Resistance

Channel - soldering point	$R_{thchs}$	$\leq 280$	K/W
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**Electrical Characteristics** at  $T_A = 25\text{ °C}$ ; unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>DC characteristics</b>					
Drain-source breakdown voltage $I_D = 10\text{ }\mu\text{A}$ , $-V_{G1S} = 4\text{ V}$ , $-V_{G2S} = 4\text{ V}$	$V_{(BR)DS}$	12	-	-	V
Gate 1 source breakdown voltage $\pm I_{G1S} = 10\text{ mA}$ , $V_{G2S} = V_{DS} = 0$	$\pm V_{(BR)G1SS}$	8	-	12	
Gate 2 source breakdown voltage $\pm I_{G2S} = 10\text{ mA}$ , $V_{G1S} = 0\text{ V}$ , $V_{DS} = 0\text{ V}$	$\pm V_{(BR)G2SS}$	8	-	12	
Gate 1 source leakage current $\pm V_{G1S} = 5\text{ V}$ , $V_{G2S} = V_{DS} = 0$	$\pm I_{G1SS}$	-	-	50	nA
Gate 2 source leakage current $\pm V_{G2S} = 5\text{ V}$ , $V_{G1S} = 0\text{ V}$ , $V_{DS} = 0\text{ V}$	$\pm I_{G2SS}$	-	-	50	
Drain current $V_{DS} = 5\text{ V}$ , $V_{G1S} = 0$ , $V_{G2S} = 4\text{ V}$	$I_{DSS}$	-	-	1	$\mu\text{A}$
Gate 1-source pinch-off voltage $V_{DS} = 5\text{ V}$ , $V_{G2S} = 4\text{ V}$ , $I_D = 200\text{ }\mu\text{A}$	$V_{G1S(p)}$	-	0.3	-	V
Gate 2-source pinch-off voltage $V_{DS} = 5\text{ V}$ , $I_D = 100\text{ }\mu\text{A}$	$V_{G2S(p)}$	-	0.2	-	

**Electrical Characteristics** at  $T_A = 25\text{ °C}$ , unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>AC characteristics</b>					
Forward transconductance $V_{DS} = 5\text{ V}$ , $I_D = 10\text{ mA}$ , $V_{G2S} = 4\text{ V}$ , $f = 1\text{ kHz}$	$g_{fs}$	-	24	-	mS
Gate 1 input capacitance $V_{DS} = 5\text{ V}$ , $I_D = 10\text{ mA}$ , $V_{G2S} = 4\text{ V}$ , $f = 1\text{ MHz}$	$C_{g1ss}$	-	1.2	-	pF
Gate 2 input capacitance $V_{DS} = 5\text{ V}$ , $I_D = 10\text{ mA}$ , $V_{G2S} = 4\text{ V}$ , $f = 1\text{ MHz}$	$C_{g2ss}$	-	-	-	
Feedback capacitance $V_{DS} = 8\text{ V}$ , $I_D = 10\text{ mA}$ , $V_{G2S} = 4\text{ V}$ , $f = 1\text{ MHz}$	$C_{dg1}$	-	25	-	fF
Output capacitance $V_{DS} = 5\text{ V}$ , $I_D = 10\text{ mA}$ , $V_{G2S} = 4\text{ V}$ , $f = 1\text{ MHz}$	$C_{dss}$	-	0.8	-	pF
Power gain $V_{DS} = 5\text{ V}$ , $I_D = 10\text{ mA}$ , $V_{G2S} = 4\text{ V}$ , $f = 45\text{ MHz}$	$G_{ps}$	28	29	-	dB
Power gain $V_{DS} = 5\text{ V}$ , $I_D = 10\text{ mA}$ , $V_{G2S} = 4\text{ V}$ , $f = 800\text{ MHz}$	$G_{ps}$	-	22	-	
Noise figure $V_{DS} = 5\text{ V}$ , $I_D = 10\text{ mA}$ , $V_{G2S} = 4\text{ V}$ , $f = 45\text{ MHz}$	$F$	-	1.1	-	
Noise figure $V_{DS} = 5\text{ V}$ , $I_D = 10\text{ mA}$ , $V_{G2S} = 4\text{ V}$ , $f = 800\text{ MHz}$	$F$	-	1	-	
Gain control range $V_{DS} = 8\text{ V}$ , $V_{G2S} = 4 \dots -2\text{ V}$ , $f = 800\text{ MHz}$	$\Delta G_{ps}$	40	-	-	