

## 4M x 1-Bit Dynamic RAM Low Power 4M x 1-Bit Dynamic RAM

HYB 314100BJ/BJL -50/-60/-70

### Advanced Information

- 4 194 304 words by 1-bit organization
- 0 to 70 °C operating temperature
- Fast Page Mode Operation
- Performance:

		-50	-60	-70	
$t_{RAC}$	$\overline{RAS}$ access time	50	60	70	ns
$t_{CAC}$	$\overline{CAS}$ access time	13	15	20	ns
$t_{AA}$	Access time from address	25	30	35	ns
$t_{RC}$	Read/Write cycle time	95	110	130	ns
$t_{PC}$	Fast page mode cycle time	35	40	45	ns

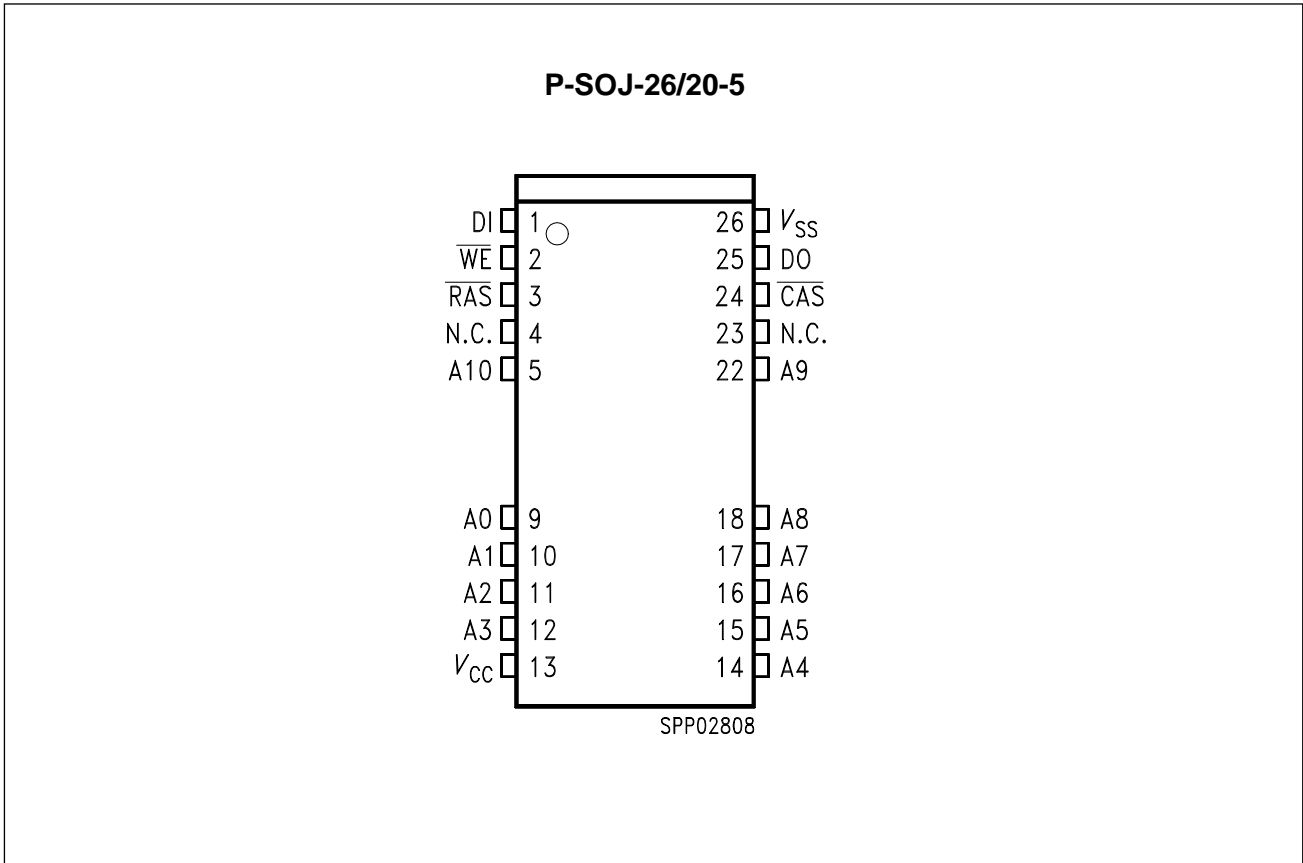
- Single + 3.3 V ( $\pm 0.3$  V ) supply with a built-in  $V_{bb}$  generator
- Low power dissipation  
max. 252 mW active (-50 version)  
max. 216 mW active (-60 version)  
max. 198 mW active (-70 version)
- Standby power dissipation:  
7.2 mW max. standby (TTL)  
3.6 mW max. standby (CMOS)  
720  $\mu$ W max. standby (CMOS) for Low Power Version
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify write,  $\overline{CAS}$ -before- $\overline{RAS}$  refresh,  $\overline{RAS}$ -only refresh, hidden refresh and test mode capability
- All inputs and outputs TTL-compatible
- 1024 refresh cycles / 16 ms
- 1024 refresh cycles / 128 ms Low Power Version
- Plastic Packages: P-SOJ-26/20-5 with 300 mil width

The HYB 314100BJ/BJL is the new generation dynamic RAM organized as 4 194 304 words by 1-bit. The HYB 314100BJ/BJL utilizes CMOS silicon gate process as well as advances circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514100BJ/BJL to be packed in a standard plastic P-SOJ-26/20 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include single + 3.3 V ( $\pm 0.3$  V) power supply, direct interfacing with high performance logic device families.

**Ordering Information**

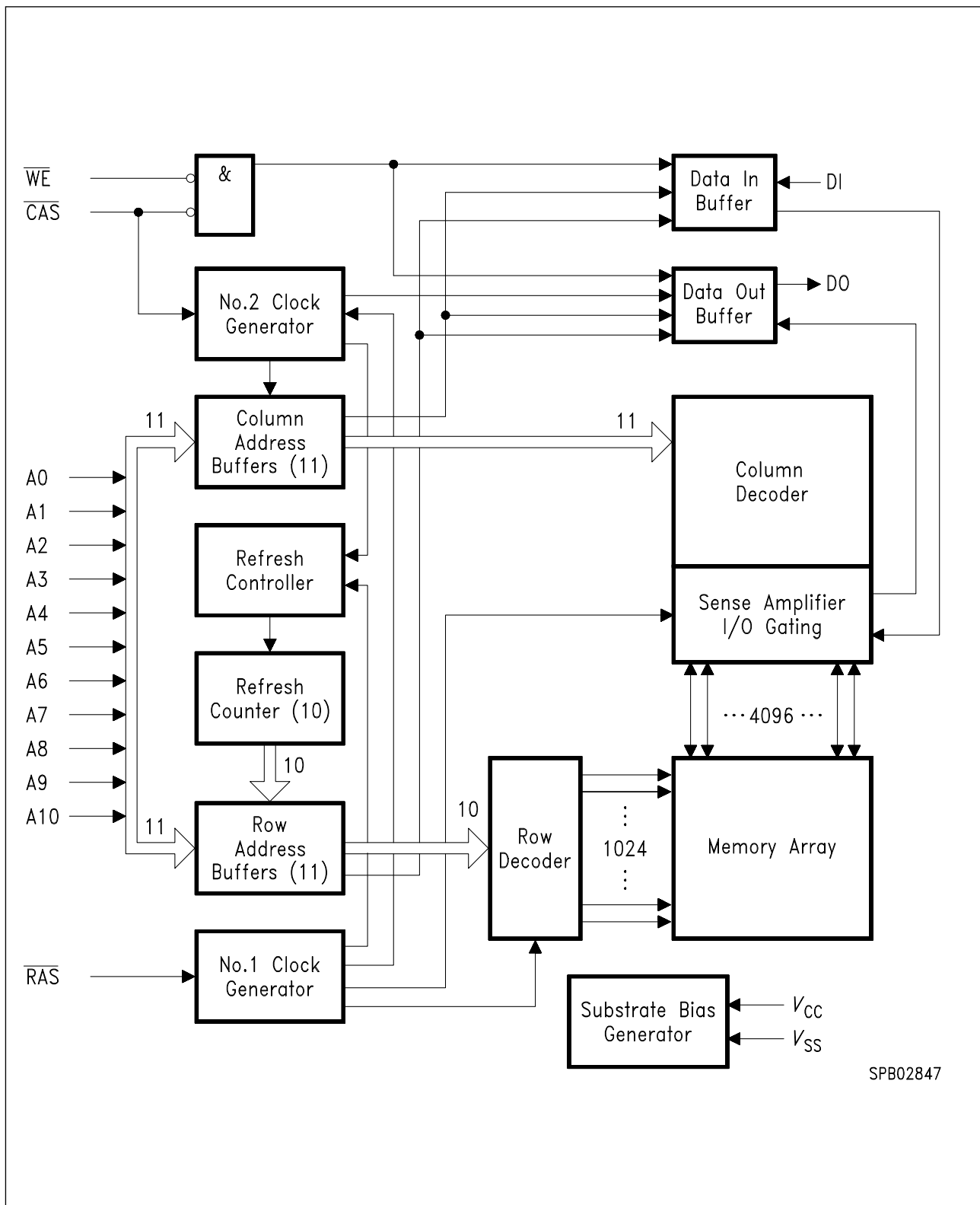
<b>Type</b>	<b>Ordering Code</b>	<b>Package</b>	<b>Descriptions</b>
HYB 314100BJ-50	Q67100-Q2035	P-SOJ-26/20-5	3.3 V DRAM (access time 50 ns)
HYB 314100BJ-60	Q67100-Q2037	P-SOJ-26/20-5	3.3 V DRAM (access time 60 ns)
HYB 314100BJ-70	Q67100-Q2039	P-SOJ-26/20-5	3.3 V DRAM (access time 70 ns)
HYB 314100BJL-50	on request	P-SOJ-26/20-5	3.3 V Low Power DRAM (access time 50 ns)
HYB 314100BJL-60	on request	P-SOJ-26/20-5	3.3 V Low Power DRAM (access time 60 ns)
HYB 314100BJL-70	on request	P-SOJ-26/20-5	3.3 V Low Power DRAM (access time 70 ns)

### Pin Configuration (top view)



### Pin Names

A0-A10	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read/Write Input
DI	Data In
DO	Data Out
$V_{\text{CC}}$	Power Supply (+ 3.3 V)
$V_{\text{SS}}$	Ground (0 V)
N.C.	No Connection



**Block Diagram**

### Absolute Maximum Ratings

Operating temperature range .....	0 to 70 °C
Storage temperature range.....	- 55 to + 150 °C
Input/output voltage .....	- 1 to + min ( $V_{CC} + 0.5$ , 4.6) V
Power Supply voltage .....	- 1 to + 4.6 V
Data out current (short circuit) .....	50 mA

**Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Characteristics

$T_A = 0$  to 70 °C,  $V_{SS} = 0$  V,  $V_{CC} = 3.3$  V  $\pm$  0.3 V,  $t_T = 5$  ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	$V_{IH}$	2.0	$V_{CC} + 0.5$	V	1)
Input low voltage	$V_{IL}$	- 1.0	0.8	V	1)
TTL Output high voltage ( $I_{OUT} = - 2$ mA)	$V_{OH}$	2.4	-	V	1)
TTL Output low voltage ( $I_{OUT} = 2$ mA)	$V_{OL}$	-	0.4	V	1)
CMOS Output high voltage ( $I_{OUT} = - 100$ $\mu$ A)	$V_{OH}$	$V_{CC} - 0.2$	-	V	
CMOS Output low voltage ( $I_{OUT} = 100$ $\mu$ A)	$V_{OL}$	-	0.2	V	
Input leakage current, any input ( $0$ V < $V_{in}$ < $V_{CC} + 0.3$ V, all other input = 0 V)	$I_{I(L)}$	- 10	10	$\mu$ A	1)
Output leakage current (DO is disabled, $0$ V < $V_{OUT}$ < $V_{CC}$ )	$I_{O(L)}$	- 10	10	$\mu$ A	1)
Average $V_{CC}$ supply current -50 version -60 version -70 version	$I_{CC1}$	-	70 60 55	mA	2) 3)4)
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{CAS} = \overline{WE} = V_{IH}$ )	$I_{CC2}$	-	2	mA	-
Average $V_{CC}$ supply current during $\overline{RAS}$ -only refresh cycles -50 version -60 version -70 version	$I_{CC3}$	-	70 60 55	mA	2)4)
Average $V_{CC}$ supply current during fast page mode operation -50 version -60 version -70 version	$I_{CC4}$	-	50 45 40	mA	2) 3)4)
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{CAS} = \overline{WE} = V_{CC} - 0.2$ V)	$I_{CC5}$	-	1 200	mA $\mu$ A	1) L-version

### DC Characteristics (cont'd)

$T_A = 0$  to  $70$  °C,  $V_{SS} = 0$  V,  $V_{CC} = 3.3$  V  $\pm$  0.3 V,  $t_T = 5$  ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average $V_{CC}$ supply current during $\overline{CAS}$ before $\overline{RAS}$ refresh mode -50 version -60 version -70 version	$I_{CC6}$	–	70 60 55	mA	2)4)
For Low Power Version only: Battery backup current (average power supply current in battery backup mode): ( $\overline{CAS} = \overline{CAS}$ before $\overline{RAS}$ cycling or 0.2 V, $\overline{WE} = V_{CC} - 0.2$ V or 0.2 V, A0 to A10 = $V_{CC} - 0.2$ V or 0.2 V; DI = $V_{CC} - 0.2$ V or 0.2 V or open, $t_{RC} = 125$ $\mu$ s, $t_{RAS} = t_{RAS}$ min = 1 $\mu$ s)	$I_{CC7}$	–	250	$\mu$ A	–

### Capacitance

$T_A = 0$  to  $70$  °C;  $V_{CC} = 3.3$  V  $\pm$  0.3 V;  $f = 1$  MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A10, DI)	$C_{I1}$	–	5	pF
Input capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ )	$C_{I2}$	–	7	pF
Output capacitance (DO)	$C_{I0}$	–	7	pF

### AC Characteristics <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3 V,  $t_T = 5$  ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		

### Common Parameters

Random read or write cycle time	$t_{RC}$	95	–	110	–	130	–	ns	
RAS precharge time	$t_{RP}$	35	–	40	–	50	–	ns	
RAS pulse width	$t_{RAS}$	50	10k	60	10k	70	10k	ns	
CAS pulse width	$t_{CAS}$	13	10k	15	10k	20	10k	ns	
Row address setup time	$t_{ASR}$	0	–	0	–	0	–	ns	
Row address hold time	$t_{RAH}$	8	–	10	–	10	–	ns	
Column address setup time	$t_{ASC}$	0	–	0	–	0	–	ns	
Column address hold time	$t_{CAH}$	10	–	15	–	15	–	ns	
RAS to CAS delay time	$t_{RCD}$	18	37	20	45	20	50	ns	
RAS to column address delay time	$t_{RAD}$	13	25	15	30	15	35	ns	
RAS hold time	$t_{RSH}$	13		15	–	20	–	ns	
CAS hold time	$t_{CSH}$	50		60	–	70	–	ns	
CAS to RAS precharge time	$t_{CRP}$	5	–	5	–	5	–	ns	
Transition time (rise and fall)	$t_T$	3	50	3	50	3	50	ns	7
Refresh period	$t_{REF}$	–	16	–	16	–	16	ms	
Refresh period for L-version	$t_{REF}$	–	128	–	128	–	128	ms	

### Read Cycle

Access time from RAS	$t_{RAC}$	–	50	–	60	–	70	ns	8, 9
Access time from CAS	$t_{CAC}$	–	13	–	15	–	20	ns	8, 9
Access time from column address	$t_{AA}$	–	25	–	30	–	35	ns	8,10
Column addr. to RAS lead time	$t_{RAL}$	25	–	30	–	35	–	ns	
Read command setup time	$t_{RCS}$	0	–	0	–	0	–	ns	
Read command hold time	$t_{RCH}$	0	–	0	–	0	–	ns	11
Read command hold time referenced to RAS	$t_{RRH}$	0	–	0	–	0	–	ns	11
CAS to output in low-Z	$t_{CLZ}$	0	–	0	–	0	–	ns	8

### AC Characteristics (cont'd) <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3 V,  $t_T = 5$  ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
Output buffer turn-off delay	$t_{OFF}$	0	13	0	15	0	20	ns	12

### Write Cycle

Write command hold time	$t_{WCH}$	8	–	10	–	10	–	ns	
Write command pulse width	$t_{WCP}$	8	–	10	–	10	–	ns	
Write command setup time	$t_{WCS}$	0	–	0	–	0	–	ns	13
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	13	–	15	–	20	–	ns	
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	13	–	15	–	20	–	ns	
Data setup time	$t_{DS}$	0	–	0	–	0	–	ns	14
Data hold time	$t_{DH}$	10	–	10	–	15	–	ns	14

### Read-Modify-Write Cycle

Read-write cycle time	$t_{RWC}$	115	–	130	–	155	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	50	–	60	–	70	–	ns	13
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	13	–	15	–	20	–	ns	13
Column address to $\overline{WE}$ delay time	$t_{AWD}$	25	–	30	–	35	–	ns	13

### Fast Page Mode Cycle

Fast page mode cycle time	$t_{PC}$	35	–	40	–	45	–	ns	
$\overline{CAS}$ precharge time	$t_{CP}$	10	–	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	$t_{CPA}$	–	30	–	35	–	40	ns	7
$\overline{RAS}$ pulse width	$t_{RAS}$	50	200 k	60	200 k	70	200 k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	$t_{RHCP}$	30	–	35	–	40	–	ns	



### AC Characteristics (cont'd) <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3 V,  $t_T = 5$  ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		

### **Fast Page Mode Read-Modify-Write Cycle**

Fast page mode read-write cycle time	$t_{PRWC}$	55	–	60	–	70	–	ns	
CAS precharge to $\overline{WE}$	$t_{CPWD}$	30	–	35	–	40	–	ns	

### **$\overline{CAS}$ -before- $\overline{RAS}$ refresh cycle**

$\overline{CAS}$ setup time	$t_{CSR}$	10	–	10	–	10	–	ns	
$\overline{CAS}$ hold time	$t_{CHR}$	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	$t_{RPC}$	5	–	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	$t_{WRP}$	10	–	10	–	10	–	ns	
Write hold time referenced to $\overline{RAS}$	$t_{WRH}$	10	–	10	–	10	–	ns	

### **$\overline{CAS}$ -before- $\overline{RAS}$ counter test cycle**

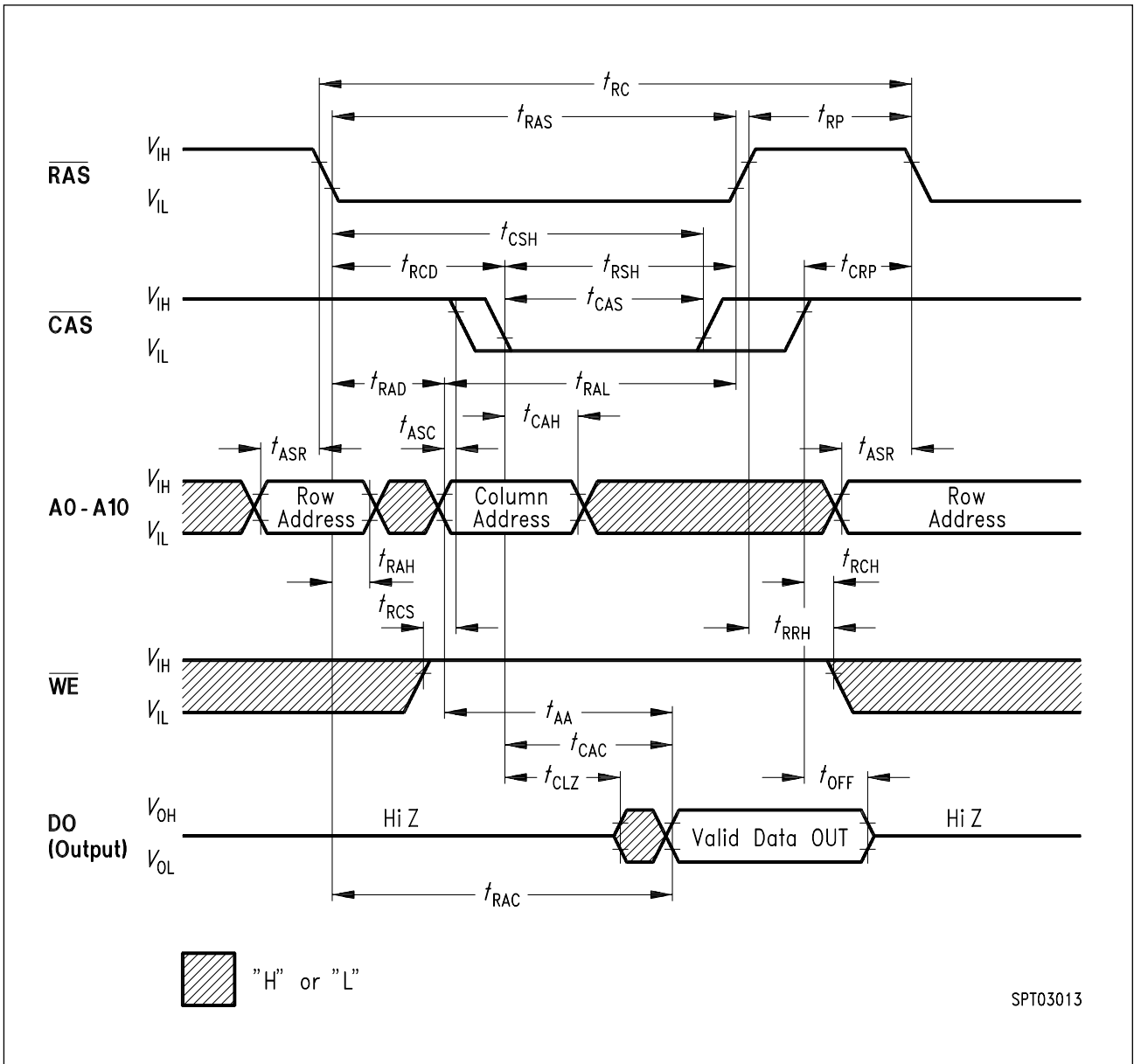
CAS precharge time	$t_{CPT}$	35	–	40	–	40	–	ns	
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### **Test Mode**

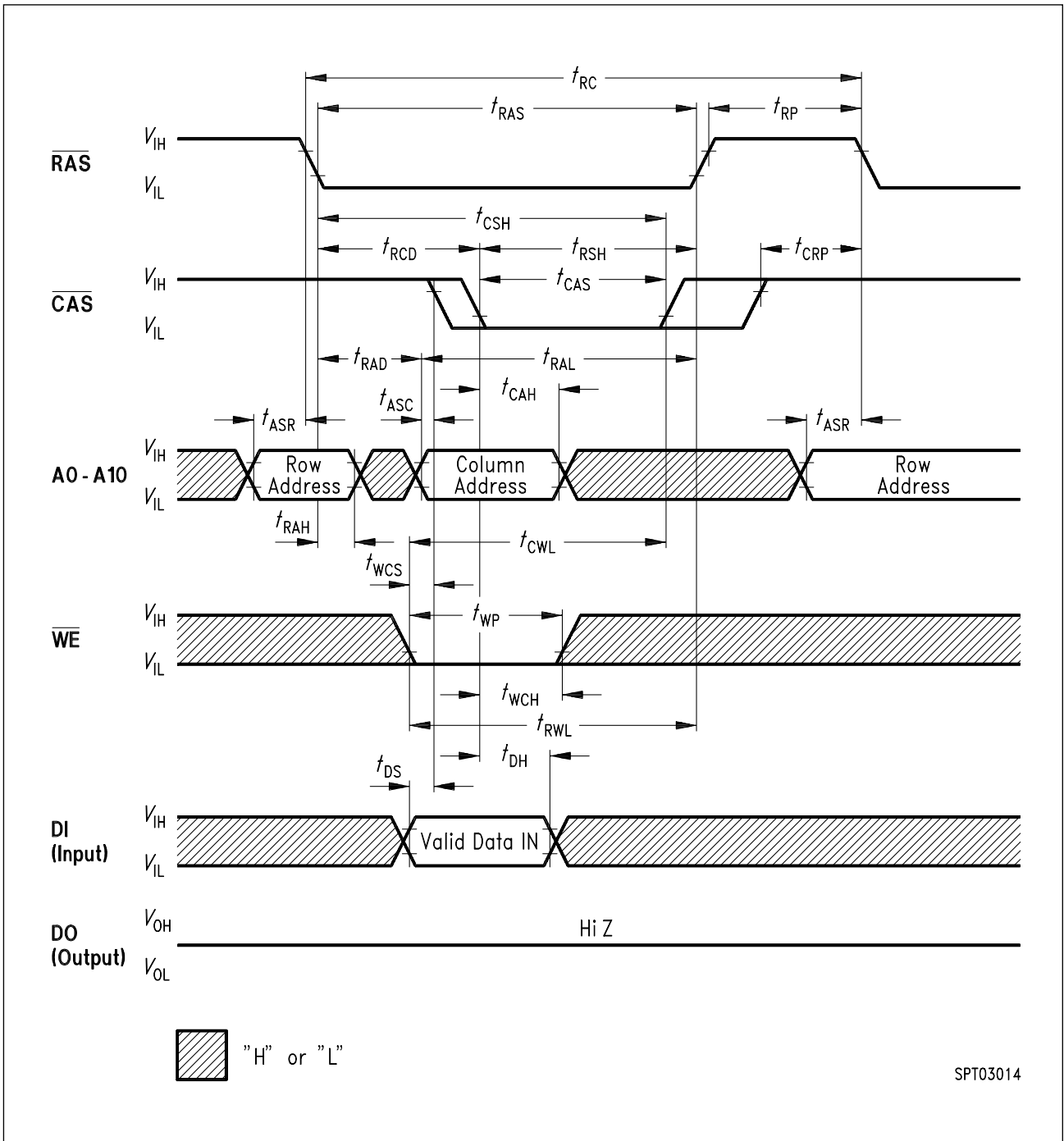
Write command setup time	$t_{WTS}$	10	–	10	–	10	–	ns	
Write command hold time	$t_{WTH}$	10	–	10	–	10	–	ns	

### Notes:

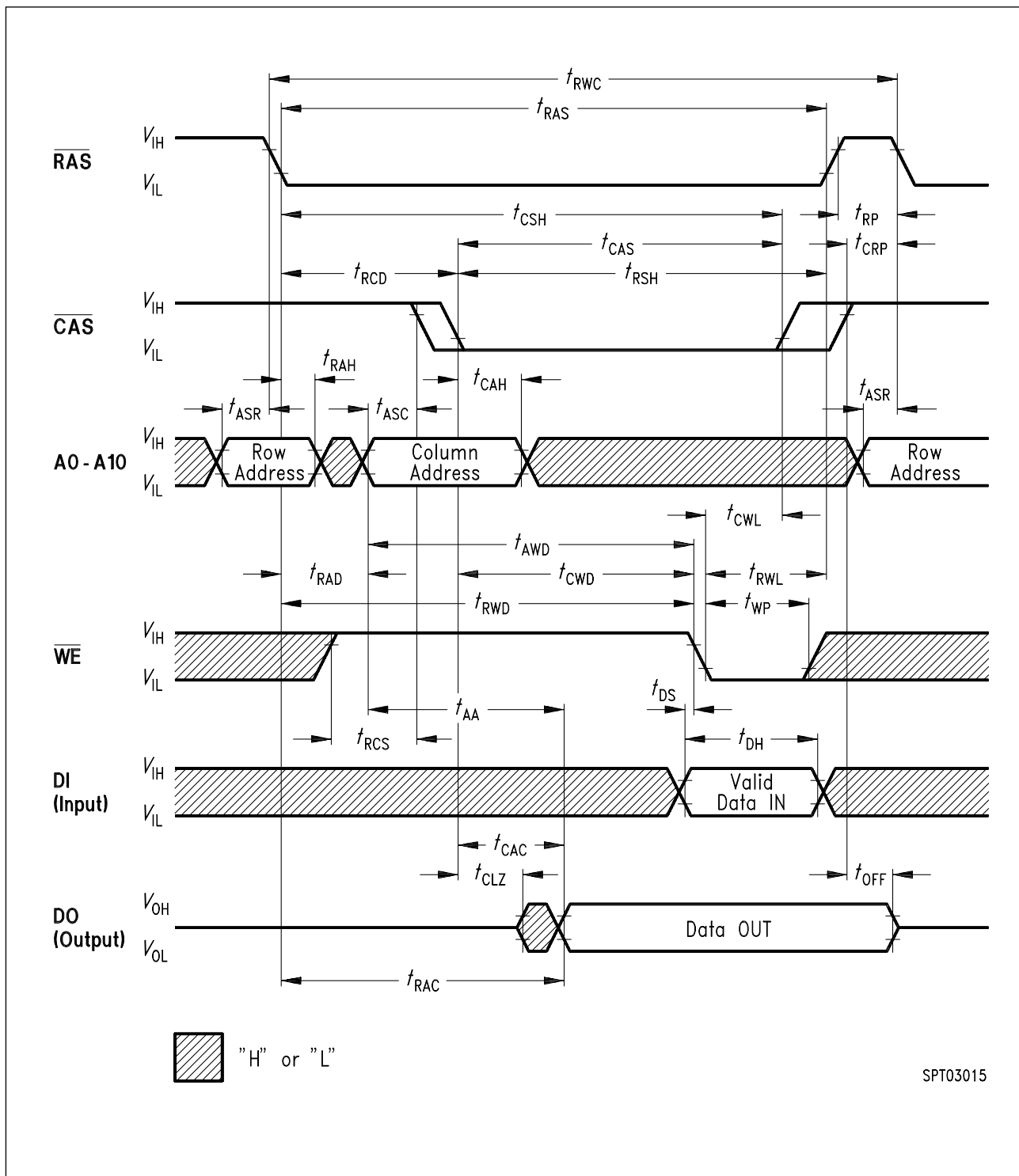
- 1) All voltages are referenced to  $V_{SS}$ .
- 2)  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on cycle rate.
- 3)  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are measured with the output open.
- 4) Address can be changed once or less while  $\overline{RAS} = V_{IL}$ . In the case of  $I_{CC4}$  it can be changed once or less during a fast page mode cycle ( $t_{PC}$ ).
- 5) An initial pause of 200  $\mu s$  is required after power-up followed by 8 RAS cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.
- 6) AC measurements assume  $t_T = 5$  ns.
- 7)  $V_{IH (min.)}$  and  $V_{IL (max.)}$  are reference levels for measuring timing of input signals. Transition times are also measured between  $V_{IH}$  and  $V_{IL}$ .
- 8) Measured with the specified current load and 100 pF at  $V_{OL} = 0.8$  and  $V_{OH} = 2.0$  V.
- 9) Operation within the  $t_{RCD (max.)}$  limit ensures that  $t_{RAC (max.)}$  can be met.  $t_{RCD (max.)}$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD (max.)}$  limit, then access time is controlled by  $t_{CAC}$ .
- 10) Operation within the  $t_{RAD (max.)}$  limit ensures that  $t_{RAC (max.)}$  can be met.  $t_{RAD (max.)}$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD (max.)}$  limit, then access time is controlled by  $t_{AA}$ .
- 11) Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- 12)  $t_{OFF (max.)}$  defines the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
- 13)  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} > t_{WCS (min.)}$ , the cycle is an early write cycle and the data out pin will remain open-circuit (high impedance) through the entire cycle; if  $t_{RWD} > t_{RWD (min.)}$ ,  $t_{CWD} > t_{CWD (min.)}$ ,  $t_{AWD} > t_{AWD (min.)}$  and  $t_{CPWD} > t_{CPWD (min.)}$ , the cycle is a read-write cycle and DO will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the DO pin (at access time) is indeterminate.
- 14) These parameters are referenced to the CAS leading edge in early write cycles and to the WE leading edge in read-write cycles.



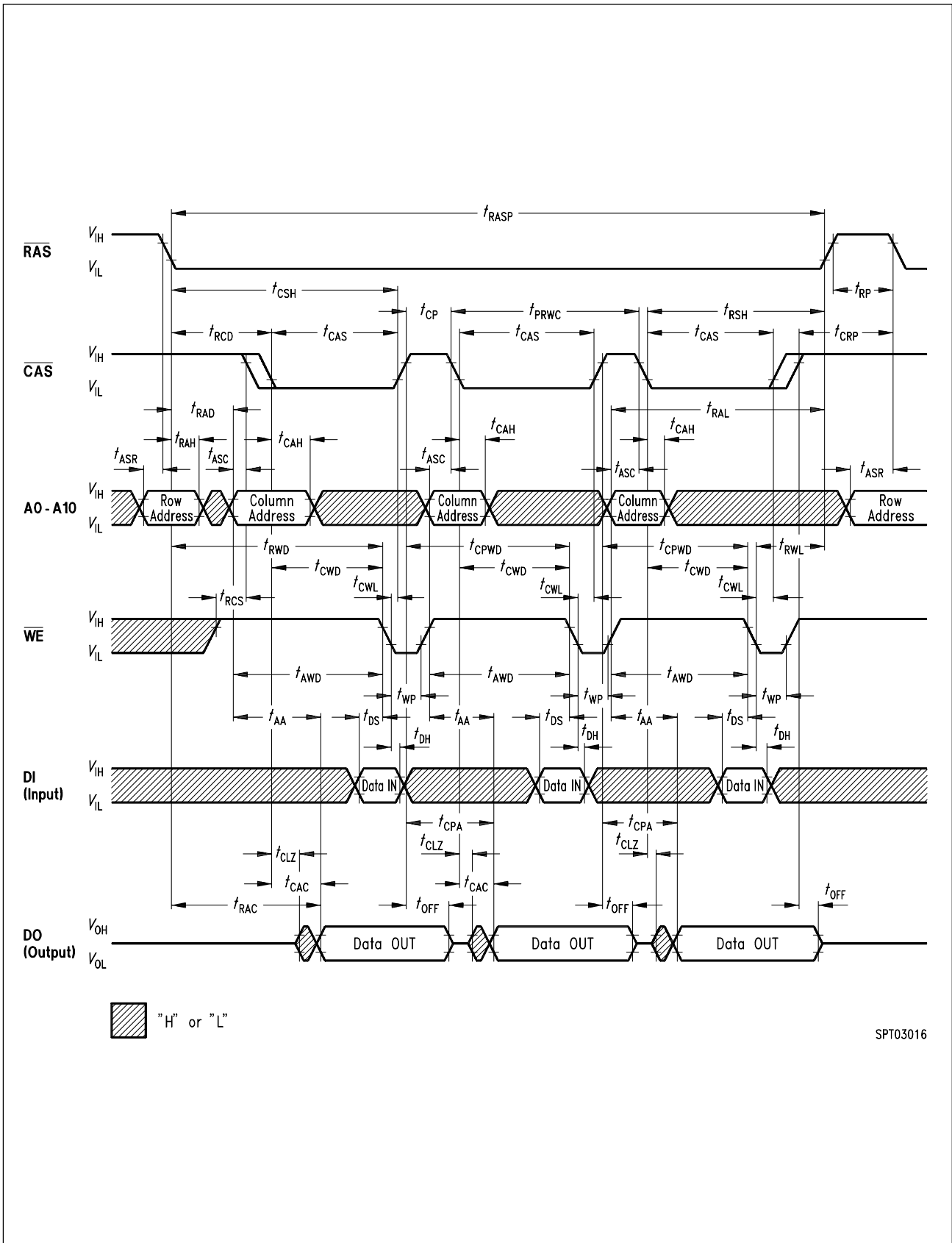
Read Cycle



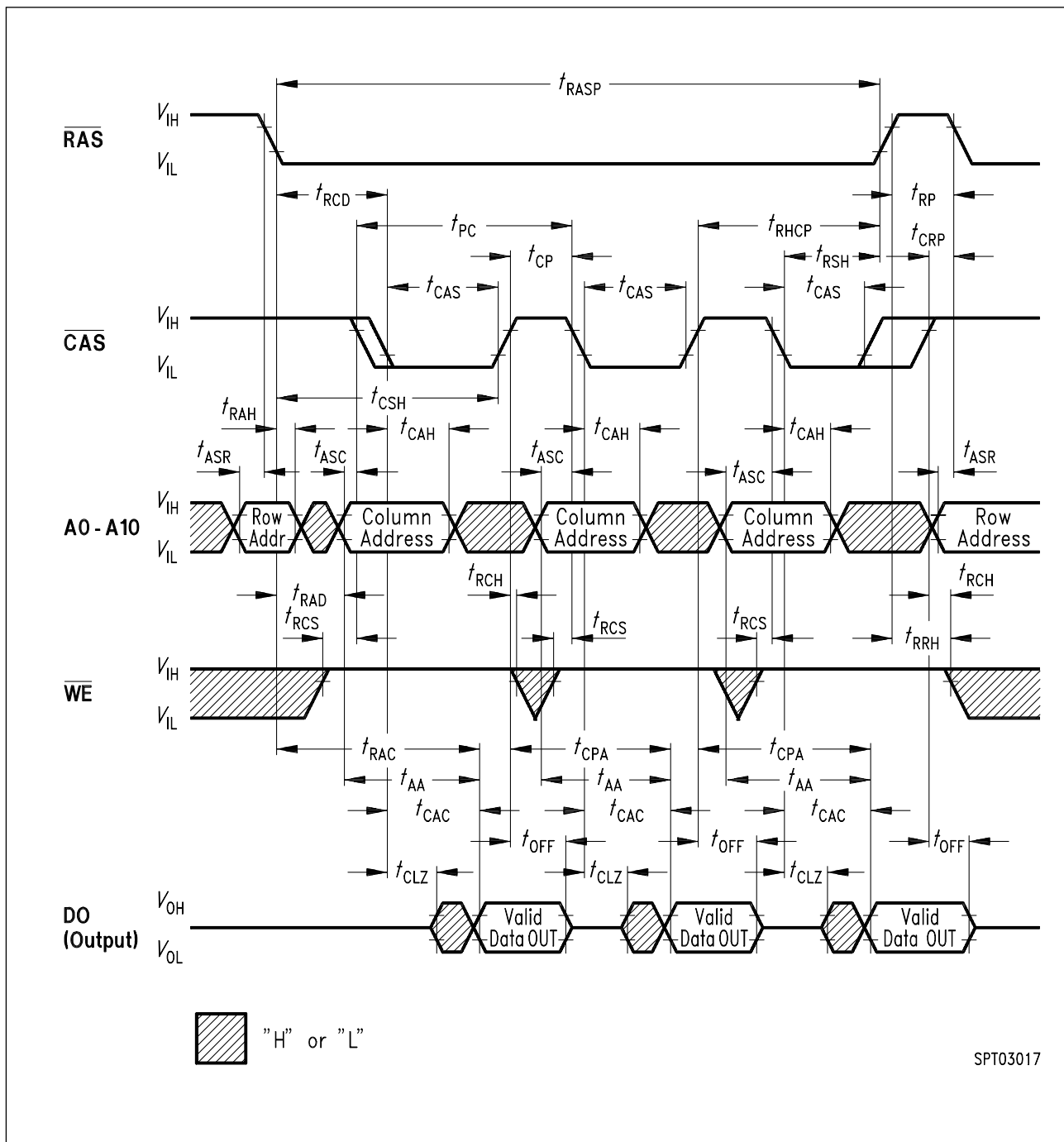
**Write Cycle (Early Write)**



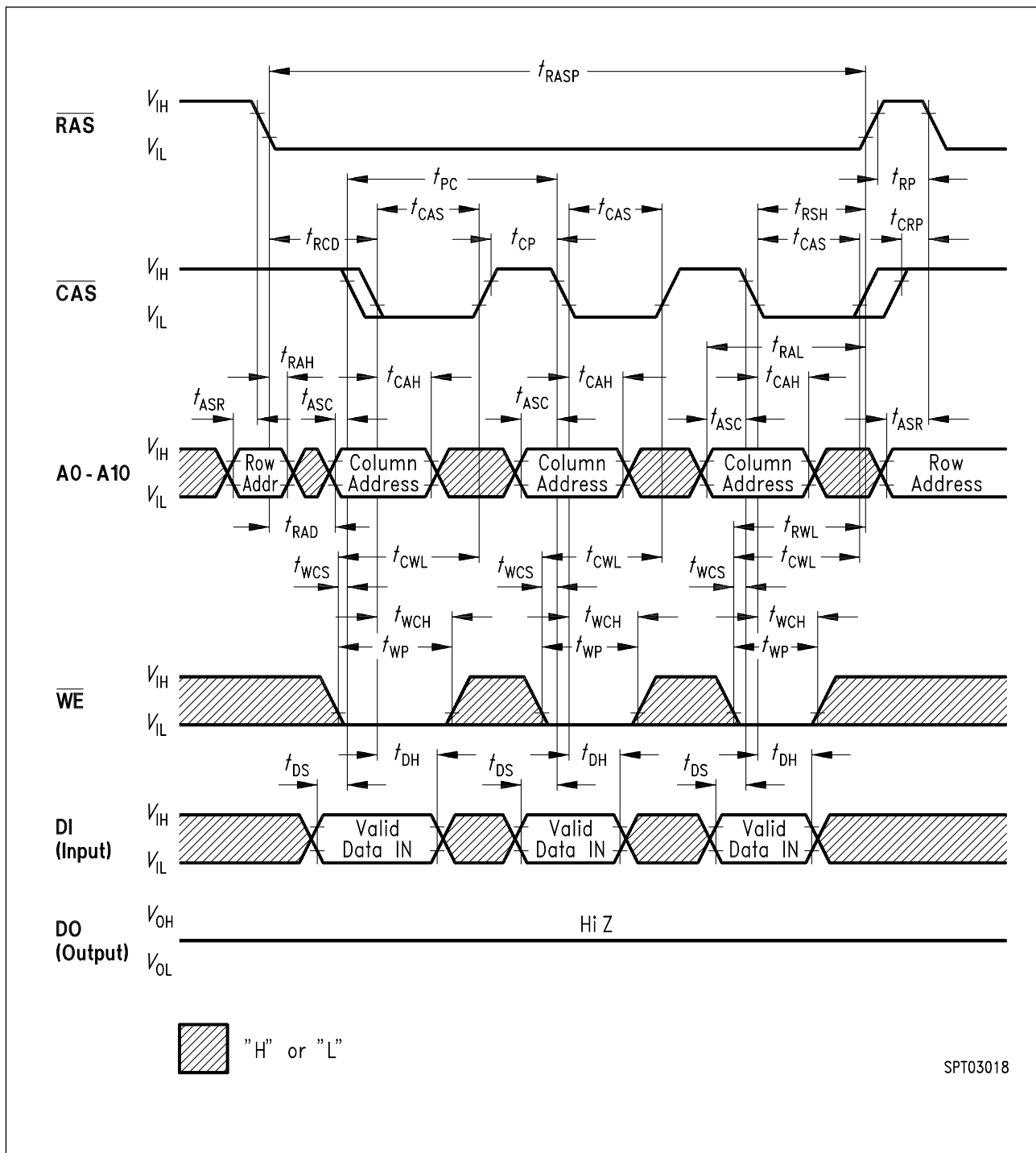
Read-Write (Read-Modify-Write) Cycle



**Fast Page Mode Read-Modify-Write Cycle**

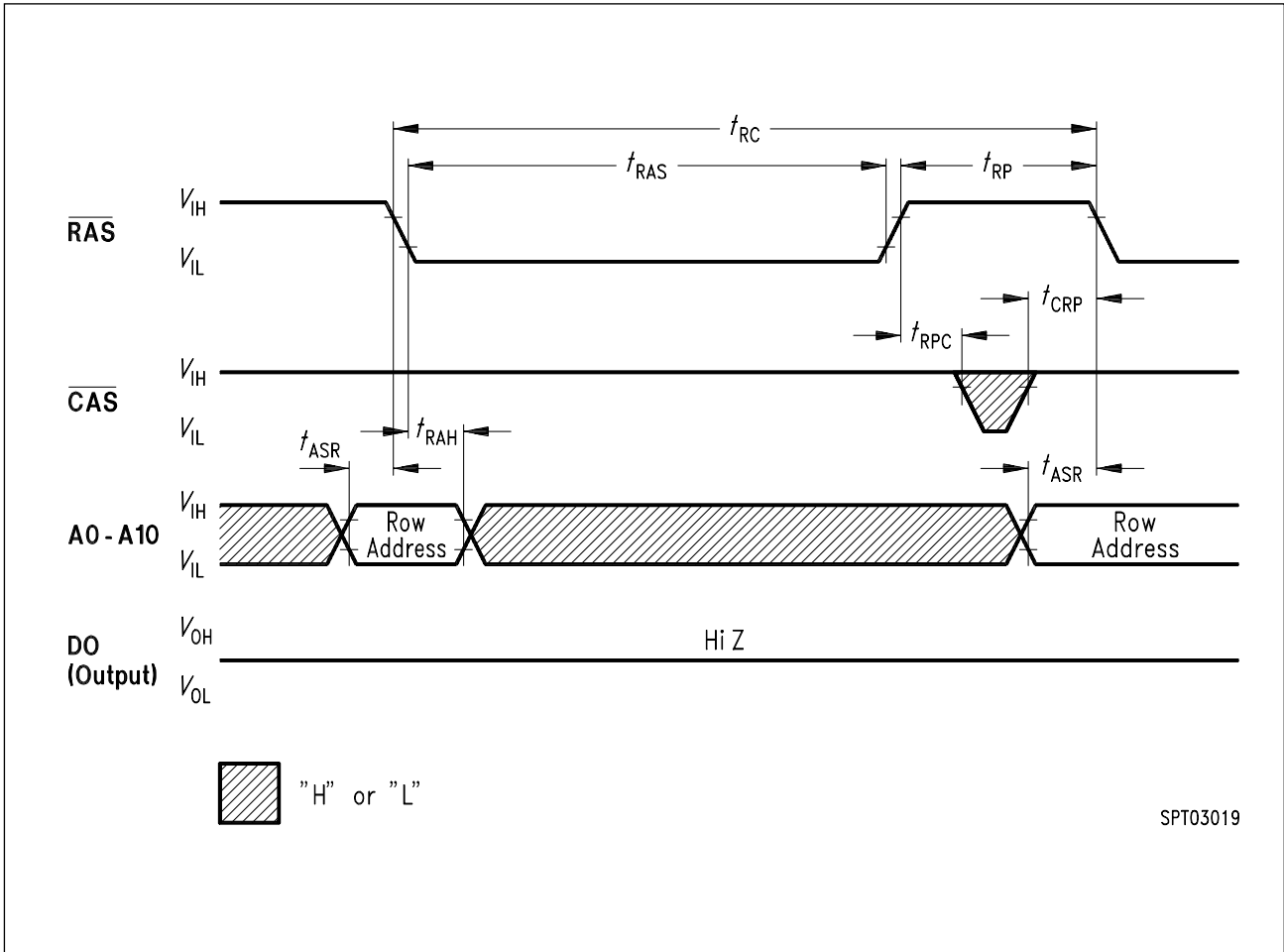


Fast Page Mode Read Cycle

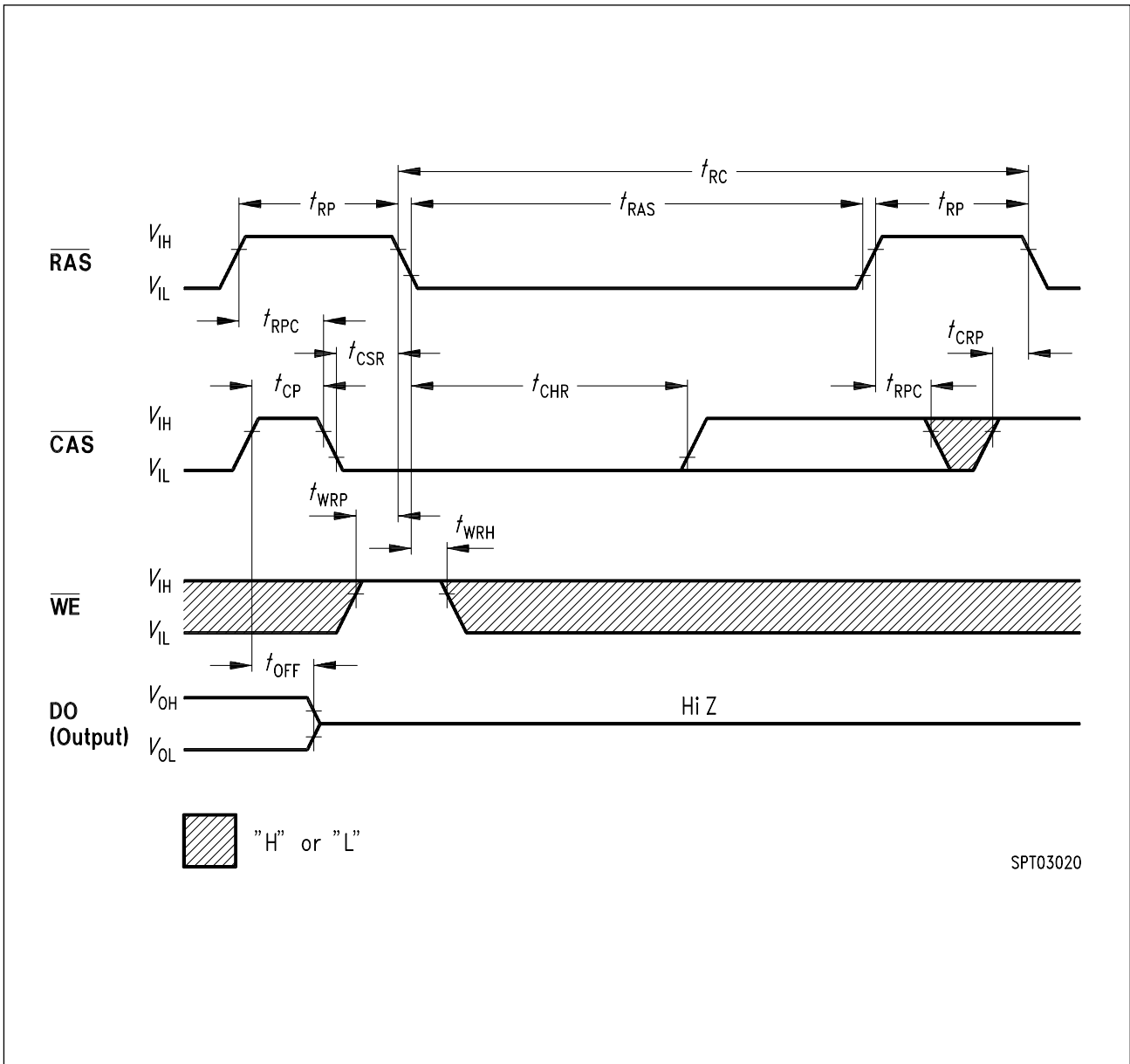


**Fast Page Mode Early Write Cycle**

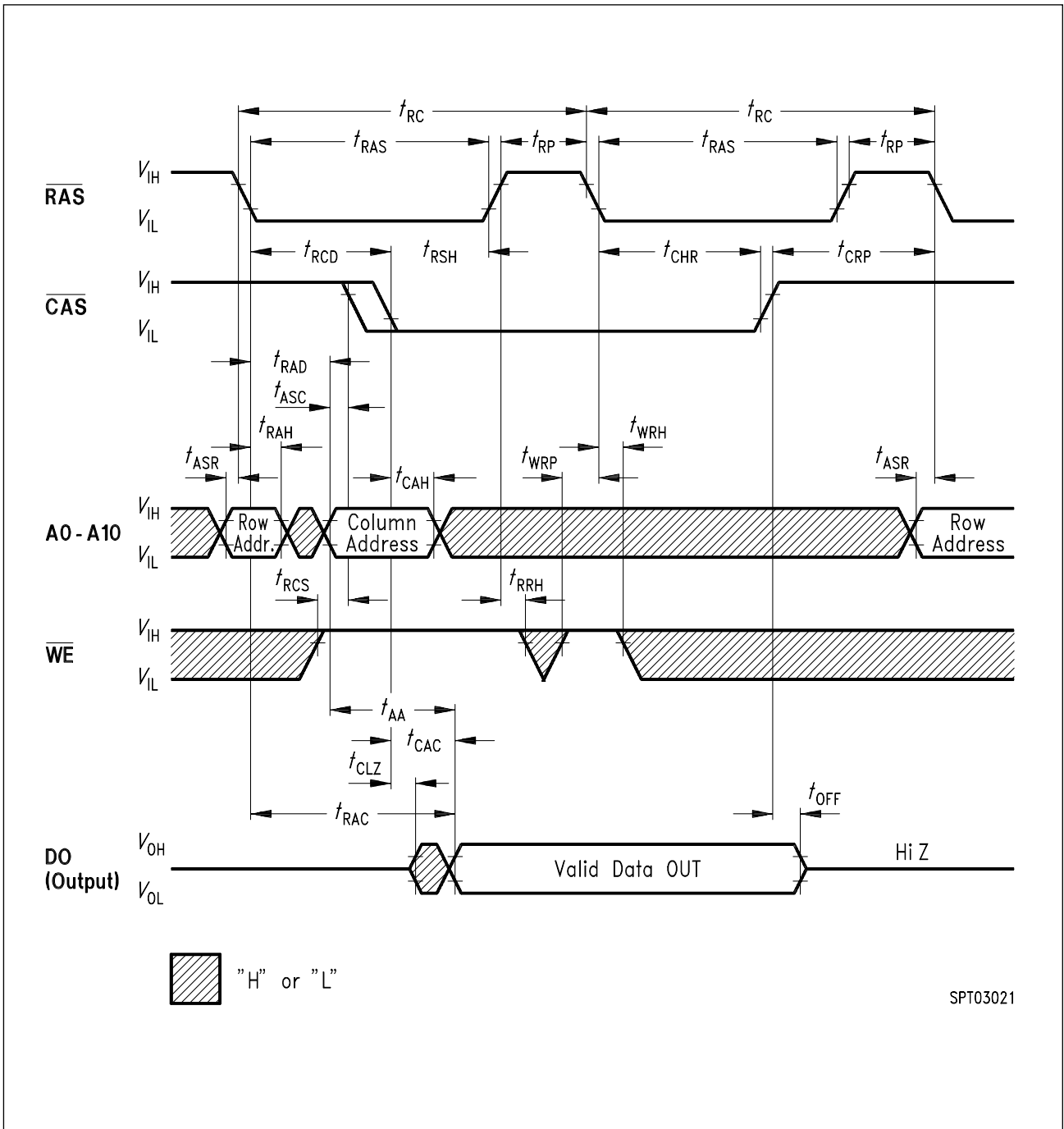




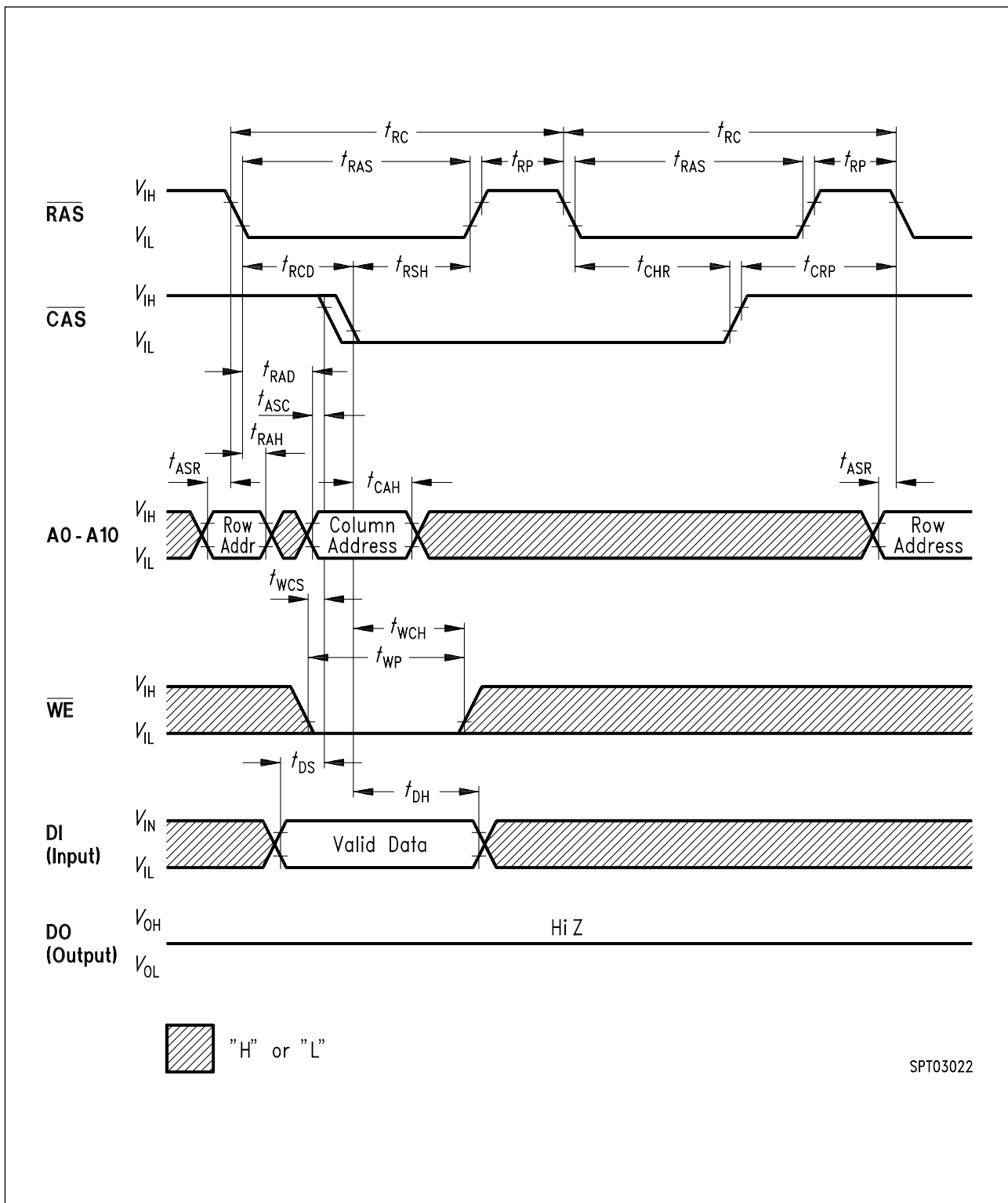
**RAS-Only Refresh Cycle**



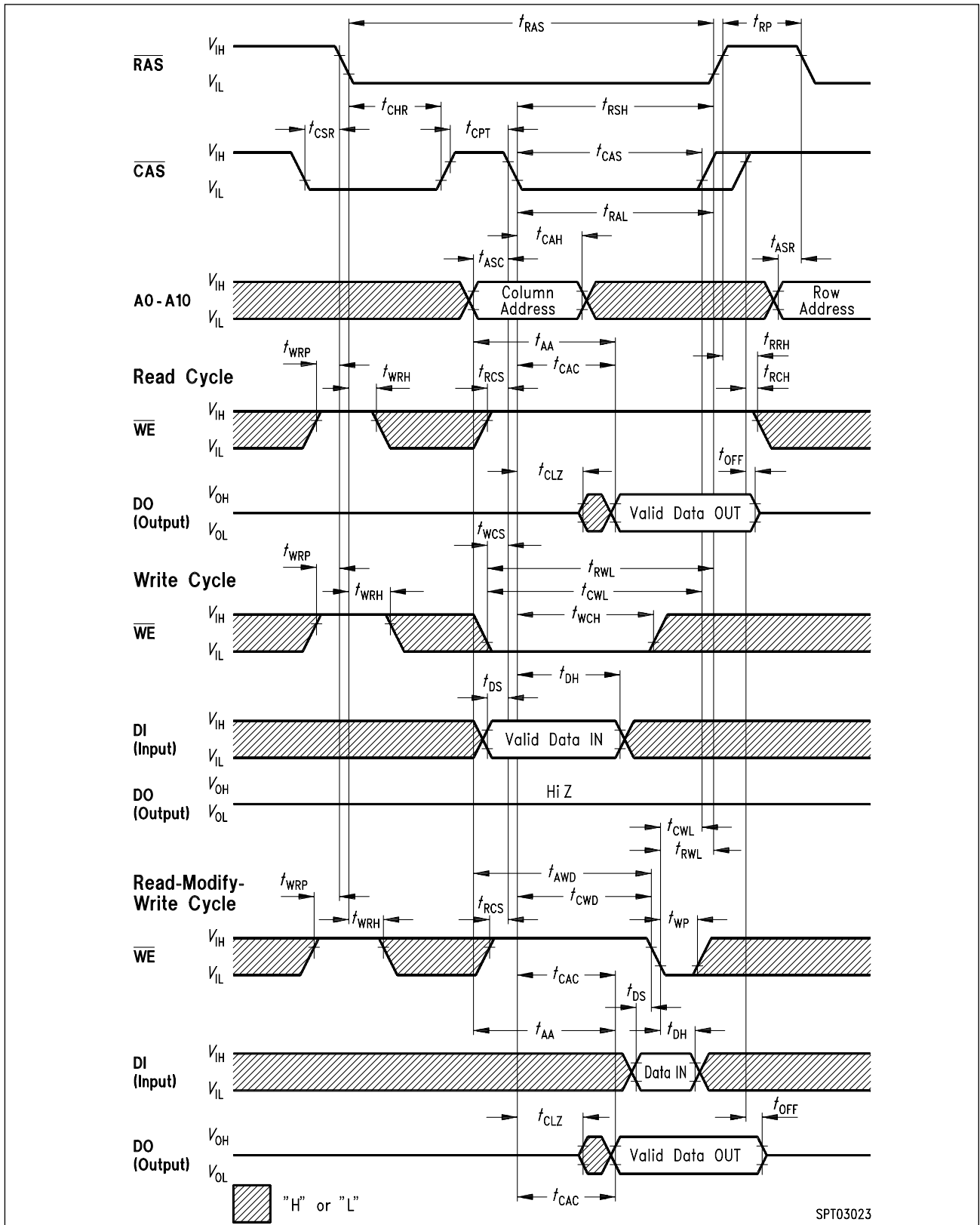
CAS-Before-RAS Refresh Cycle



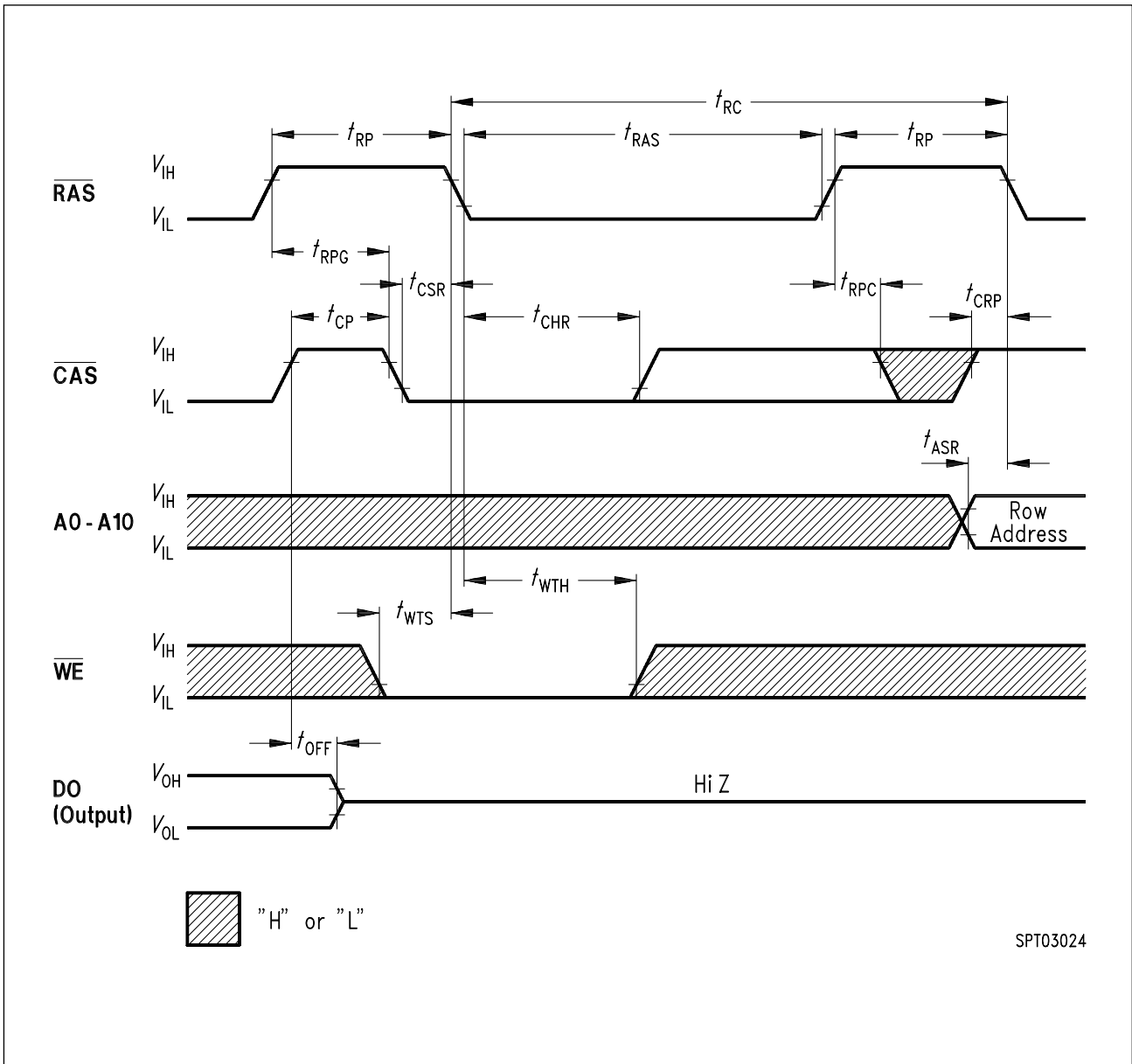
Hidden Refresh Cycle (Read)



**Hidden Refresh Cycle (Early Write)**



**CAS-Before-RAS Refresh Counter Test Cycle**



**Test Mode Entry**

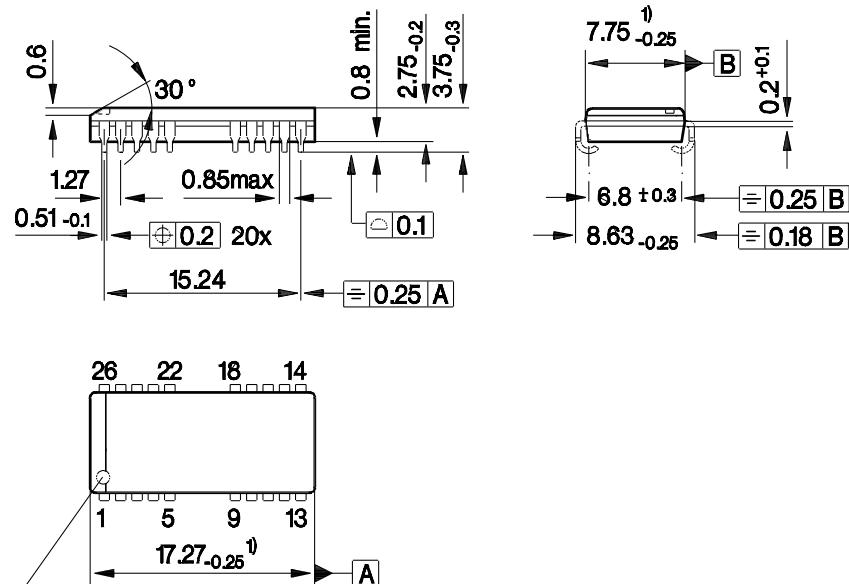
**Test Mode**

The HYB314100BJ/BJL is organized 4 194 304 words by 1-bit but can internally be configured as 524 288 words by 8-bits. A  $\overline{WE}$ ,  $\overline{CAS}$ -before- $\overline{RAS}$  cycle puts the device into Test Mode.

In Test Mode, data is written into 8 sectors in parallel and retrieved the same way. If, upon reading, all bits are equal, the data output pin indicates a "1". If any of the bits differ, the data output pin indicates a "0". In Test Mode the 4M DRAM can be tested as if it were a 512K DRAM. Test Mode is exited by any refresh operation which is not a  $\overline{WE}$ ,  $\overline{CAS}$ -before- $\overline{RAS}$  cycle. Addresses A10R, A10C and A0C do not care during Test Mode.

### Package Outlines

#### Plastic Package P-SOJ-26/20-5 (Plastic Small Outline J-leaded Package)



Index Marking

1) Does not include plastic or metal protrusion of 0.15 max. per side

GPJ05627

### Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm