Quatro® 4050

Driving the Digital Lifestyle

Programmable SOC Solution for Printers and All-in-Ones	Imaging	Software	Processors	Quatro SOCs	Solutions
		www.zoran.com			

Product Brief

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Based on Zoran's advanced Quatro architecture, the Quatro 4050 provides OEMs with a flexible and cost-effective platform for implementing ultra-low-cost AIO and photo printer controllers. Building upon Zoran's Quatro 4100 and 4110 solutions, the 4050 provides a new solution that integrates a scanner analog front-end (AFE), and enables the lowest

Benefits

Cost-effective solution

Highly integrated system-on-a-chip with both PC and non-PC interfaces, optimized for ultra-low-cost AIOs and photo printers, enabling the lowest possible cost

Rapid time-to-market

Programmable platform for rapidly deploying innovative features and associated image processing pipelines

High performance

Specialized imaging DSP core paired with high-performance ARM7 CPU core

Flexible connectivity

Optional WiFi and Bluetooth wireless connectivity

possible cost by focusing on a basic feature-set tailored for the new generation of ultra-low-cost AlOs and photo printers. With fully-programmable image processing based on the Quatro DSP, the Quatro 4050 is ideal for PictBridge-capable AlOs, inkjet photo printers and dye-sub photo printers.

Key Features

- · 67 MHz ARM7 CPU core
- · 133 MHz Quatro 4-datapath SIMD DSP core
- · 133 MHz JPEG assist module
- · Integrated 16-bit scanner AFE
- · USB Full-Speed device interface
- · USB Full-Speed host interface
- Programmable printer and scanner mechanism control interface with 133 MHz 8-bit flexRISC processor
- Programmable interfaces to control inkjet and dye-sub print heads, laser engines, and scanner assemblies
- Copies 8.5" x 11" photos in 40 seconds at 600 dpi
- Complete development tool suite
- · Complete reference design
- · Compatible with code bases developed for other Quatro SOCs
- · Extensive image processing library

Description

Entry-Level Print Appliances

The entry-level segments within the market for print appliances AIOs and direct-connect photo printers are growing dramatically and extending into ever lower price-points. Driving this growth are lower prices, innovative features, and the proliferation of image-rich content from digital cameras, scanned documents, and the Web. The 4050 is designed to address the aggressive cost requirements of these segments. Through its full programmability, the 4050 allows OEMs to rapidly bring products cost-optimized AIOs and photo-printers with PictBridge photo printing to market. The sophisticated image processing functions in the 4050 enable products that feature superb quality, performance and usability within a simple and cost-effective system design.

Programmable Platform

The 4050 is a highly integrated SOC solution for appliance printers that OEMs can program to implement the features and associated image processing required across a range of products. Because it is programmable, the 4050 offers OEMS both significant time-to-market advantages and differentiation over conventional ASIC solutions.

Quatro Architecture

The 4050 is based on a scalable, extensible platform for a series of application-specific SOC solutions.

At the heart of the architecture are four key elements:

- · ARM 32-bit RISC CPU core
- · Quatro 4-datapath SIMD DSP core
- · Industry-standard internal bus
- · Easy-to-use C-based programming environment

Quatro 4050

Programmable SOC Solution for Printers and All-in-Ones

Product Brief

Descriptions (continued)



By pairing the ARM CPU core with the Quatro DSP core, the Quatro solution provides OEMs with a unique combination of high performance processing and easy-to-use programmability. The ARM CPU core, the established leader in embedded CPU cores, delivers high performance system and control processing with dense code size and highly regarded software development tool suite.

The 4050 Quatro DSP core builds on 6 generations and 10 years of Zoran Quatro DSP technology. The 4-datapath parallel processing Single Instruction, Multiple Data (SIMD) architecture is specifically tailored for imaging applications, delivering unmatched performance. The Quatro DSP offers up to 530 million multiply-accumulates (MACs) per second at 133 MHz, allowing new imaging features to be quickly implemented without changing hardware, enabling rapid timeto-market and minimizing development expense.

Programming Environment

The programming environment for the 4050 is based on the ARM RealView Developer Suite, widely recognized as one of the best embedded development tool sets available. To these proven ARM tools Zoran integrates a set of tools for programming the Quatro DSP-C compiler assembler, simulators, debugger, and libraries. Using the ARM CPU and Quatro DSP simulators, an OEM's complete system-both system functions and image processing pipelines-can be fully developed and simulated on a PC. Zoran's extensive library of optimized image processing algorithms makes developing image processing pipelines easy.

Reference Design

To further shorten time-to-market, Zoran provides OEMs with a reference design for an inkjet AIO. The reference design includes both a controller board and firmware. The reference controller board also serves as a development board that OEMs can use to prototype their own system code.

Processing Modules

- · 67 MHz ARM7 32-bit RISC CPU core
- · 133 MHz Quatro 4-datapath SIMD DSP core
- 133 MHz JPEG assist module

Interface Modules

- 133 MHz 16-bit SDRAM interface (w/8-bit mode)
- · USB Full-Speed device interface
- · USB Full-Speed host interface
- · Programmable scanner mechanism control interface with 133 MHz 8-bit flexRISC processor
- Integrated 16-bit scanner AFE supporting CCD and CIS sensors
- Programmable printer mechanism control interface with 133 MHz 8-bit flexRISC processor
- 13-channel 3-MHz 10-bit A/D for printer mechanism control
- · SPI serial flash/EEPROM interface
- · System bus interface
- · General-purpose I/O interface
- · Serial port
- JTAG interface

Key Specifications

- 176-pin LQFP package
- 0.18 micron process
- · On-chip PLL with EMI reduction
- · Full scan design and on-chip memory BIST for high production test coverage
- Core voltage 1.8V
- I/O voltage 3.3V (5V tolerant)
- Power dissipation <2W at maximum clock speed
- · Sleep mode



Quatro 4050 Controller Block Diagram

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