

RD151TS502US

PLL clock generator series

REJ03D0898-0100
Rev.1.00
Apr 25, 2007

Description

RD151TS502US is phase-locked loop clock generator with high-performance. And RD151TS502US is low-jitters and will enable high density mounting by shrink small-size package (SSOP-8).

Features

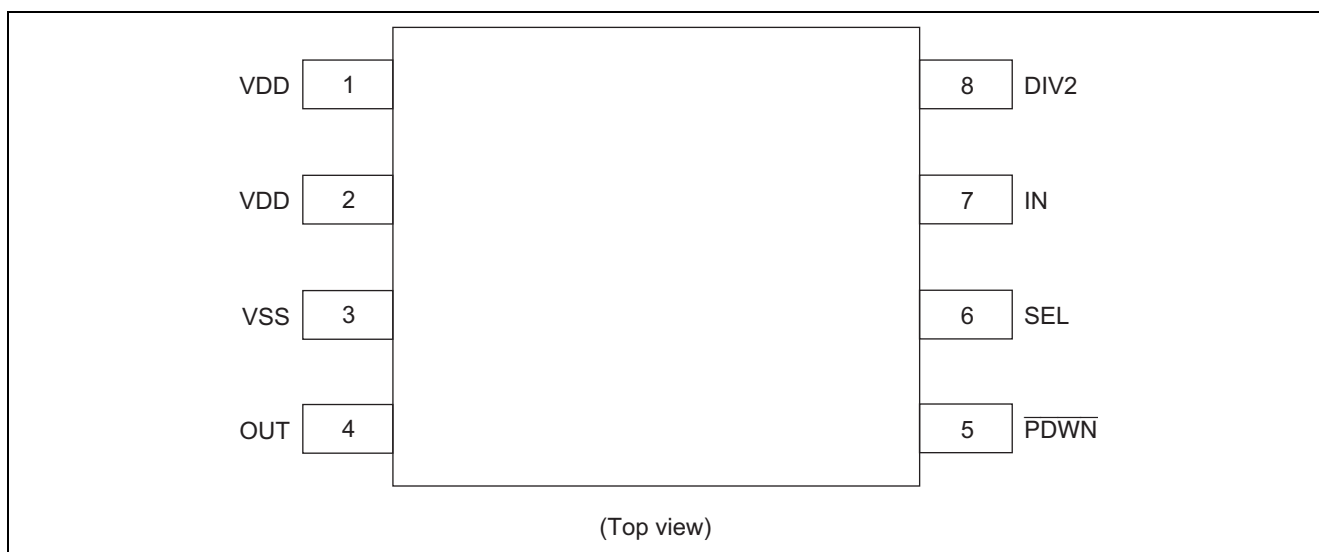
- Input frequency: 27.0 MHz
- Output frequency: 27.0 MHz (1 : 1), 33.75 MHz (1 : 1.25)
13.5 MHz (1 : 0.5), 16.875MHz (1 : 0.625) (Selectable)

Key Specifications

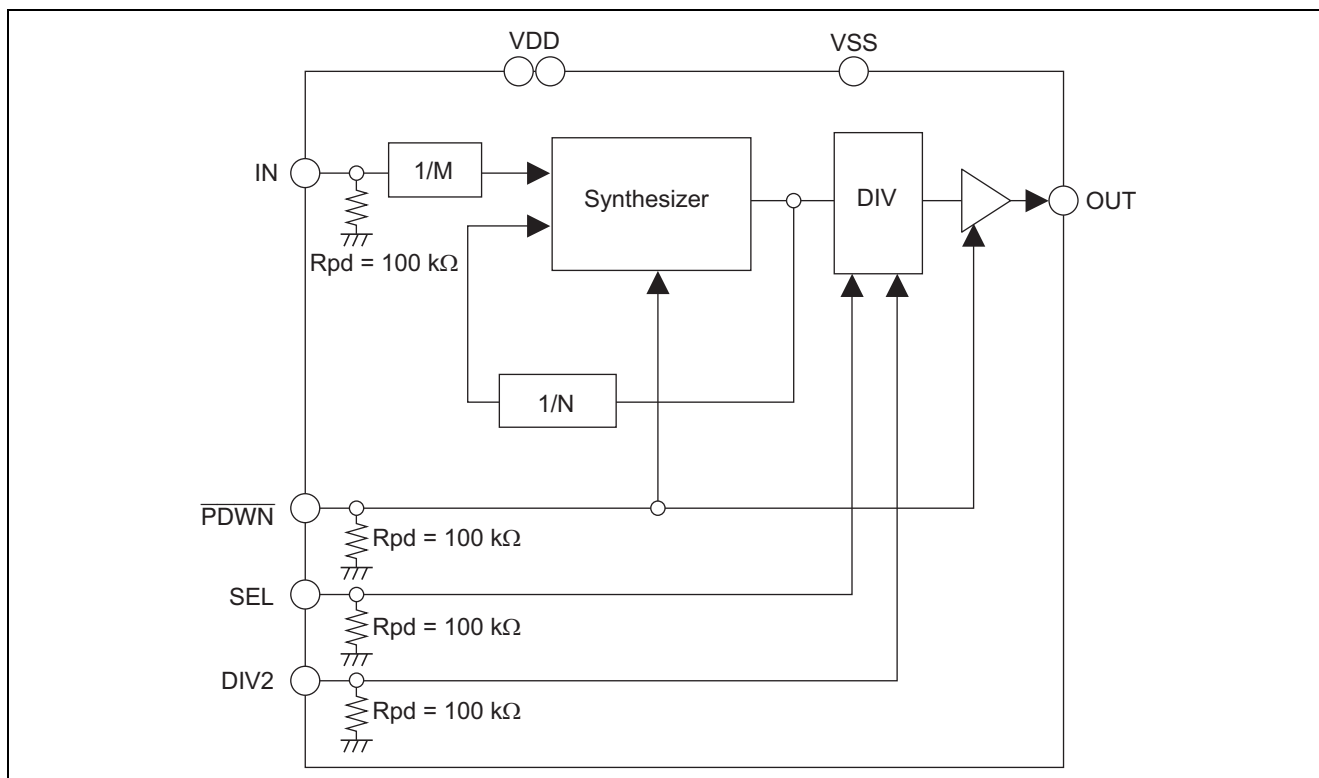
- Supply voltages: $V_{DD} = 2.7$ to 3.6 V
- Operating temperature = -10 to 75 °C
- Cycle to cycle jitter = ± 75 ps typ.
- Clock output duty cycle = $50 \pm 5\%$
- Stabilization time: 2ms max
- Power-down mode is supported
- Ordering Information

| Part Name | Package Type | Package Code (Previous Package Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|---------------|--------------|---|-------------------------|-----------------------------------|
| RD151TS502USE | SSOP-8 pin | PVSP0008KA-A (TTP-8DBV) | US | E (3,000 pcs / Reel) |

Pin Arrangement



Block Diagram



Pin Descriptions

| Pin name | No. | Type | Description |
|--------------------------|-----|--------|----------------------------------|
| VDD | 1,2 | Power | Power supply |
| VSS | 3 | Ground | GND |
| OUT | 4 | Output | Clock signal output |
| $\overline{\text{PDWN}}$ | 5 | Input | Power-down control ^{*1} |
| SEL | 6 | Input | Frequency select ^{*1} |
| IN | 7 | Input | Clock signal input ^{*1} |
| DIV2 | 8 | Input | Frequency select ^{*1} |

Note: 1. LVCMOS level input. Pull-down by internal resistor (100 kΩ).

Power-down Function Table

| $\overline{\text{PDWN}}$ | IC Operating | OUTPUT | Remark |
|--------------------------|--------------|---------------------|-----------------------|
| L | Power-down | Low level | Default ^{*1} |
| H | Active | Clock signal output | |

Note: 1. All Circuits are set stand-by condition.

Clock Frequency Table

| SEL | DIV2 | Output Frequency (IN:OUT Ratio) | Remark |
|-----|------|------------------------------------|---------|
| L | L | 27.0 MHz (1:1) | Default |
| H | L | 33.75 MHz (1:1.25) | |
| L | H | 13.5 MHz (1:0.5) | |
| H | H | 16.875 MHz (1:0.625) | |

Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit | Conditions |
|---------------------------|-----------|----------------------|------------------|---|
| Supply voltage | V_{DD} | -0.5 to 4.6 | V | |
| Input voltage | V_I | -0.5 to 4.6 | V | |
| Output voltage | V_O | -0.5 to $V_{DD}+0.5$ | V | |
| Input clamp current *1 | I_{IK} | -50 | mA | $V_I < 0$ |
| Output clamp current *1 | I_{OK} | -50 | mA | $V_O < 0$ |
| Continuous output current | I_O | ± 50 | mA | $V_O = 0$ to V_{DD} |
| Maximum power dissipation | P_W | 0.2 | W | $T_a = 25^\circ\text{C}$ (in still air) |
| Storage temperature | T_{stg} | -65 to +150 | $^\circ\text{C}$ | |

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Recommended Operating Conditions

| Item | Symbol | Min | Typ | Max | Unit | Conditions |
|-------------------------|----------|------|-----|--------------|------------------|------------|
| Supply voltage | V_{DD} | 2.7 | 3.3 | 3.6 | V | |
| DC input signal voltage | | -0.3 | — | $V_{DD}+0.3$ | V | |
| Operating temperature | T_a | -10 | — | 75 | $^\circ\text{C}$ | |

DC Electrical Characteristics

$T_a = -10$ to 75°C , $V_{DD} = 2.7$ to 3.6 V

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--------------------|----------|--------------|-------|-----------|---------------|---|
| Input voltage | V_{IL} | — | — | 0.8 | V | IN, PDWN, SEL, DIV2 pins |
| | V_{IH} | 2.0 | — | — | V | IN, $\overline{\text{PDWN}}$, SEL, DIV2 pins |
| Input current | I_I | — | — | ± 100 | μA | $V_I = 0\text{V}$ or 3.6V , IN, $\overline{\text{PDWN}}$, SEL, DIV2 pins |
| Input capacitance | C_I | — | 3 | — | pF | IN, PDWN, SEL, DIV2 pins |
| Output voltage | V_{OL} | — | — | 0.5 | V | $V_{OL} = 1$ mA, $V_{DD} = 3.3$ V, OUT pin |
| | V_{OH} | $V_{DD}-0.2$ | — | V_{DD} | | $V_{OH} = -1$ mA, $V_{DD} = 3.3$ V, OUT pin |
| Output current | I_{OL} | — | 15 | — | mA | $V_{OL} = 1.65$ V, $V_{DD} = 3.3$ V, OUT pin |
| | I_{OH} | — | -15 | — | mA | $V_{OH} = 1.65$ V, $V_{DD} = 3.3$ V, OUT pin |
| Output impedance | | — | 30 | — | Ω | OUT pin |
| Pull-down resistor | R_{pd} | 80 k | 100 k | 120 k | Ω | |

Note: The condition of the minimum and maximum value must use the value specified under "Recommended Operating Conditions".

Parameters are target of design. Not 100% tested in production.

AC Electrical Characteristics

$T_a = -10$ to 75 °C, $V_{DD} = 2.7$ to 3.3 V, $C_L = 15$ pF

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Notes |
|-----------------------|------------|-----|--------|-----|------|--|----------------|
| Operating current | I_{DD} | — | 6 | — | mA | $V_{DD} = 3.3$ V, $\overline{PDWN} = 1$, $C_L = 0$ pF | |
| Stand-by current | I_{DDPD} | — | 10 | — | μA | $V_{DD} = 3.3$ V, $\overline{PDWN} = 0$, $I_N = 0$ V | |
| Cycle to cycle jitter | t_{CCJ} | — | 75 | — | ps | $C_L = 0$ pF | Figure 1 |
| Output Frequency | | — | 13.5 | — | MHz | SEL = 0, DIV2 = 1 | *1 Figure 2 |
| | | — | 16.875 | — | | SEL = 1, DIV2 = 1 | |
| | | — | 27.0 | — | | SEL = 0, DIV2 = 0 | |
| | | — | 33.75 | — | | SEL = 1, DIV2 = 0 | |
| Frequency accuracy | | -50 | — | 50 | ppm | | *2 |
| Slew Rate | t_{SR} | — | 1.5 | — | ns | $V_{DD} = 3.3$ V, $0.2V_{DD}$ to $0.8V_{DD}$ | |
| Clock duty cycle | t_{DT} | 45 | 50 | 55 | % | | |
| Stabilization time | t_{SB} | — | — | 2 | ms | | *3 |

Notes: Parameters are target of design. Not 100% tested in production.

1. Output Frequency means average value.
2. The accuracy of the output frequency to a set value.
3. Stabilization time is the time required for the integrated circuit to obtain phase lock of its input signal after power up.

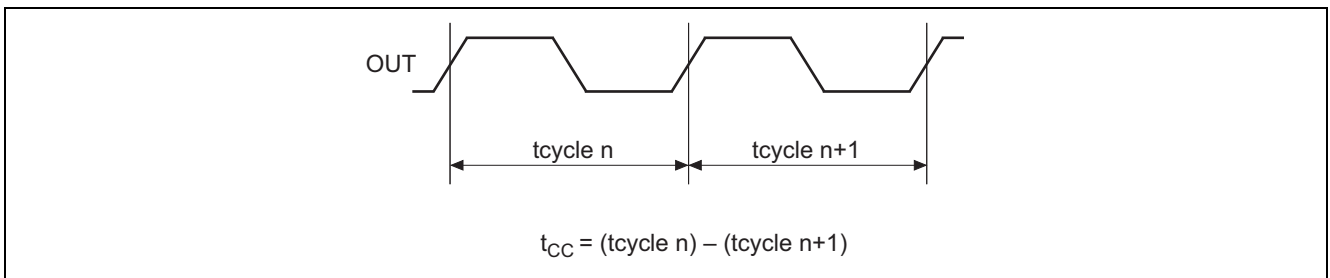


Figure 1 Cycle to cycle jitter

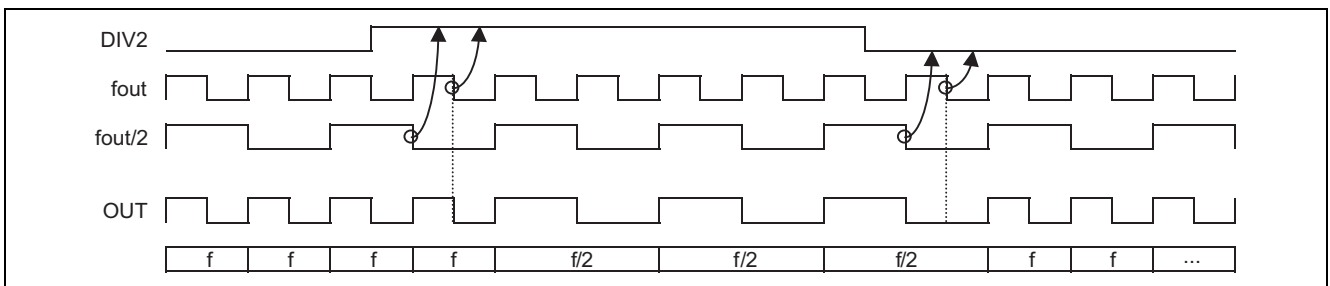


Figure 2 Timing chart

Recommended Circuit Configuration

The power supply circuit of the optimal performance on the application of a system should refer to Figure 3.

V_{DD} decoupling is important to reduce Jitter performance.

The C1 decoupling capacitor should be placed as close to the VDD pin as possible, otherwise the increased trace inductance will negate its decoupling capability.

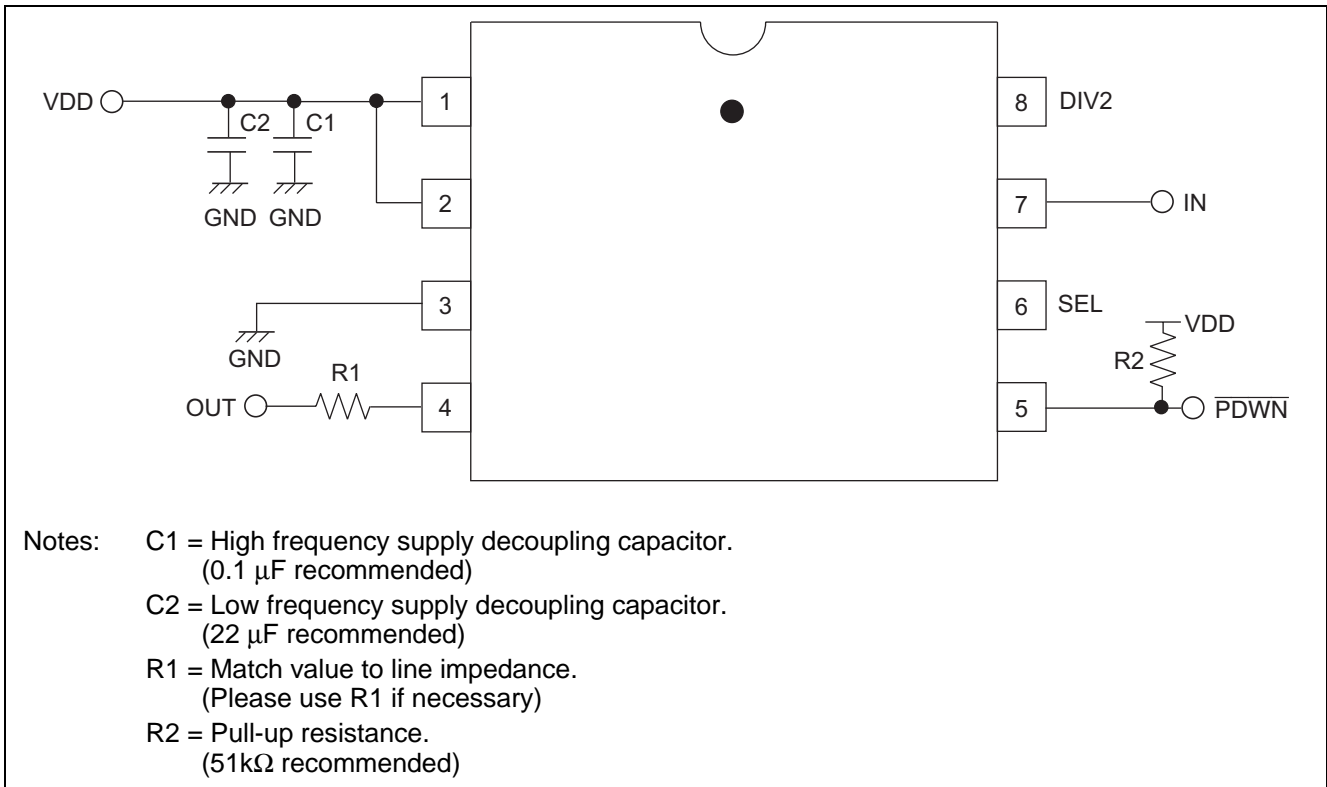


Figure 3 Recommended circuit configuration

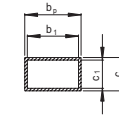
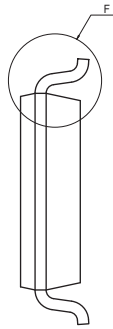
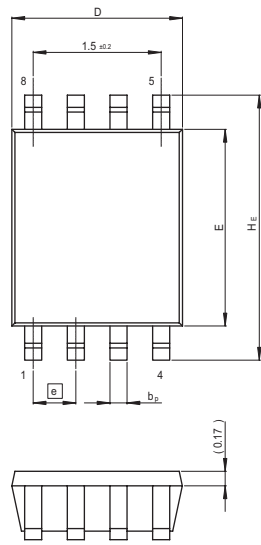
Remark for use

- Please do not use the pull-up resistance for the OUT terminal to prevent wrong operation of IC.
- Please set the voltage of the PDWN terminal according to the following procedures when it is necessary to set IC to power-down (standby) operation immediately after the start-up this IC.
 1. Set the Hi level voltage when IC starts.
 2. Set the Low level voltage after IC starts.

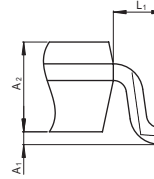
As this counter measures, we recommend the pull-up register that has been described to the above recommended circuit to be added beforehand.

Package Dimensions

| | | | |
|---------------------|--------------|------------------|------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
| P-VSSOP8-2.3x2-0.50 | PVSP0008KA-A | TTP-8DB/TTP-8DBV | 0.010g |



Terminal cross section



Detail F

| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|-------|------|
| | Min | Nom | Max |
| D | 1.8 | 2.0 | 2.2 |
| E | 2.2 | 2.3 | 2.4 |
| A ₂ | 0.6 | 0.7 | 0.8 |
| A ₁ | 0 | — | 0.1 |
| A | — | — | — |
| b _p | 0.15 | 0.22 | 0.3 |
| b ₁ | — | 0.20 | — |
| c | 0.08 | 0.13 | 0.23 |
| c ₁ | — | 0.11 | — |
| θ | — | — | — |
| H _E | 2.8 | 3.1 | 3.4 |
| ⓐ | — | (0.5) | — |
| x | — | — | — |
| y | — | — | — |
| Z | — | — | — |
| L | — | — | — |
| L ₁ | — | (0.4) | — |

Notes:

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