RF6100-4

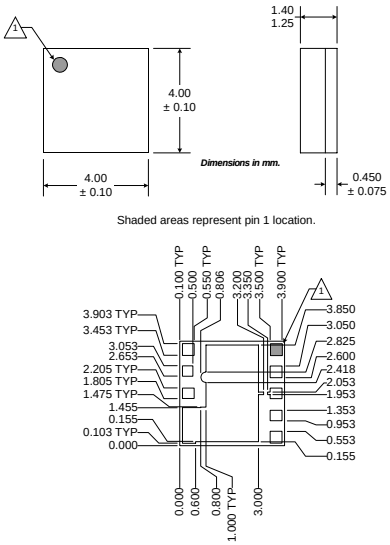
3V 1900MHZ LINEAR POWER AMPLIFIER MODULE

Typical Applications

- 3V CDMA US-PCS Handset
- 3V CDMA2000/1XRTT US-PCS Handset
- 3V CDMA2000/1X-EV-DO US-PCS Handset
- Spread-Spectrum System

Product Description

The RF6100-4 is a high-power, high-efficiency linear amplifier module specifically designed for 3V handheld systems. The device is manufactured on an advanced third generation GaAs HBT process, and was designed for use as the final RF amplifier in 3V IS-95/CDMA 2000 1X handheld digital cellular equipment, spread-spectrum systems, and other applications in the 1850MHz to 1910MHz band. The RF6100-4 has a digital control line for low power applications to lower quiescent current. The device is self-contained with 50Ω input and output that is matched to obtain optimum power, efficiency and linearity. The module is a 4mmx4mm land grid array with backside ground. The RF6100-4 is footprint compatible with industry standard 4mmx4mm CDMA modules, and requires only one decoupling capacitor.



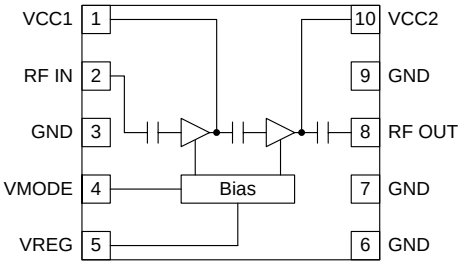
Package Style: Module (4mmx4mm)

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS
- ☐ InGaP/HBT
- ☐ GaN HEMT
- ☐ SiGe Bi-CMOS

Features

- Input/Output Internally Matched@50Ω
- 28.5dBm Linear Output Power
- 39% Peak Linear Efficiency
- 28dB Linear Gain
- -48dBc ACPR @ 1.25MHz



Functional Block Diagram

Ordering Information

RF6100-4	3V 1900MHz Linear Power Amplifier Module
RF6100-4 PCBA	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V
Supply Voltage ($P_{OUT} \leq 31$dBm)	+5.2	V
Control Voltage (V_{REG})	+3.9	V
Input RF Power	+10	dBm
Mode Voltage (V_{MODE})	+3.5	V
Operating Temperature	-30 to +110	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

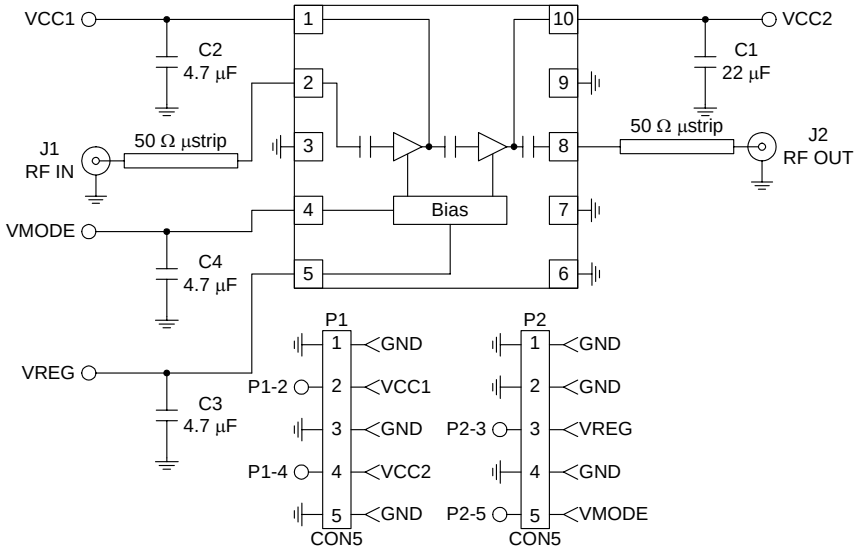
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Gain Mode (V_{MODE} Low)					T=25°C Ambient, V_{CC}=3.4V, V_{REG}=2.8V, V_{MODE}=0V, and P_{OUT}=28.5dBm for all parameters (unless otherwise specified).
Operating Frequency Range	1850		1910	MHz	
Linear Gain	26	28	31	dB	
Second Harmonics		-35	-30	dBc	
Third Harmonics		-40		dBc	
Maximum Linear Output	28.5			dBm	
Linear Efficiency	35	39		%	
Maximum I_{CC}		535	600	mA	
ACPR @ 1.25MHz		-48	-46	dBc	
ACPR @ 2.25MHz		-62	-56	dBc	
Input VSWR		2:1			
Output VSWR Stability			6:1		No oscillation>-70dBc
			10:1		No damage
Noise Power		-139		dBm/Hz	At 80MHz offset.
Low Gain Mode (V_{MODE} High)					T=25°C Ambient, V_{CC}=3.4V, V_{REG}=2.8V, V_{MODE}=2.8V, and P_{OUT}=28.5dBm for all parameters (unless otherwise specified).
Operating Frequency Range	1850		1910	MHz	
Linear Gain	25	27	31	dB	
Second Harmonics		-35	-30	dBc	
Third Harmonics		-40		dBc	
Maximum Linear Output	28.5			dBm	
Linear Efficiency	35	39		%	
ACPR @1.25MHz		-48	-46	dBc	
ACPR @2.25MHz		-60	-56	dBc	
Maximum I_{CC}		140	165	mA	P_{OUT}=16dBm
Linear Gain		26		dB	P_{OUT}=16dBm
Input VSWR		2:1			
Output VSWR Stability			6:1		No oscillation>-70dBc
			10:1		No damage

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Supply					T=25°C Ambient
Supply Voltage	3.2	3.4	4.2	V	
High Gain Idle Current	60	75	90	mA	V_{MODE}=low and V_{REG}=2.8V
Low Gain Idle Current	50	65	80	mA	V_{MODE}=high and V_{REG}=2.8V
V_{REG} Current		1.1	2	mA	V_{CC}=3.4V, V_{REG}=2.8V
V_{MODE} Current		250	500	uA	
RF Turn On/Off Time		1.2	6	uS	
DC Turn On/Off Time		2	40	uS	
Total Current (Power Down)		0.2	5	uA	
V_{REG} Low Voltage (Power Down)	0		0.5	V	
V_{REG} High Voltage (Recommended)	2.75	2.8	2.95	V	
V_{REG} High Voltage (Operational)	2.7		3.0	V	
V_{MODE} Voltage	0		0.5	V	High Gain Mode
V_{MODE} Voltage	2.0		3.0	V	Low Gain Mode

Pin	Function	Description	Interface Schematic
1	VCC1	First stage collector supply. A low frequency decoupling capacitor (e.g., 4.7μF) may be required.	
2	RF IN	RF input internally matched to 50Ω. This input is internally AC-coupled.	
3	GND	Ground connection. Connect to package base ground. For best performance, keep traces physically short and connect immediately to ground plane.	
4	VMODE	For nominal operation (High Power Mode), V_{MODE} is set LOW. When set HIGH, devices are biased lower to improve efficiency.	
5	VREG	Regulated voltage supply for amplifier bias. In Power Down mode, both V_{REG} and V_{MODE} need to be LOW (<0.5V).	
6	GND	Ground connection. Connect to package base ground. For best performance, keep traces physically short and connect immediately to ground plane.	
7	GND	Ground connection. Connect to package base ground. For best performance, keep traces physically short and connect immediately to ground plane.	
8	RF OUT	RF Output internally matched to 50Ω. This output is internally AC-coupled.	
9	GND	Ground connection. Connect to package base ground. For best performance, keep traces physically short and connect immediately to ground plane.	
10	VCC2	Output stage collector supply. A low frequency decoupling capacitor (e.g., 4.7μF) is required.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land and Solder Mask Pattern

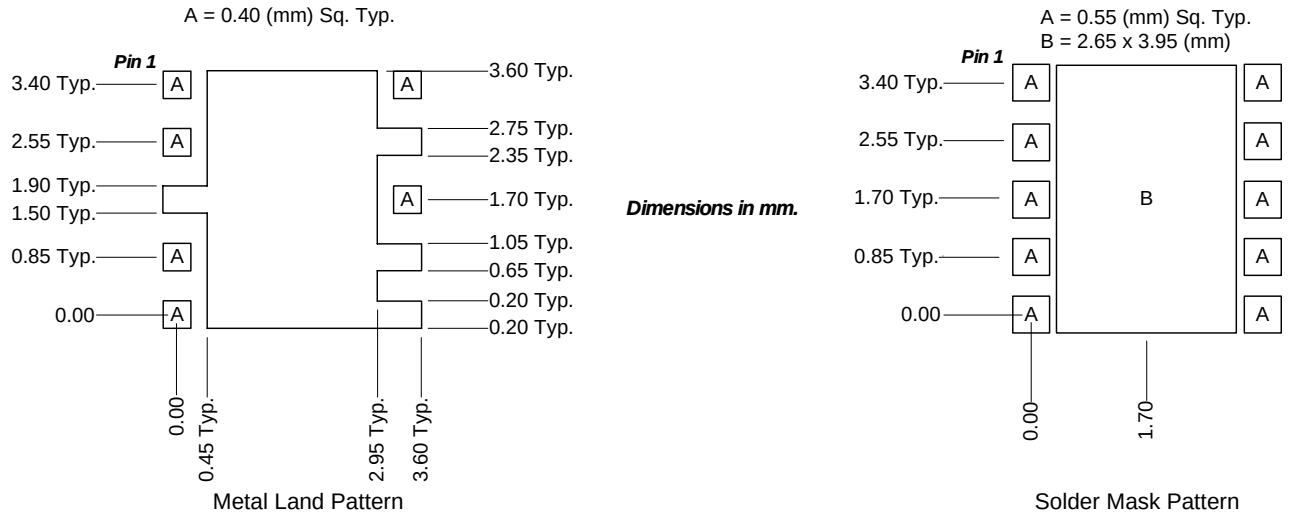


Figure 1. PCB Metal Land Pattern and Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.