

4A, 60V, 0.600 Ohm, Logic Level, N-Channel Power MOSFETs

The RFD4N06L, RFD4N06LSM are N-Channel enhancement mode silicon gate power field effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control from logic circuit supply voltages.

Formerly developmental type TA09520.

Ordering Information

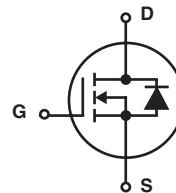
PART NUMBER	PACKAGE	BRAND
RFD4N06L	TO-251AA	RFD4N06L
RFD4N06LSM	TO-252AA	RFD4N06LSM

NOTE: When ordering, use the entire part number.

Features

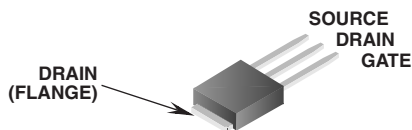
- 4A, 60V
- $r_{DS(ON)} = 0.600\Omega$
- Design Optimized for 5 Volt Gate Drive
- Can be Driven Directly From Q-MOS, N-MOS, or TTL Circuits
- SOA is Power Dissipation Limited
- 175°C Rated Junction Temperature
- Logic Level Gate
- High Input Impedance
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

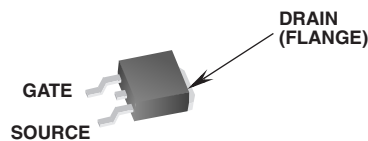


Packaging

JEDEC TO-251AA



JEDEC TO-252AA



RFD4N06L, RFD4N06LSM

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	RFD4N06L	RFD4N06LSM	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS}	60	V
Drain to Gate Voltage (Note 1)	V_{DGR}	60	V
Gate to Source Voltage	V_{GS}	± 10	V
Continuous Drain Current	I_D	4	A
Pulsed Drain Current (Note 3)	I_{DM}	10	A
Maximum Power Dissipation	P_D	30	W
Derated above 25°C		0.20	$W/^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 1mA, V _{GS} = 0V		60	-	-	V
Gate to Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA		1	-	2.5	V
Zero Gate Voltage Drain Current	I _{DSS}	T _C = 25°C, V _{DS} = 50V, V _{GS} = 0V		-	-	1	μA
		T _C = 125°C, V _{DS} = 50V, V _{GS} = 0V		-	-	50	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±10V, V _{DS} = 0V		-	-	±100	nA
Drain to Source On Voltage (Note 2)	V _{DS(ON)}	I _D = 1A, V _{GS} = 5V		-	-	0.8	V
		I _D = 2A, V _{GS} = 5V		-	-	2.0	V
		I _D = 4A, V _{GS} = 7.5V		-	-	4.0	V
Drain to Source On Resistance (Note 2)	r _{DS(ON)}	I _D = 1A, V _{GS} = 5V		-	-	0.600	Ω
Forward Transconductance (Note 2)	V _(plateau)	V _{DS} = 15V, I _D = 4A		-	-	4.5	V
Turn-On Delay Time	t _{d(ON)}	V _{DD} = 30V, I _D = 1A, R _{GS} = 6.25Ω, V _{GS} = 5V		-	-	20	ns
Rise Time	t _r			-	-	130	ns
Turn-Off Delay Time	t _{d(OFF)}			-	-	40	ns
Fall Time	t _f			-	-	160	ns
Total Gate Charge (Gate to Source + Gate to Drain)	Q _{g(TOT)}	V _{GS} = 0-10V	V _{DD} = 48V, I _D = 2A, R _L = 24Ω	-	-	8	nC
Gate Charge at 5V	Q _{g(5)}	V _{GS} = 0-5V		-	-	5	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0-1V		-	-	1	nC
Thermal Resistance Junction to Case	R _{θJC}			-	-	5	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = 1\text{A}$	-	-	1.4	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 2\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	150	-	ns

NOTES:

2. Pulsed: pulse duration = 300 μs max, duty cycle = 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

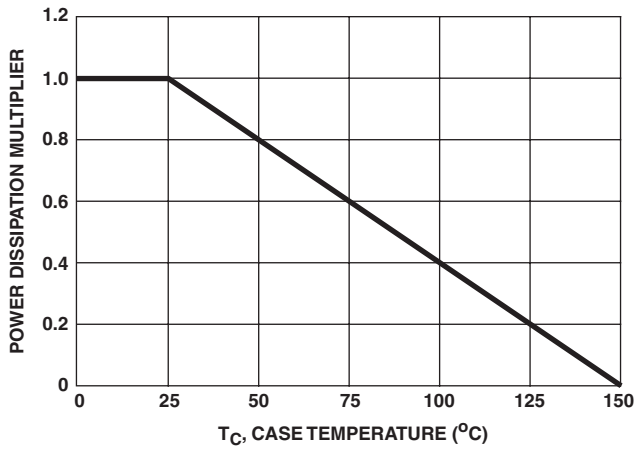


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

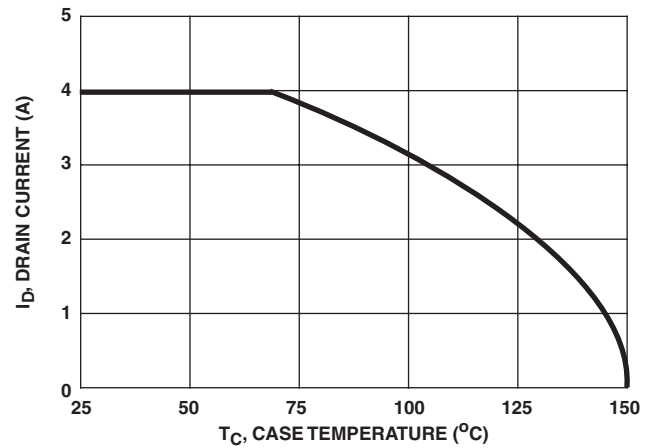


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

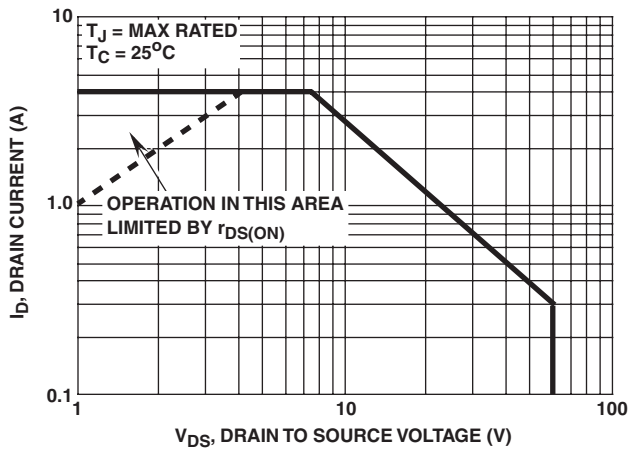


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

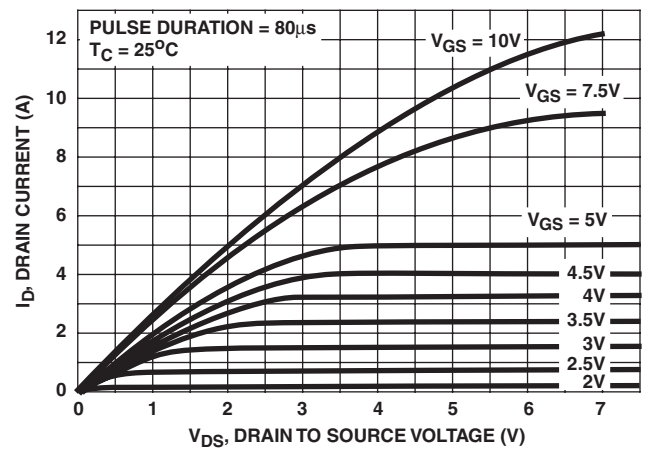


FIGURE 4. SATURATION CHARACTERISTICS

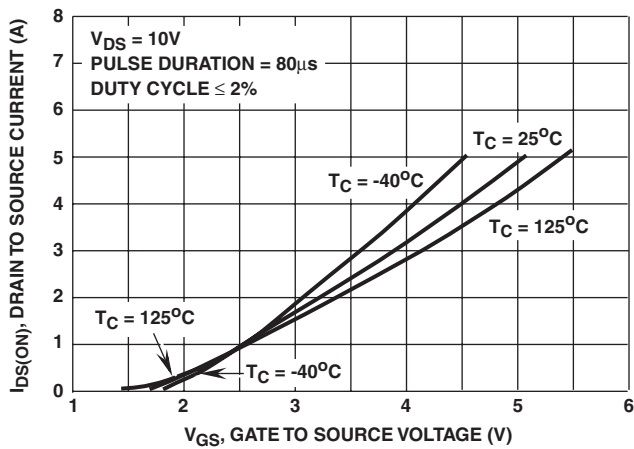


FIGURE 5. TRANSFER CHARACTERISTICS

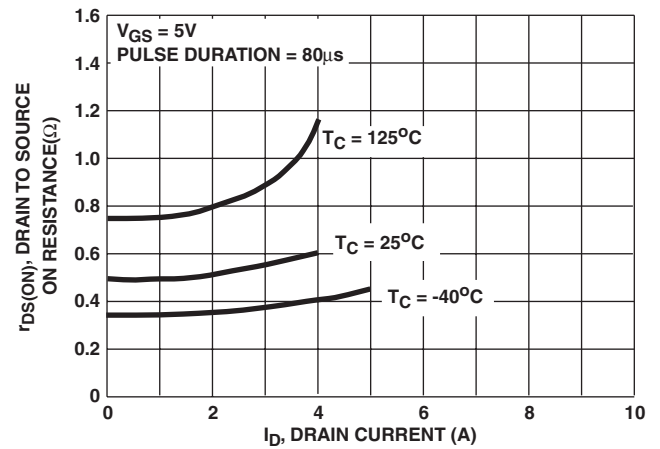


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified (Continued)

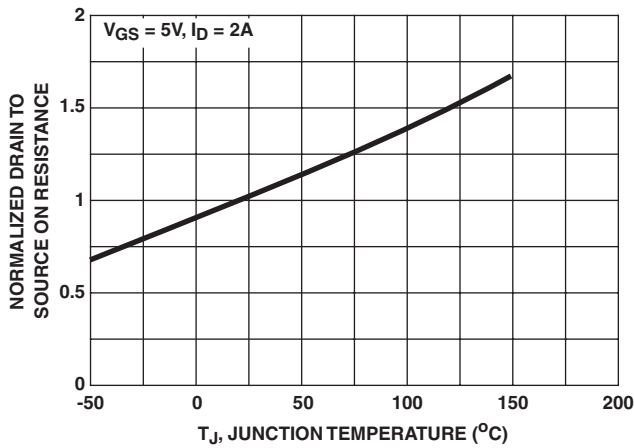


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

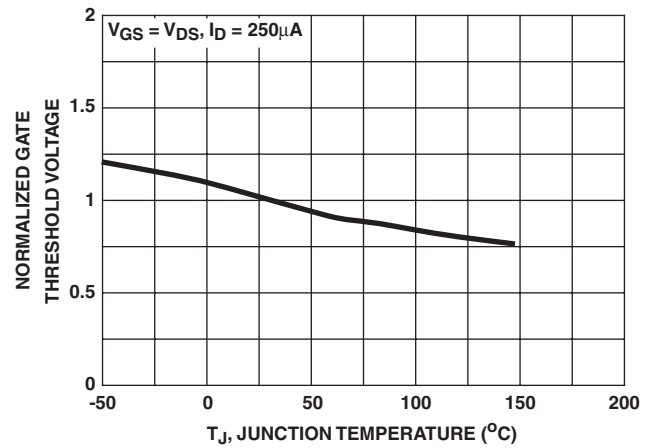


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

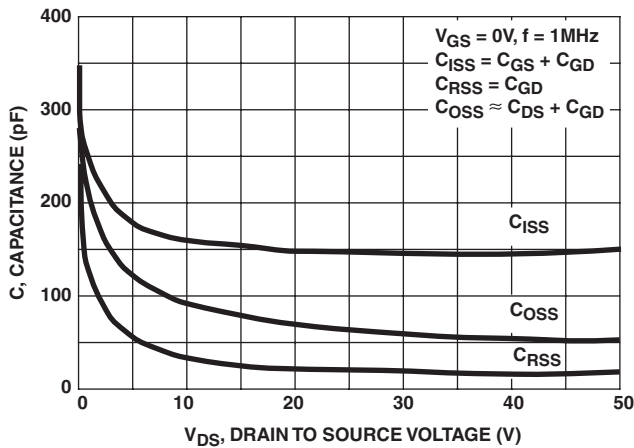
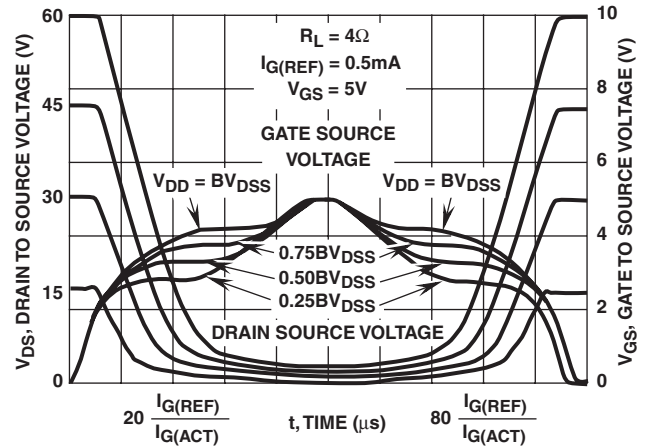


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

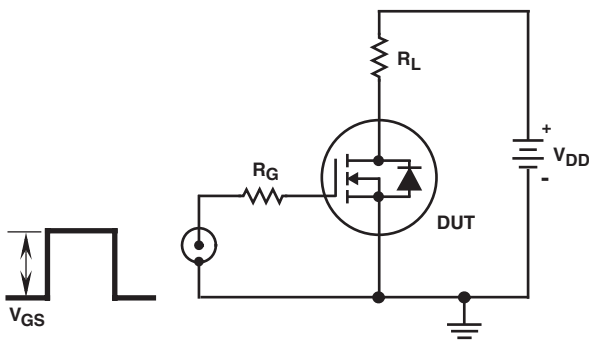


FIGURE 11. SWITCHING TIME TEST CIRCUIT

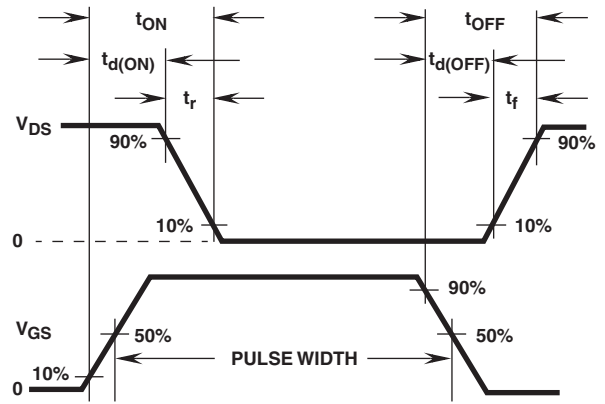


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

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CROSSVOLT TM	GlobalOptoisolator TM	POP TM	SuperSOT TM -3	
DenseTrench TM	GTO TM	Power247 TM	SuperSOT TM -6	
DOME TM	HiSeC TM	PowerTrench [®]	SuperSOT TM -8	
EcoSPARK TM	ISOPLANAR TM	QFET TM	SyncFET TM	
E ² CMOS TM	LittleFET TM	QS TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
FACT TM	MicroPak TM	Quiet Series TM	UHC TM	
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