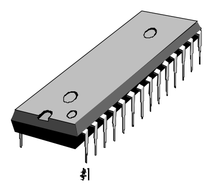
VIDEO AMP MERGED OSD PROCESSOR

32-DIP-600A



The S1D2502B01 is a very high frequency video amplifier & wide range OSD processor 1 chip system with I^2C Bus control used in monitors. It contains 3 matched R/G/B video amplifiers with OSD processor and provides flexible interfacing to I^2C Bus controlled adjustment systems.

FUNCTIONS

- R/G/B video amplifier
- OSD processor
- I^2C bus control
- Cut-off brightness control
- R/G/B sub contrast/cut-off control
- Half tone

ORDERING INFORMATION

Device	Package	Operating Temperature
S1D2502B01-D0B0	32-DIP-600A	-20 °C — +75°C

FEATURES

VIDEO AMP PART

- 3-channel R/G/B video amplifier, 175MHz @f-3dB
- I^2C bus control items
  — Contrast control: -38dB
  — Sub contrast control for each channel: -12dB
  — Brightness control
  — OSD contrast control: -38dB
  — Cut-off brightness control (AC coupling)
  — Cut-off control for each channel (AC coupling)
  — Switch registers for SBLK and video half tone and CLP/BLK polarity selection and INT/EXT CLP selection and generated CLP width control
- Built in ABL (automatic beam limitation)
- Built in video input clamp, BRT clamp
- Built in video half tone (3mode) function on OSD pictures
- Capable of 8.0Vp-p output swing
- Improvement of rise & fall time (2.2ns)
- Cut-off brightness control
- Built in blank gate with spot killer
- Clamp pulse generator
- OSD intensity
- BLK, CLP polarity selection
- Clamp gate with anti OSD sagging

OSD PART

- Built in 1K-byte SRAM
- 448 ROM fonts (each font consists of 12×18 dots.)
- Full screen memory architecture
- Wide range PLL available (15kHz — 90kHz, Reference 800 X 600)
- Programmable vertical height of character
- Programmable vertical and horizontal positioning
- Character color selection up to 16 different colors
- Programmable background color (up to 16 colors)
- Character blinking, bordering and shadowing
- Color blinking
- Character scrolling
- Fade-in and fade-out
- Box drawing
- Character sizing up to four times
- 72MHz pixel frequency from on-chip PLL (Reference 800 X 600)

BLOCK DIAGRAM

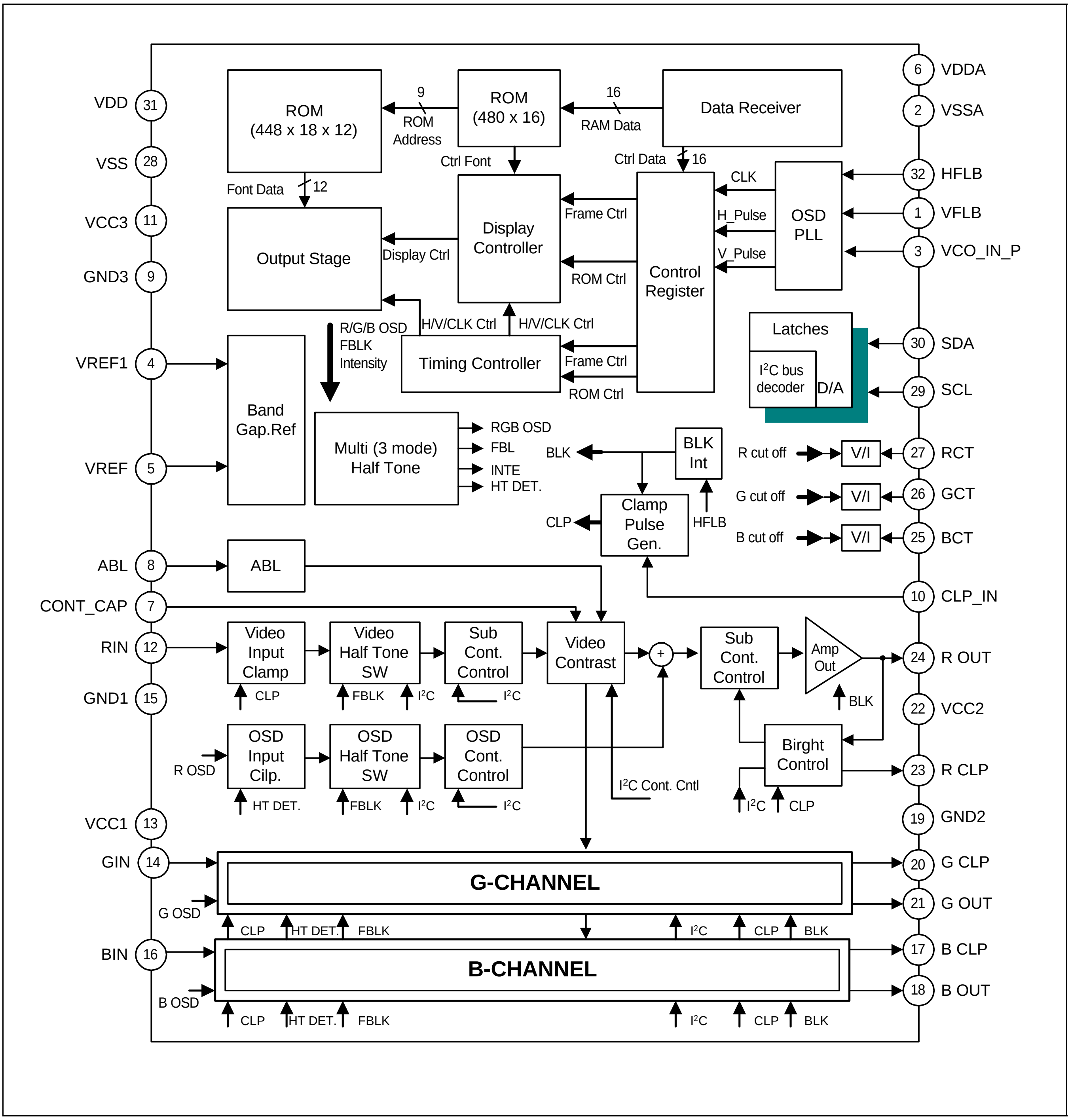


Figure 1. Functional Block Diagram

PIN CONFIGURATION

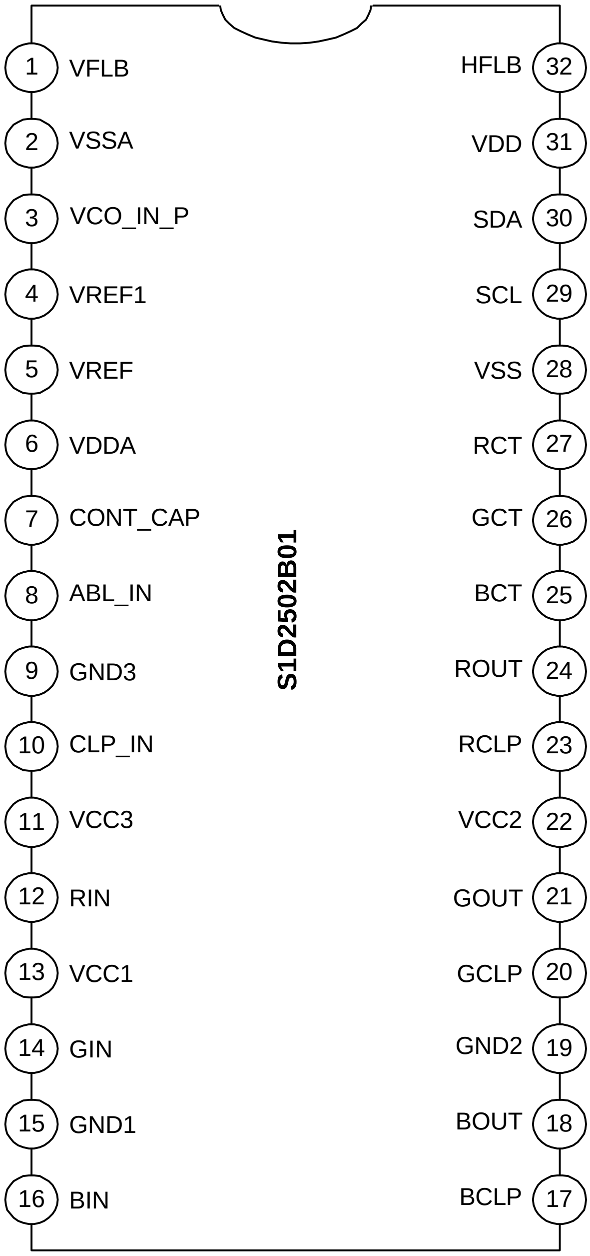


Figure 2. Pin Configuration

Table 1. Pin Configuration

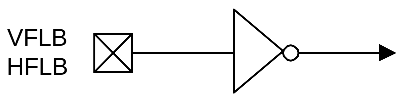
Pin No.	Symbol	I/O	Configuration
1	VFLB	I	Vertical flyback signal
2	VSSA	-	Ground (PLL part)
3	VCO_IN_P	I	This voltage is generated at the external loop filter and goes into the input stage of the VCO.
4	VREF1	O	Charge pump output
5	VREF	O	PLL regulator filter
6	VDDA	-	+5V supply voltage for PLL part
7	CONT_CAP	-	Contrast control for AMP part
8	ABL	-	Auto beam limit.
9	GND3	-	Ground for video AMP part(for AMP control)
10	CLP_IN	-	Video clamp pulse input
11	VCC3	-	+12V supply voltage for video AMP part(for AMP control)
12	RIN	I	Video signal input (red)
13	VCC1	-	+12V supply voltage for video AMP(for main video signal process)
14	GIN	I	Video signal input (green)
15	GND1	-	Ground for video AMP part(for main video signal process)
16	BIN	I	Video signal input (blue)
17	BCLP	-	B output clamp cap
18	BOUT	O	Video signal output (blue)
19	GND2	-	Ground for video AMP part(for video output drive)
20	GCLP	-	G output clamp cap
21	GOUT	O	Video signal output (green)
22	VCC2	-	+12V supply voltage for video AMP part(for video output drive)
23	RCLP	-	R output clamp cap
24	ROUT	O	Video signal output (red)
25	BCT	-	B cut-off output
26	GCT	-	G cut-off output
27	RCT	-	R cut-off output
28	VSS	-	Ground for digital part
29	SCL	I	Serial clock (I^2C)
30	SDA	I/O	Serial data (I^2C)
31	VDD	-	+5V supply voltage for digital part
32	HFLB	I	Horizontal flyback signal

PIN DESCRIPTION

Table 2. Pin Description

<table>
<tr><th>Pin No</th><th>Pin Name</th><th>Schematic</th><th>Description</th></tr>
<tr><td>1

32</td><td>VFLB

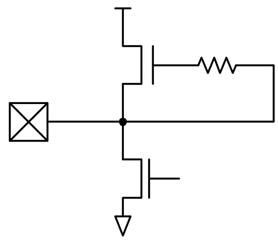
HFLB</td><td>
</td><td>FLB signal is in TTL level

Multi polarity input</td></tr>
<tr><td>3

4

5</td><td>VCO_IN_P

VPEF/

VREF</td><td></td><td>PLL loop filter output

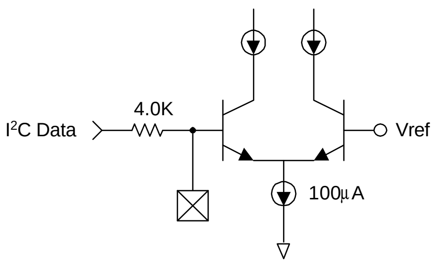
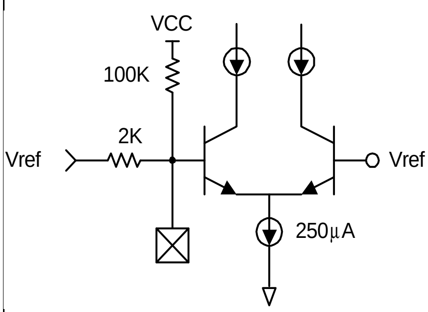
BandGap ref. output</td></tr>
<tr><td>7</td><td>Contrast cap
(CONT_CAP)</td><td>
</td><td>Contrast cap range
(0.1uF — 5uF)</td></tr>
<tr><td>8</td><td>ABL_IN</td><td>
</td><td>ABL input DC range
(1 — 4.5V)</td></tr>
</table>

Table 2. Pin Description (Continued)

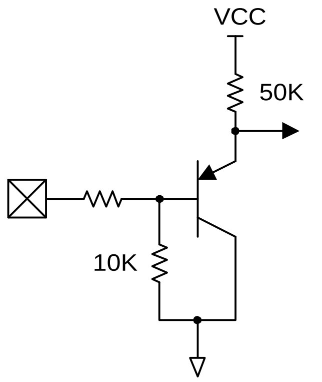
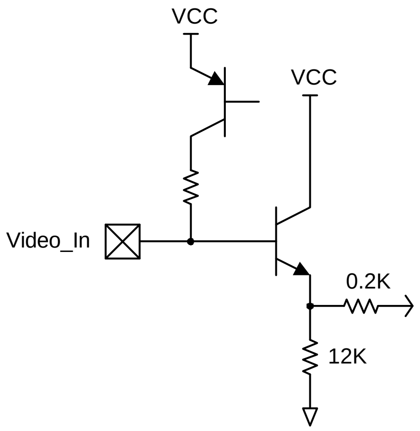
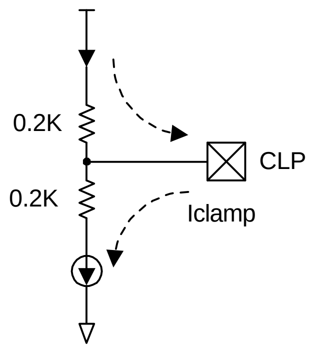
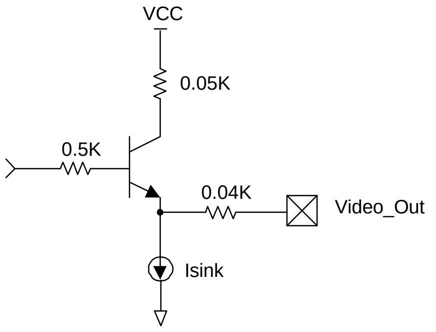
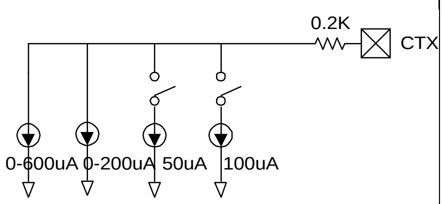
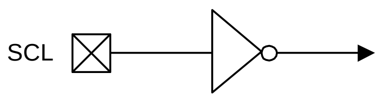
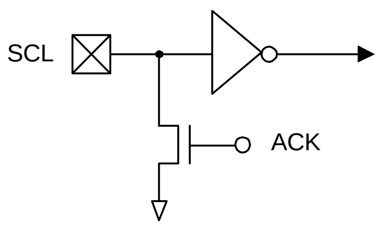
Pin No	Pin Name	Schematic	Description
10	CLP_IN		Multi polarity input Clamp gate pulse TTL level input
12 14 16	Red video input (RIN) Green video input (GIN) Blue video input (BIN)		Max input video signal is 0.7 Vpp
17 20 23	Blue (B clamp cap) Green (G clamp cap) Red (R clamp)		Brightness controlling actives by charging and discharging of the external cap. (0.1µF) (During clamp gate)

Table 2. Pin Description (Continued)

Pin No	Pin Name	Schematic	Description
18 21 24	Blue video output (BOUT) Green video output (GOUT) Red video output (ROUT)		Video signal output
27 26 25	Red cut-off control (RCT) Green cut-off control (GCT) Blue cut-off control (BCT)		Cut-off control output
29	SCL		Serial clock input port of I^2C bus
30	SDA		Serial data input port of I^2C bus

ABSOLUTE MAXIMUM RATINGS (see 1)

(Ta = 25 °C)

Table 3. Absolute Maximum Ratings

No	Item	Symbol	Value			Unit
			Min	Typ	Max	
1	Maximum supply voltage	V_{CC}	-	-	13.2	V
		V_{DD}	-	-	6.5	
2	Operating temperature (see 2)	Topr	-20	-	75	°C
3	Storage temperature	Tstg	-65		150	°C
4	Operating supply voltage	V_{CCop}	11.4	12.0	12.6	V (see 3)
		V_{DDop}	4.75	5.00	5.25	
5	Power dissipation	P_D	-	-		W

THERMAL & ESD PARAMETER

Table 4. Thermal & ESD Parameter

No	Item	Symbol	Value			Unit
			Min	Typ	Max	
1	Thermal resistance (junction-ambient)	θja	-	48	-	°C/W
2	Junction temperature	Tj	-	150	-	°C
3	Human body model (C = 100p, R = 1.5k)	HBM	2	-	-	KV
4	Machine model (C = 200p, R = 0)	MM	300	-	-	V
5	Charge device model	CDM	800	-	-	V

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

(Tamb = 25 °C, V_{CC} = 12V, V_{DD} = V_{DDA} = 5V, ABL input voltage = 5V, HFLB input signal = S3, load resistors = 470Ω, except OSD part current 35mA, unless otherwise stated)

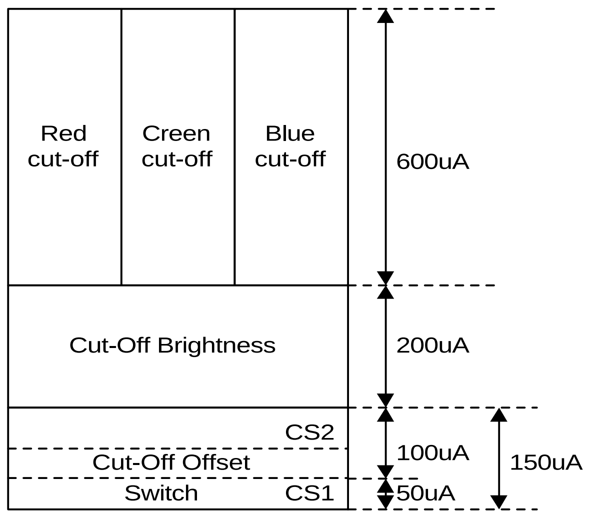
Table 5. DC Electrical Characteristics

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Supply current	I_{CC} (see 4)		100	125	130	mA
Minimum supply current	I_{CC} min	V_{CC} = 11.4V	95	110	120	mA
Maximum supply current	I_{CC} max	V_{CC} = 12.6V	105	130	140	mA
ABS supply current	I_{CC} abs	V_{CC} = 13.2V	-	-	175	mA
Video input bias voltage	V bias		1.8	2.1	2.4	V
Video black level voltage (POR)	V blackpor		1.20	1.50	1.80	V
Black level voltage channel difference (POR)	Δ V blackpor (see 5)		Δ 10	-	-	%
Video black level voltage (FFH)	V blackff	04 = FFH (see 13)	2.2	2.7	3.2	V
Black level voltage channel difference (FFH)	Δ V blackff		Δ 10	-	-	%
Video black level voltage (00H)	V black00	04 = 00H	-	0.2	0.5	V
Black level voltage channel difference (00H)	Δ V black00		Δ 10	-	-	%
Spot killer voltage	Vspot	V_{CC} = Var.	9.20	10.4	11.2	V
Cut-off current (FFH)	ICTff	Pin25, 26, 27 = 12V 09 — 0B: FFH 0C: 00H	500	625	750	µA
Cut-off current (00H)	ICT00	Pin25, 26, 27 = 12V 09 — 0C: 00H	-	2.0	5.0	µA
Cut-off brightness current (FFH)	ICTBRTff	Pin25, 26, 27 = 12V 09 — 0B: 00H 0C: FFH	100	180	260	µA
Cut-off brightness current (80H)	ICTBRT80	Pin25, 26, 27 = 12V 09 — 0B: 00H 0C: 80H	50	90	130	µA
Cut-off offset current 1	ICS1	Pin25, 26, 27 = 12V 09 — 0C: 00H 0E: 11H	25	50	75	µA

Table 5. DC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Cut-off offset current 2	ICS2	Pin25, 26, 27 = 12V 09 — 0C: 00H 0E: 12H	50	100	130	µA
Soft BLK output voltage	Vsblk	0D: 80H 0E: 14H	-	0.2	0.5	V
Clamp cap voltage (POR)	Vcap		6.0	7.0	8.0	V

Total external cut-off current range



AC ELECTRICAL CHARACTERISTICS

(Tamb = 25 °C, V_{CC} = 12V, V_{DD} = V_{DDA} = 5V, ABL input voltage = 5V, HFLB input signal = S3, load resistors = 470Ω, Vin = 0.7Vpp manually adjust video output pins 18, 21 and 24 to 4V DC for the AC test (see 11) unless otherwise stated (see 12))

Table 6. AC Electrical Characteristics

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Contrast max. output voltage	Vcff	03, 05, 06, 07 = FFH 04, 08 — 0C = 80H RGB input = S1	5.0	5.7	6.4	Vpp
Contrast max. output channel difference	Δ Vcff		Δ 10	-	-	%
Contrast center output voltage	Vc80	03, 04, 08 ~ 0C = 80H 05, 06, 07 = FFH RGB input = S1	2.5	2.85	3.2	Vpp
Contrast center output channel difference	Δ Vc80		Δ 10	-	-	%
Contrast max. - Center attenuation	C	C = 20log (Vc80/Vcff)	-8	-6	-4	dB
Sub contrast center output voltage	Vd80	03 = FFH 04 — 0C = 80H RGB input = S1	2.3	2.6	2.9	Vpp
Sub contrast center output channel difference	Δ Vd80		Δ 10	-	-	%
Sub contrast min. output voltage	Vd00	03 = FFH, 05—07: 00H 04, 08 — 0C = 80H RGB input = S1	1.3	1.6	1.9	Vpp
Sub contrast min. output channel difference	Δ Vd00		Δ 10	-	-	%
Sub contrast max. - min. attenuation	D	D = 20log (Vd00/Vcff)	-14	-12	-10	dB
ABL control range	ABL	(see 15)	-12	-10	-8	dB
R/G/B video rising time (see 7)	tr (video)	03, 05 ~ 07: FFH 04, 08 ~ 0C: 80H RGB input = S2	-	2.2	2.8	ns
R/G/B video falling time (see 7)	tf (video)		-	2.2	2.8	ns
R/G/B blank output rising time (see 7)	tr (blank)	POR HFLB: S4	-	6.0	12.0	ns
R/G/B blank output falling time (see 7)	tf (blank)		-	8.0	15.0	ns
R/G/B video band width (see 7, 8)	f (-3dB)	(see 16)	175	-	-	MHz
Video AMP 50MHz cross talk	CT_50M (see7, 9)	(see 17)	-	-25	-20	dB
Video AMP 130MHz cross talk	CT_130M (see7, 9)	(see 18)	-	-15	-10	dB
Absolute gain match	Avmatch (see 6)		-1	-	1	dB
Gain change between amplifier	Avtrack (see 7)		-1	-	1	dB

OSD ELECTRICAL CHARCTERISTICS

(Tamb = 25 °C, V_{CC} = 12V, V_{DD} = V_{DDA} = 5V, HFLB input voltage = S3, load rosistors = 470Ω, V-AMP test registors FBLK, OSD input conditions unless otherwise stated)

Table 7. OSD Electrical Chaacteristics

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
OSD contrast max. output voltage	Vocff	08 = FFH OSD RGB output conditions	5.4	6.4	7.4	Vpp
OSD contrast max. output channel difference	Δ Vocff		Δ 10	-	-	%
OSD contrast center output voltage	Voc80	08 = 80H OSD RGB output conditions	2.7	3.2	3.7	Vpp
OSD contrast center output channel difference	Δ Voc80		Δ 10	-	-	%
R/G/B OSD rising time	tr (OSD)	08: FFH	-	4.0	5.0	ns
R/G/B OSD falling time	tf (OSD)		-	4.0	5.0	ns
HT video level	HTvideo	ABL = 6V RGB input = S1 03, 05 — 08: FFH 0D: 01H OSD black conditions input HTvideo = 20log($V_{htvideo}$/V_{cff})	-6.0	-4.5	-3.0	dB
HT video output channel difference	Δ HTvideo		Δ 15	-	-	%
HT OSD level	HTosd	ABL = 6V 05 — 08: FFH 0D: 0FH OSD white condition input HTosd = 20log (V_{htosd}/V_{ocff})	-7.0	-5.5	-4.0	dB
HT OSD output channel difference	Δ HTosd		Δ 15	-	-	%

OPERATION TIMINGS

Table 8. Operation Timings

Parameter	Symbol	Min	Typ	Max	Unit
Input Signal HFLB, VFLB					
Horizontal flyback signal frequency	f_{HFLB}	-	-	120	kHz
Vertical flyback signal frequency	f_{VFLB}	-	-	200	Hz
I^{2}C Interface SDA, SCL (Refer to Figure 3)					
SCL clock frequency	f_{SCL}	-	-	300	kHz
Hold time for start condition	t_{hs}	500	-	-	ns
Set up time for stop condition	t_{sus}	500	-	-	ns
Low duration of clock	t_{low}	400	-	-	ns
High duration of clock	t_{high}	400	-	-	ns
Hold time for data	t_{hd}	0	-	-	ns
Set up time for data	t_{sud}	500	-	-	ns
Time between 2 access	t_{ss}	500	-	-	ns
Fall time of SDA	t_{fSDA}	-	-	20	ns
Rise time of both SCL and SDA	t_{rSDA}	-	-	-	ns

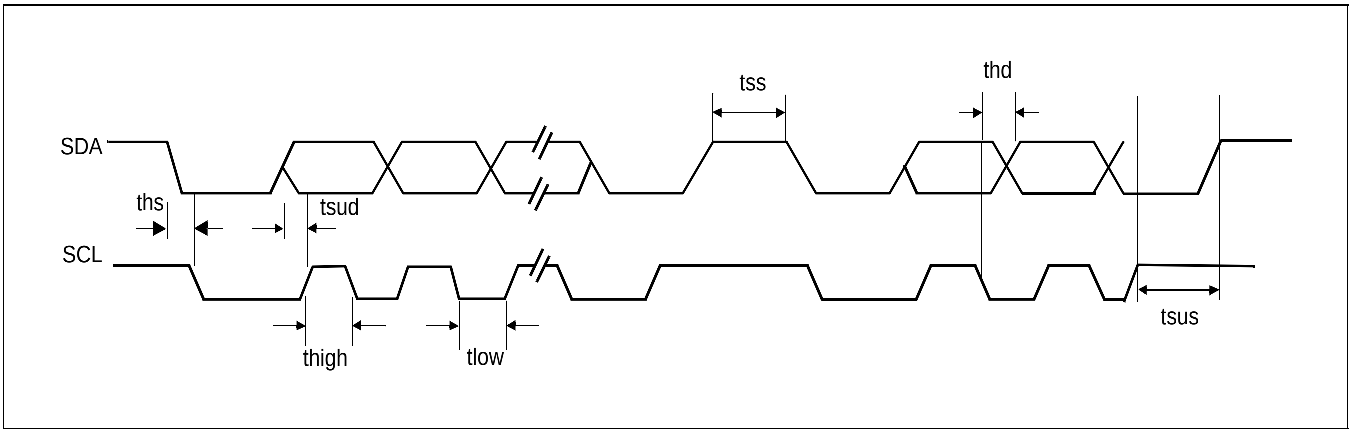


Figure 3. I^{2}C Bus Timing Diagram

OSD PART ELECTRICAL CHARACTERISTICS

OSD PART DC ELECTRICAL CHARACTERISTICS

(Ta = 25 °C, V_{DDA} = V_{DD} = 5V)

Table 9. OSD Part DC Electrical Characteristics

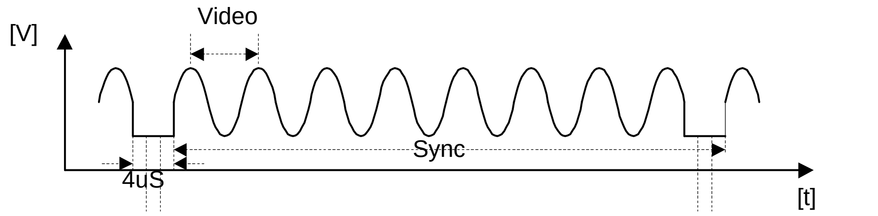
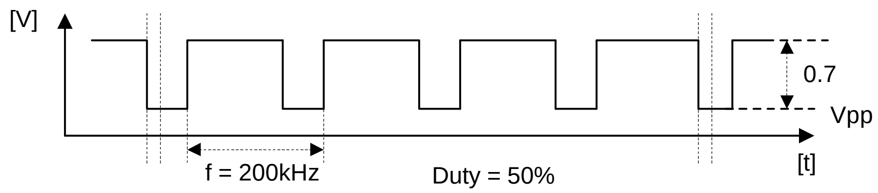
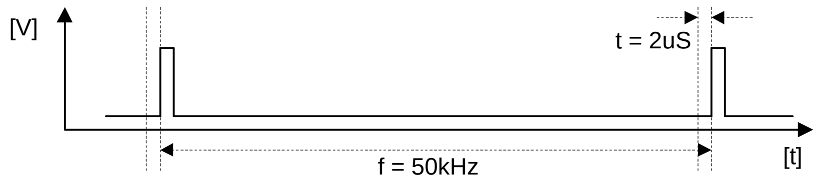
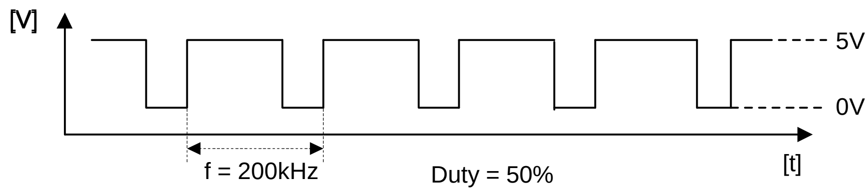
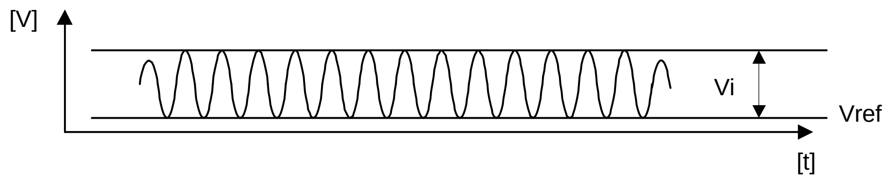
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Supply current (no load on any output)	I_{DD}	-	-	25	mA
Input voltage	V_{IH}	$0.8V_{DD}$	-	-	V
	V_{IL}	-	-	V_{SS} + 0.4	V
Output voltage (Iout = ±1mA)	V_{OH}	$0.8V_{DD}$	-	-	V
	V_{OL}	-	-	V_{SS} + 0.4	V
Input leakage current	I_{IL}	-10	-	10	µA
VCO input voltage	V_{VCO}		2.5		V

NOTES:

1. Absolute maximum rating indicates the limit beyond which damage to the device may occur.
2. Operating ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the electrical characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
3. VCC supply pins 11, 13, and 22 must be externally wired together to prevent internal damage during VCC power on/off cycles.
4. The supply current specified is the quiescent current for VCC1/VCC2 and VCC3 with RL = ∞, The supply current for VCC2 (pin 22) also depends on the output load.
5. Output voltage is dependent on load resistor. Test circuit uses RL = 470Ω
6. Measure gain difference between any two amplifiers Vin = 700mVpp.
7. When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended. Video amplifier 50MHz cross talk test also requires this printed circuit board. The reason for a double sided full ground plane PCB is that large measurement variations occur in single sided PCBs.
8. Adjust input frequency from 10MHz (AV max reference level) to the -3dB frequency (f -3dB).
9. Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at fin = 50MHz for cross talk 50MHz.
10. A minimum pulse width of 200 ns is guaranteed for a horizontal line of 15kHz. This limit is guaranteed by design. if a lower line rate is used a longer clamp pulse may be required.
11. During the AC test the 4V DC level is the center voltage of the AC output signal. For example. If the output is 4Vpp the signal will swing between 2V DC and 6V DC.
12. These parameters are not tested on each product which is controlled by an internal qualification procedure.
13. The conditions block's 03, 04, 05... etc. signify sub address'0F03, 0F04, 0F05... etc.
14. Sub address 0F03, 0F05 ~ 0F07: FFH
    0F04, 0F08 ~ 0F0C: 80H
    RGB input = S1,
    When the ABL input voltage is 0V, the R/G/B's output voltage is VR/VG/VB and uses the formula ABLR = 20log (VR/V_{cffR})
15. OSD TST mode = High, CLP operation off,
    RGB input = S5 (frequency sweep),
    RGB input clamp cap = 2.1V DC,
    RGB clamp cap (pin 23/20/17) = Vcap voltage (7.0V),
    S5's frequency 1MHz → 130MHz sweep, -3dB point = 20log (V_{130MHz}/V_{1MHz})
    03, 05 ~ 07: FFH
    04, 08 ~ 0C: 80H
    0F: 80H
16. OSD TST mode = High, CLP operation off,
    RGB input clamp cap = 2.1V DC,
    RGB clamp cap (pin 23/20/17) = Vcap voltage (7.0V),
    03, 05 ~ 07: FFH
    04, 08 ~ 0C: 80H
    0F: 80H
    R input = S5 (50MHz)
    CT_50M = 20log (V_{outG}/V_{outR}) or 20log (V_{outB}/V_{outR})
17. OSD TST mode = High, CLP operation off,
    RGB input clamp cap = 2.1V DC,
    RGB clamp cap (pin 23/20/17) = Vcap voltage (7.0V),
    03, 05 ~ 07: FFH
    04, 08 ~ 0C: 80H
    0F: 80H
    R input = S5 (130MHz)
    CT_150M = 20log (V_{outG}/V_{outR}) or 20log (V_{outB}/V_{outR})

TEST SIGNAL FORMAT

Table 10. Test Signal Format

Signal Name	Input Signal Formal	Signal Description
S1		Video gain measurement Video = 1MHz/0.7Vpp Sync = 50kHz
S2		Video Tr/Tf measurement f = 200kHz V = 0.7Vpp Duty = 50%
S3		HFLB (posi & nega.) input f = 50kHz t = 2uS V = 0V/5V
S4		OSD level measurement Blank Tr/Tf measurement f = 50kHz V = 0V/5V
S5		Crosstalk test Bandwidth measurement 1MHz/10MHz/50MHz/ 130MHz Vref = input clamp voltage Vi = 0.7Vpp

- S1, S2 signal's low level must be synchronized with the S3 signal's sync. term.
- The input signal level uses the IC pin as reference.

TEST CIRCUIT

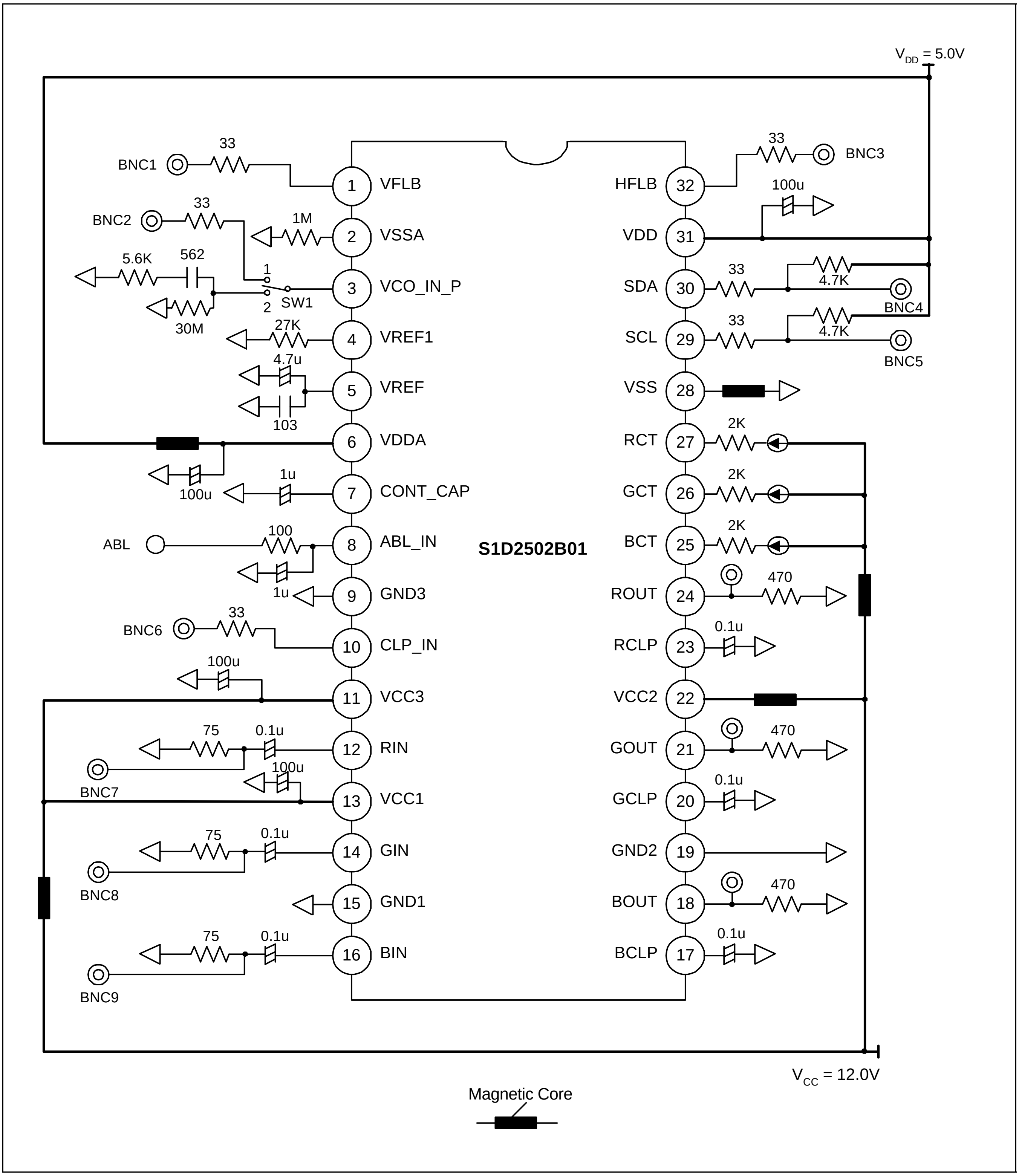


Figure 4. Test Circuit

FUNCTIONAL DESCRIPTIONS

DATA TRANSMISSION

The interface between S1D2502B01 and MCU follows the I^2C protocol. After the starting pulse, the transmission takes place in the following order: Slave address with R/W bit, 2-byte register address, 2-byte data, and stop condition. an acknowledge signal is received for each byte, excluding only the start/stop condition. The 2-byte register address is composed of an 8-bit row address, and an 8-bit column address. The order of transmission for a 2-byte register address is 'Row address → Column address'. The 2 bytes of data is because S1D2502B01 has a 16-bit base register configuration. S1D2502B01's slave address is BAh. It is BBh in read mode, and BAh in write mode.

- **Address Bit Pattern for Display Registers Data**
  (a) row address bit pattern
  R3 - R0: Valid data for row address

A15	A14	A13	A12	A11	A10	A9	A8
X	X	X	X	R3	R2	R1	R0

(b) Column address bit pattern
C4 - C0: Valid data for column address

A7	A6	A5	A4	A3	A2	A1	A0
X	X	X	C4	C3	C2	C1	C0

X:Don't care bit

- **Data Transmission Format**

Start → Slave address → ACK → Row address → ACK → Column address → ACK
Data byte N → ACK → Data byte N+1 → ACK → Stop

Figure 5. Data Transmission Format at Writing Operation

Start → Slave address → ACK → Row address → ACK → Column address → ACK → Stop
Start → Slave address → ACK → Data byte N → ACK → Data byte N+1 → ACK → Stop

Figure 6. Data Transmission Format at Reading Operation

- **SDA / SCL Signal At Communication**

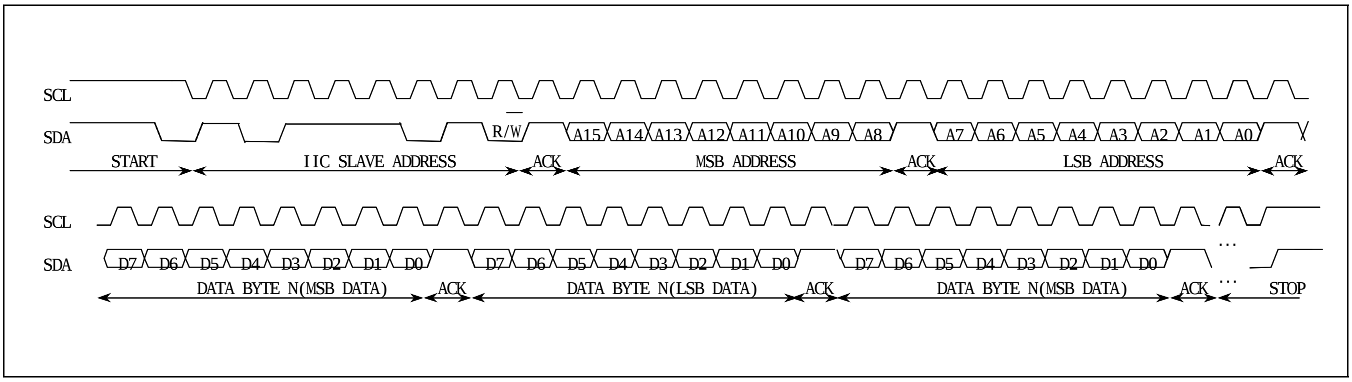


Figure 7. SDA line and SCL line (Write Operation)

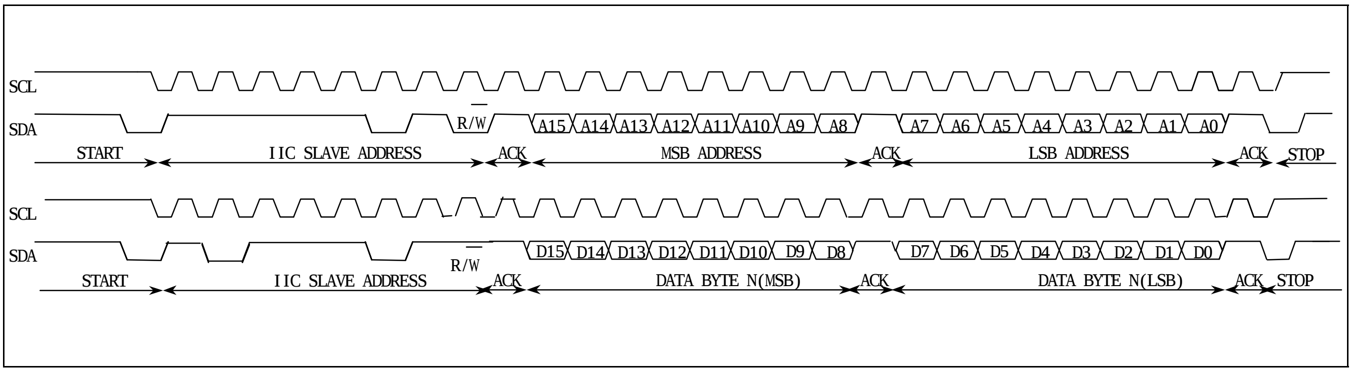


Figure 8. SDA line and SCL line (Read Operation)

MEMORY MAP

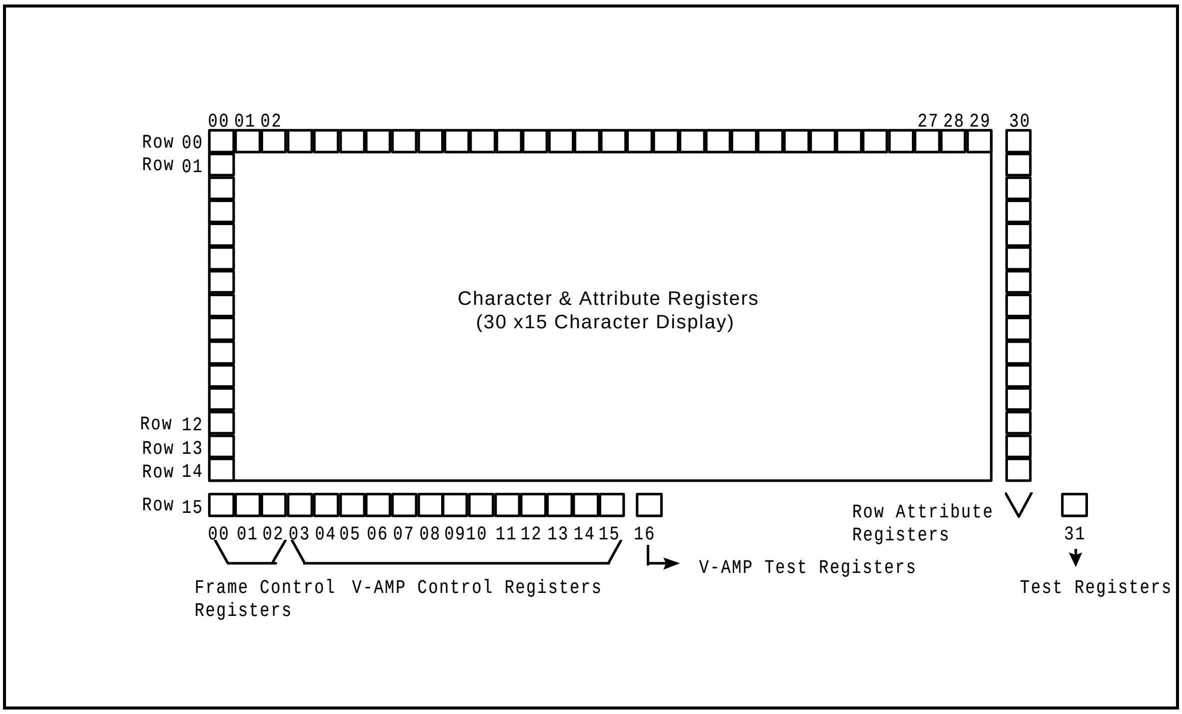


Figure 9. Memory Map of Display Registers

The display RAM's address of the row and column number are assigned in order. The display RAM is composed of 4 register groups (character & attribute register, row attribute register, frame control register, and V-AMP control register).

The display area in the monitor screen is 30 column $\times$ 15 row, so the related character & attribute registers are also 30 column $\times$ 15 row. Each register has a character address and characteristics corresponding to the display location on the screen, and one register is composed of 16 bits. The lower 9 bits select the font from the 448 ROM fonts, and the upper 7 bits give font characteristics to the selected font.

The row attribute register takes up the display RAM's 31st column. It provides raster color, raster color intensity, character color intensity, horizontal & vertical character size, box, border, and shadow features in units of row.

The frame control registers are in the 16th row. It controls OSD's display location, character height, scroll, and fade-in/out in units of frame.

The V-AMP control registers are also located in the 16th row.

REGISTER DESCRIPTION

Character & Attribute Register: Row00 ~ 14, Column00 ~ 29

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
BINV	BOX1	BOX0	B	G	R	Blink/Fint	C8	C7	C6	C5	C4	C3	C2	C1	C0
Character Attribute							Character Code (448 fonts)								

Row Attribute Register: Row00 ~ 14, Column30

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	BREN	INTE	CBil	BOXE	BORD	SHA	RB	RG	RR	RINT	CINT	HZ2	HZ0	VZ1	VZ0
							Raster Color			Intensity		Character Size			

Frame Control Register 0: Row15, Column00

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	Fde	FdeT	VPOL	HPOL	-	-	-	-	Erase	EN	Scrl	ScrT	Bli1	Bli0	BliT

Frame Control Register 1: Row15, Column01

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
CP1	CP0	Fpll	HF2	HF1	HF0	dot1	dot0	-	FBLK	CH5	CH4	CH3	CH2	CH1	CH0
PLL Control										Character Height Control					

Frame Control Register 2: Row15, Column02

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
Horizontal Start Position								Vertical Start Position							

V-AMP Control Register: Row15, Column03 ~ 15

Column03

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	--	-	-	-	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
								Contrast Control							

Column04

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	--	-	-	-	BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0
								Brightness Control							

Column05

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	--	-	-	-	RSB7	RSB6	RSB5	RSB4	RSB3	RSB2	RSB1	RSB0
								R SUB Contrast Control							

Column06

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	--	-	-	-	GSB7	GSB6	GSB5	GSB4	GSB3	GSB2	GSB1	GSB0
								G SUB Contrast Control							

¨ V-AMP Control Register: Row15, Column03 ~ 15

Column07

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	BSB7	BSB6	BSB5	BSB4	BSB3	BSB2	BSB1	BSB0

Bits 7–0: B SUB Control

Column08

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	OSD7	OSD6	OSD5	OSD4	OSD3	OSD2	OSD1	OSD0

Bits 7–0: OSD Contrast Control

Column09

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	RWB7	RWB6	RWB5	RWB4	RWB3	RWB2	RWB1	RWB0

Bits 7–0: R Cut-off Control

Column10

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	GWB7	GWB6	GWB5	GWB4	GWB3	GWB2	GWB1	GWB0

Bits 7–0: G Cut-off Control

Column11

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	BWB7	BWB6	BWB5	BWB4	BWB3	BWB2	BWB1	BWB0

Bits 7–0: B Cut-off Control

Column12

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	CUT7	CUT6	CUT5	CUT4	CUT3	CUT2	CUT1	CUT

Bits 7–0: Cut-off Brightness Control

Column13

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	SB	HS6	HS5	HS4	HS3	HS2	HS1	HT

Bits 7–0: Half Tone & Soft Blank Control

Column14

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	CLPS	CLPP	BLKP	BPW2	BPW1	-	CS2	CS1

Bits 7–0: Clamp, Polarity & Offset Control

Column15

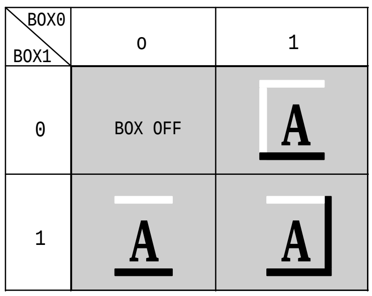
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	TST	HS9	HS8	HS7

Bits 2–0: Half Tone Control

' **-** '; Dont care bit

Figure 10. Register Description

Table 11. Register Description

<table>
<tr><th>Registers</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="5">Character & Attribute Registers
(Row 00 — 14,
Column 00 — 29)</td><td>C8 — C0
(Bit 8 — 0)</td><td>Character code address
This is the address of 448 ROM fonts.</td></tr>
<tr><td>Blink/FINT
(Bit 9)</td><td>Character blinking/font intensity
If row attribute register's INTE bit is set to '1', this bit carries out the font intensity feature, and if not, the character blinking feature instead. In other words, to carry out character blinking, set the INTE bit to '0'. Select frame control register-0's BliT bit as blinking time, and select Bli1, Bli0 Bit as blinking duty. When giving intensity in units of font, refer to the table below.
<table>
<tr><th>Blink/FINT</th><th>INTE</th><th>RINT</th><th>CINT</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>-</td><td>-</td><td>Normal</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>-</td><td>Normal</td></tr>
<tr><td>1</td><td>0</td><td>-</td><td>-</td><td>Blink</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Character intensity</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Raster intensity</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Character & raster intensity</td></tr>
</table></td></tr>
<tr><td>B, G, R
(Bit C — A)</td><td>Character color
The character color is chosen from 16 colors using these 3 bits and the row attribute register's CINT bit.</td></tr>
<tr><td>BOX1, BOX0
(Bit E, D)</td><td>Character box drawing
You can make 4 box drawing modes using these 2 bits in combination. The box drawings possible with font 'A' are shown below.


Refer to row attribute register's 'BOXE' bit.</td></tr>
<tr><td>BINV
(Bit F)</td><td>Box inversion
The white box turns black and black box turns white in the box drawing using BOX1, BOX0.</td></tr>
</table>

Table 11. Register Description (Continued)

<table>
<tr><th>Registers</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="4">Row Attribute Registers (Row00— 14, Column30)</td><td>VZ1, VZ0
(Bit 1, 0)</td><td>Vertical character size control
<table><tr><th>VZ1</th><th>VZ0</th><th>Vertical Character Size</th></tr><tr><td>0</td><td>0</td><td>1X (1 time)</td></tr><tr><td>0</td><td>1</td><td>2X (2 times)</td></tr><tr><td>1</td><td>0</td><td>3X (3 times)</td></tr><tr><td>1</td><td>1</td><td>4X (4 times)</td></tr></table>As shown above, the vertical character size is decided by using these two bits in combination.</td></tr>
<tr><td>HZ1, HZ0
(Bit 3, 2)</td><td>Horizontal character size control
<table><tr><th>HZ1</th><th>HZ0</th><th>Horizontal Character Size</th></tr><tr><td>0</td><td>0</td><td>1X (1 time)</td></tr><tr><td>0</td><td>1</td><td>2X (2 times)</td></tr><tr><td>1</td><td>0</td><td>3X (3 times)</td></tr><tr><td>1</td><td>1</td><td>4X (4 times)</td></tr></table>As shown above, the horizontal character size is decided by using these two bits in combination. However, unlike VZ, the surrounding area (row) is taken over in the amount of the HZ increase, so you must keep that in mind when changing font size. Refer to Character Size.</td></tr>
<tr><td>CINT
(Bit 4)</td><td>Character color intensity
When this bit is set to '1', the color intensity of the character on the same row becomes high. Refer to BLINK/FINT, INTE, RINT, and CINT's combination chart in the previous page. (Even if you change this bit, you can't check the intensity feature on the demo board. This is because the OSD IC's output INT is applied as the video Pre Amp's input, and the demo board doesn't apply the OSD IC's INT output to the Pre Amp.)</td></tr>
<tr><td>RINT
(Bit 5)</td><td>Raster color intensity
When this bit is set to '1', the color intensity of the raster on the same row becomes high. Refer to BLINK/FINT, INTE, RINT, and CINT's combination chart in the previous page. (Like CINT given above, you can't check RINT's feature on the demo board.)</td></tr>
</table>

Table 11. Register Description (Continued)

Registers	Bits	Description
Row Attribute Registers (Row00 — 14, Column30)	RB, RG, RR (Bit 8 — 6)	Raster color is determined by these bits The raster color is chosen from out of 16 colors using these 3 bits and the row attribute register's 'RINT' bit. If 'BOXE' Bit is not '1', the setting of these three bits have no meaning. Refer to 'BOXE' bit shown below.
	SHA	Character shadowing Character shadowing feature is carried out if you set this bit to '1'.
	BORD	Character bordering Character bordering feature is carried out if you set this bit to '1'.
	BOXE (Bit B)	BOX enable If you set this bit to '1', it uses the character & attribute register's 'BINV', 'BOX1', and 'BOX0' bits to carry out box drawing, and if you set it to '0', the character & attribute register's bits F~D (BINV, BOX1, BOX0) act as each raster color's B, G, and R. This has higher priority than selection by setting RB, RG, and RR bits. In other words, if the BOXE bit is set to '0', the character & attribute register's BINV, BOX1, and BOX0 each do the function of RB, RG, and RR to decide the raster color, and the original row attribute register's RB, RG, and RR don't do anything.
	CBli (Bit C)	Color blink enable If this bit is '1', the color blinking effect is applied. Color blinking is instead of normal blinking, 8 colors appear in order in the font's character part. Its time and duty is controlled by 'BliT', 'Bli1', and 'Bli0', like in character blinking.
	INTE (Bit D)	Intensity enable Refer to the table on the combination of BLINK/FINT, INTE, RINT, and CINT bits in the explanation of the character & attribute register's BLINK/FINT bit.
	BREN (Bit E)	Back raster enable If the BREN bit is '1' and the raster color is black, the raster is transparent. That is, the video back raster is shown. If not, the OSD raster covers the video's back raster. Refer to other color effect.
	Bit F	Reserved

Table 11. Register Description (Continued)

<table>
<tr><th>Registers</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="6">Frame Control Registers — 0 (Row 15, Column 00)</td><td>BliT
(Bit 0)</td><td>Blink time control
If this bit is '1', blink time is 0.5sec, and if not, 1sec.</td></tr>
<tr><td>Bli1, Bli0
(Bit 2 — 1)</td><td>Blinking duty control
As the font blinks, there is a time when it is visible and invisible on screen. Blinking duty is the ratio of the invisible time to the visible time, and is decided by the combination of these two bits. In other words, blinking duty is the length of time the font is shown on screen.
<table>
<tr><th>Bli1</th><th>Bli0</th><th>Blinking Duty</th></tr>
<tr><td>0</td><td>0</td><td>Blink Off</td></tr>
<tr><td>0</td><td>1</td><td>Duty 25%</td></tr>
<tr><td>1</td><td>0</td><td>Duty 50%</td></tr>
<tr><td>1</td><td>1</td><td>Duty 75%</td></tr>
</table></td></tr>
<tr><td>ScrT
(Bit 3)</td><td>Scroll time control
If this bit is '1', scroll time is 0.5sec, and if not, 1sec.</td></tr>
<tr><td>Scrl
(Bit 4)</td><td>Scroll enable
Scrolling effect is controlled by this bit. If this bit is '1', scrolling effect is enabled. You must remember that scrolling can be turned on/off only when OSD is enabled/disabled.</td></tr>
<tr><td>EN
(Bit 5)</td><td>OSD enable
OSD is enabled when this bit is '1'. In other words, if this bit isn't '1'OSD is not output inspite of writing control data. We recommend that you enable the OSD after setting the control registers (such as the character & attribute register) because of video and OSD output timing.</td></tr>
<tr><td>Erase
(Bit 6)</td><td>RAM erasing
If this bit is '1', the RAM data (character & attribute registers and row attribute registers) is erased. The time spent in carrying out this operation is called erasing time, which can be calculated as follows.

Erasing time = RAM clock $\times$ 480 (RAM cell no.)
RAM clock = 12 dot clock
Dot clock = 1/(dot frequency)
Dot frequency = Horizontal frequency $\times$ resolution (mode)

Therefore, the maximum erasing time value is:

$(\text{Erasing Time})_{MAX} = (12 \times 480) / (15k \times 320) = 1.2ms$</td></tr>
</table>

Table 11. Register Description (Continued)

Registers	Bits	Description
Frame Control Registers — 0 (Row 15, Column 00)	HPOL (Bit B)	Polarity of horizontal fly back signal If this bit is '1', HFLB's polarity is positive, and if '0', it is negative. In other words, this bit is set to '1' if active high, and '0' if active low.
	VPOL (Bit C)	Polarity of vertical fly back signal If this bit is '1', VFLB's polarity is positive, and if '0', it is negative. In other words, this bit is set to '1' if active high, and '0' if active low.
	FdeT (Bit D)	Fade-in and fade-out time control If this bit is '1', fade-in/fade-out time is 0.5sec. If not, it is 1sec.
	Fde (Bit E)	Fade-in and fade-out enable This feature is enabled when this bit is '1'. The effect where the display goes from the center to the outside, or from the outside to the center in units of font, is called fade-in/fade-out. Refer to fade-in/fade-out. You must remember that fade-in/fade-out, like scrolling on/off, only occurs when OSD enabled/disabled.
	Bit F	Reserved.

The purpose of bits 'HPOL', and 'VPOL' is to provide flexibility when using the S1D2502B01 IC. No matter which polarity you choose for the input signal, the IC will handle them identically, so you can select active high or active low according to your convenience.

Tabel 4. Register Description (Continued)

<table>
<tr><th>Registers</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="5">Frame Control
Registers — 1
(Row 15,
Column 01)</td><td>CH5 — CH0
(bit 5 — 0)</td><td>Character height control
While the purpose of VZ[1:0] (vertical character height) is to control the absolute size of the character, the purpose of CH[5:0] (Character Height) is to output OSD of a uniform size even if the resolution changes. If you adjust the value in the range of CH = 18 — CH = 63, each line's repeating number is decided (standard height CH = 18 is the reference value), by which the line is repeated. For more information on repeating number selection, refer to character height.</td></tr>
<tr><td>FBLK
(bit 6)</td><td>Selection of the FBLK output pin's configuration
Unlike pin description's FBLK, if this bit is '0', the FBLK pin output is high while the character and raster are being displayed and the character and raster are output as they are. If this bit is '1', the FBLK pin output becomes high only when character is being displayed, so only the character is output. Refer to 'Figure 11. Character/raster signal part.</td></tr>
<tr><td>dot1, dot0
(bit 9, 8)</td><td>Resolution control (dots/line)
<table><tr><th>Dot1</th><th>Dot0</th><th>No. of Dots</th></tr><tr><td>0</td><td>0</td><td>320 dots/line</td></tr><tr><td>0</td><td>1</td><td>480 dots/line</td></tr><tr><td>1</td><td>0</td><td>640 dots/line</td></tr><tr><td>1</td><td>1</td><td>800 dots/line</td></tr></table>As shown above, the number of dots per horizontal line is decided by a combination of these two bits.</td></tr>
<tr><td>HF2— HF0
(bit C — A)</td><td>Horizontal frequency
PLL's horizontal frequency is decided by the combination of these 3 bits. This is related to the selection of DOT[1:0], so you can't numerically express the frequency range with only the HF[2:0] selection. For more information, please refer to HF Bits Selection.</td></tr>
<tr><td>FPLL
(bit D)</td><td>Full range PLL
If this bit is '1', the OSD_PLL block's VCO operates at full range (4.8MHz - 96MHz). If it is 0', it operates within the region decided by the HF bit [C:A] explained above. if you cant optimize OSD screen decided by the HF bit in the high region, you may set the FPLL bit to 1.'</td></tr>
</table>

Tabel 4. Register Description (Continued)

<table>
<tr><th>Registers</th><th>Bits</th><th>Description</th></tr>
<tr><td>Frame Control Registers — 1 (Row 15, Column 01)</td><td>CP1, CP0</td><td>Charge pump output current control
This is the PLL block's internal phase detector output status, converted into current. Refer to PLL control.
<table><tr><th>CP1</th><th>CP0</th><th>Charge Pump Current</th></tr><tr><td>0</td><td>0</td><td>0.50 mA</td></tr><tr><td>0</td><td>1</td><td>0.75 mA</td></tr><tr><td>1</td><td>0</td><td>1.00 mA</td></tr><tr><td>1</td><td>1</td><td>1.25 mA</td></tr></table>The output is decided by the combination of these two bits.</td></tr>
</table>

FBLK bit setting is explained at the figure below.

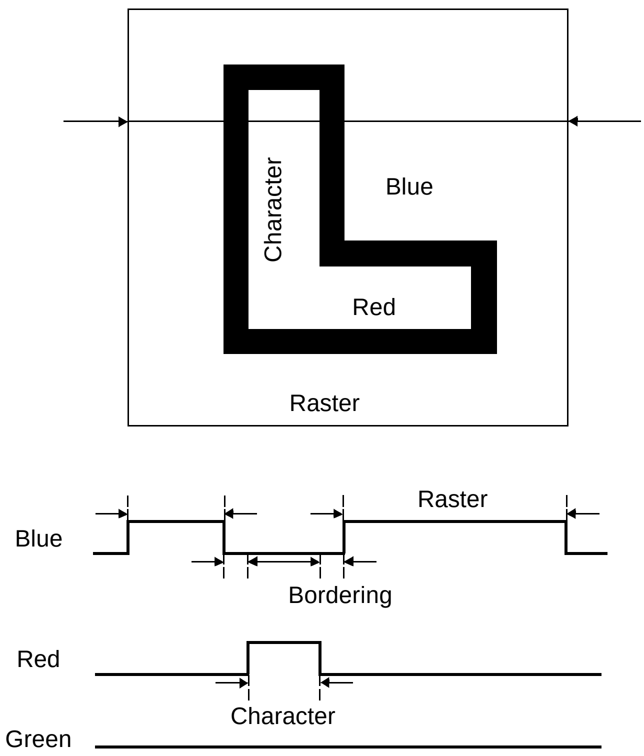


Figure 11. Character/Raster Signal Part

Tabel 4. Register Description (Continued)

Registers	Bits	Description
Frame Control Registers — 2 (Row 15, Column 02)	VP7 — VP0	Vertical start position control (= VP[7:0] × 4) Signifies top margin height from the V-Sync reference edge.
	HP7 — HP0	Horizontal start position control (= HP[7:0] × 6) Signifies delay of the horizontal display from the H-Sync reference edge to the character's 1st pixel location.
V-AMP Control Registers — 0 (Row 15, Column 03)	VC7 — VC0 (bit7 — 0)	The contrast adjustment is made by contrdling simultaneously the gain of three internal variable gain amplifiers. The contrast adjustment allows to cover a typical range of 38dB.
V-AMP Control Registers — 1 (Row 15, Column 04)	BRT7 — BRT0 (bit7 — 0)	The brightness adjustment controls to add the same black level (pedestal) to the 3-channel R/G/B signals after contrast amplifier.
V-AMP Control Registers — 2 (Row 15, Column 05)	RSB7 — RSB0 (bit7 — 0)	R channel SUB contrast control. The SUB contrast adjustment is used to adjust the white balance, and the gain of each channel is controlled. The SUB contrast adjustment allows you to cover a typical tange of 12dB.
V-AMP Control Registers - 3 (Row 15, Column 06)	GSB7 — GSB0 (bit7 — 0)	G channel SUB contrast control. The SUB contrast adjustment is used to adjust the white balance, and the gain of each channel is controlled. The SUB contrast adjustment allows you to cover a typical tange of 12dB.
V-AMP Control Registers - 4 (Row 15, Column 07)	BSB7 — BSB0 (bit7 — 0)	B channel SUB contrast control. The SUB contrast adjustment is used to adjust the white balance, and the gain of each channel is controlled. The SUB contrast adjustment allows you to cover a typical tange of 12dB.
V-AMP Control Registers - 5 (Row 15, Column 08)	OSD7 — OSD0 (bit7 — 0)	The OSD contrast adjustment is made by contrdling simultaneously the gain of three internal variable gain amplifiers. The OSD contrast adjustment allows to cover a typical range of 38dB.
V-AMP Control Registers - 6 (Row 15, Column 09)	RWB7 — RWB0 (bit7 — 0)	R channel cut-off control. The cut-off adjustment is used to adjust the raster white balance.
V-AMP Control Registers - 7 (Row 15, Column 10)	GWB7 — GWB0 (bit7 — 0)	G channel cut-off control. The cut-off adjustment is used to adjust the raster white balance.

Tabel 4. Register Description (Continued)

<table>
<tr><th>Registers</th><th>Bits</th><th>Description</th></tr>
<tr><td>V-AMP Control Registers - 8
(Row 15,
Column 11)</td><td>BWB7 — BWB0
(bit7 — 0)</td><td>B channel cut-off control.
The cut-off adjustment B used to adjust the raster white balance.</td></tr>
<tr><td>V-AMP Control Registers - 9
(Row 15,
Column 12)</td><td>CUT7 — CUT0
(bit7 — 0)</td><td>The cut-off brightness adjustment is made by simultaneously controlling the external cut-off current.</td></tr>
<tr><td rowspan="4">V-AMP Control Registers - 10
(Row 15,
Column 13)</td><td>HT
(bit 0)</td><td>Video & OSD half tone enable.
If you set this bit to '1', the half tone function is on.
Then you can see the video signal & OSD raster.</td></tr>
<tr><td>HS3 — HS1
(bit3 — 1)</td><td>HS3 — HS1 bits select OSD raster color 1 to be half tone.
To carry out half tone function, set the HT bit to '1'.
<table>
<tr><th rowspan="2">HS3</th><th rowspan="2">HS2</th><th rowspan="2">HS1</th><th colspan="3">OSD</th><th rowspan="2">Raster Color 1</th><th rowspan="2">POR</th></tr>
<tr><th>G</th><th>R</th><th>B</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Black</td><td>O</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Blue</td><td></td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Red</td><td></td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Magenta</td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Green</td><td></td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>Cyan</td><td></td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Yellow</td><td></td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>White</td><td></td></tr>
</table></td></tr>
<tr><td>HS6 — HS4
(bit6 — 4)</td><td>HS6 — HS4 bits select OSD raster color 2 to be half tone.
To carry out half tone function, set the HT bit to '1'.
<table>
<tr><th rowspan="2">HS6</th><th rowspan="2">HS5</th><th rowspan="2">HS4</th><th colspan="3">OSD</th><th rowspan="2">Raster Color 2</th><th rowspan="2">POR</th></tr>
<tr><th>G</th><th>R</th><th>B</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Black</td><td>O</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Blue</td><td></td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Red</td><td></td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Magenta</td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Green</td><td></td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>Cyan</td><td></td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Yellow</td><td></td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>White</td><td></td></tr>
</table></td></tr>
<tr><td>SB
(bit 7)</td><td>Soft blanking enable
If you set this bit '1', the R/G/B outputs go to GND.</td></tr>
</table>

Tabel 4. Register Description (Continued)

<table>
<tr><th>Registers</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="5">V-AMP Control Registers - 11 (Row 15, Column 14)</td><td>CS2 — CS1
(bit1 — bit0)</td><td>Cut-off offset current control
<table>
<tr><th>CS2</th><th>CS1</th><th>Cut-off Offset Current</th><th>POR</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>O</td></tr>
<tr><td>0</td><td>1</td><td>50µA</td><td></td></tr>
<tr><td>1</td><td>0</td><td>100µA</td><td></td></tr>
<tr><td>1</td><td>1</td><td>150µA</td><td></td></tr>
</table></td></tr>
<tr><td>BPW2 — BPW1
(bit4 — bit3)</td><td>Generated clamp pulse width control
<table>
<tr><th>BPW2</th><th>BPW1</th><th>Width</th><th>POR</th></tr>
<tr><td>0</td><td>0</td><td>0.33µs</td><td></td></tr>
<tr><td>0</td><td>1</td><td>0.66µs</td><td></td></tr>
<tr><td>1</td><td>0</td><td>1.00µs</td><td>O</td></tr>
<tr><td>1</td><td>1</td><td>1.33µs</td><td></td></tr>
</table>
To carry out this function, set the CLPS bit to " 0 "</td></tr>
<tr><td>BLKP
(bit 5)</td><td>Polarity of horizontral fly back signal
If this bit is '0', HFLB's polarity is negative, and if '1', it is positive.</td></tr>
<tr><td>CLPP
(bit 6)</td><td>Polarity of clamp pulse signal
If this bit is '0', CLP's polarity is positive, and if '1', it is negative.
This bit has meaning only if the CLPS bit is set to '1'.</td></tr>
<tr><td>CLPS
(bit 7)</td><td>Clamp pulse generation enable
If this bit is '0', clamp signal is made using the HFLB signal, so there is no need to supply the clamp signal.
and if '1'you must supply external clamp signal.</td></tr>
<tr><td>V-AMP Control Registers - 12 (Row 15, Column 15)</td><td>HS9 — HS7
(bit2 — bit 0)</td><td>HS9 — HS7 bits select OSD raster color 3 to be half tone.
To carry out half tone function, set the HT bit to " 1 ".
<table>
<tr><th rowspan="2">HS9</th><th rowspan="2">HS8</th><th rowspan="2">HS7</th><th colspan="3">OSD</th><th rowspan="2">Raster Color 3</th><th rowspan="2">POR</th></tr>
<tr><th>G</th><th>R</th><th>B</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Black</td><td>O</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Blue</td><td></td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Red</td><td></td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Magenta</td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Green</td><td></td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>Cyan</td><td></td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Yellow</td><td></td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>White</td><td></td></tr>
</table></td></tr>
</table>

VIDEO AMP PART ADDRESS MAP

Register sub address (use limited to 1byte out of 2bytes)

Table 12. Video AMP Part Address Map

SUB Address [Hex]	Function								POR Value [Hex]
	D7	D6	D5	D4	D3	D2	D1	D0	
0F03	Contrast control								80H
0F04	Brightness control								80H
0F05	SUB contrast control (R)								80H
0F06	SUB contrast control (G)								80H
0F07	SUB contrast control (B)								80H
0F08	OSD contrast control								80H
0F09	Cut-off control (R)								80H
0F0A	Cut-off control (G)								80H
0F0B	Cut-off control (B)								80H
0F0C	Cut-off brightness control								80H
0F0D	SB	HS6	HS5	HS4	HS3	HS2	HS1	HT	00H
0F0E	CLPS	CLPP	BLKP	BPW2	BPW1	-	CS2	CS1	10H
0F0F	-	-	-	-	TST	HS9	HS8	HS7	00H

In normal status, you must set TST bit to 0.

Contrast Register (SUB ADRS: 03H) (Vin = 0.7Vpp, bright: 80H, subcont: FFH)

Hex	B7	B6	B5	B4	B3	B2	B1	B0	Contrast (Vpp)	Gain (dB)	int. Value (Hex)
00	0	0	0	0	0	0	0	0	0	-	
80	1	0	0	0	0	0	0	0	2.85	-	O
FF	1	1	1	1	1	1	1	1	5.2	-	
Increment/bit									0.0223		

Brightness Register (3-ch) (SUB ADRS: 04H) (cont: 80H, subcont: 80H)

Hex	B7	B6	B5	B4	B3	B2	B1	B0	Brightness (Vpp)	Int. Value (Hex)
00	0	0	0	0	0	0	0	0	0.2	
80	1	0	0	0	0	0	0	0	1.5	O
FF	1	1	1	1	1	1	1	1	2.7	
Increment/bit									0.01055	

SUB Contrast Register (R/G/B-ch) (SUB ADRS: 05/06/07H)

(Vin = 0.7Vpp, bright: 40H, cont: FFH)

Hex	B7	B6	B5	B4	B3	B2	B1	B0	SUB Contrast (Vpp)	Gain (dB)	Int. Value (Hex)
00	0	0	0	0	0	0	0	0		-	
80	1	0	0	0	0	0	0	0		-	O
FF	1	1	1	1	1	1	1	1		-	
Increment/bit											

OSD Contrast Register (SUB ADRS: 08H) (VOSD = TTL, bright: 80H, subcont: 80H)

Hex	B7	B6	B5	B4	B3	B2	B1	B0	OSD Contrast (Vpp)	Gain (dB)	Int. Value (Hex)
00	0	0	0	0	0	0	0	0	0	-	
80	1	0	0	0	0	0	0	0	3.2	-	O
FF	1	1	1	1	1	1	1	1	6.4	-	
Increment/bit									0.025		

Cut-Off Brightness Register (3-ch) (SUB ADRS: 0CH)

Hex	B7	B6	B5	B4	B3	B2	B1	B0	Cut-Off Brightness (μA)	Int. Value (Hex)
00	0	0	0	0	0	0	0	0	0	
80	1	0	0	0	0	0	0	0	100	O
FF	1	1	1	1	1	1	1	1	200	
Increment/bit									0.781	

Cut-Off Register (R/G/B-ch) (SUB ADRS: 09/0A/0BH)

(cont = 80H, subcont: 80H)

Hex	B7	B6	B5	B4	B3	B2	B1	B0	Cut-Off EXT (μA)	Int. Value (Hex)
00	0	0	0	0	0	0	0	0	0	
80	1	0	0	0	0	0	0	0	300	O
FF	1	1	1	1	1	1	1	1	600	
Increment/bit									2.344	

ADDRESSING

- **Display RAM Structure**

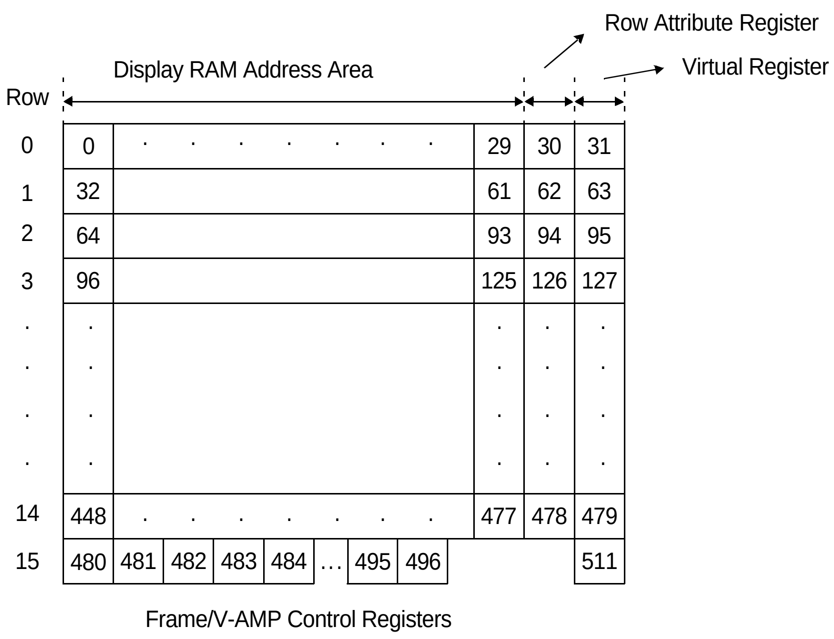


Figure 12. Display RAM Structure & Monitor Display Position

Whereas Figure 9. Memory Map of Display Registers’showed a logical configuration, the Figure above shows a 1KByte SRAM (512 × 16 bit)'s practical and physical configuration. For facilitating internal calculations, addressing is done using exponents of 2, and the rows to the right of the 'Row Attribute Registers', excepting only IFF(255), are 'Virtual Registers' that are not used.

If you set 'Frame Control Register 0's 'Erase' bit to '1', 480 areas are erased (excepting only the 16th line) in the Figure above, and the 'Erasing Time' is measured with 480 areas as the standard.

- **ROM Fonts**
  S1D2502B01 provides 448 Rom fonts for displaying OSD Icons, which allows the use of multi-language OSD Icons. Font $000 is reserved for blank data.

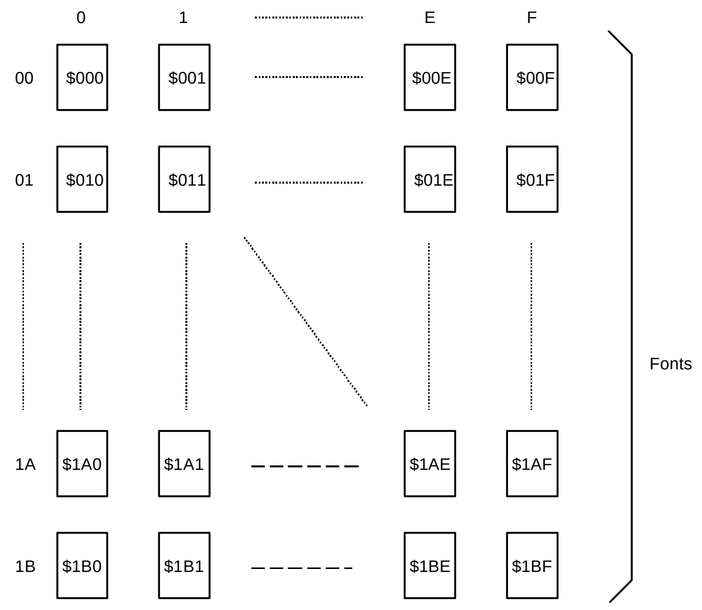


Figure 13. Composition of the ROM Fonts

COLORING

If you have an Intensity feature, the number of possible colors you can express becomes doubled. In other words, the number of colors you can represent with three colors blue, green, and red is 8 (= 2^3), but with the intensity feature, it is 16 (= 2^4).

- **Character Color**
  Character color is assinged for each font, and the 4 components for expressing a color are listed below.

Blue	Character & attribute register's B bit[C]
Green	Character & attribute register's G bit[B]
Red	Character & attribute register's R bit[A]
Intensity	Character & attribute register's BLINK/FINT bit[9] Row attribute register's INTE bit[D] Row attribute register's CINT bit[4] If all 3 bits are set to '1', the character intensity feature is enabled.

- **Raster Color**

Blue	Row attribute register's RB bit[8] if the row attribute register's 'BOXE' bit is '1', and character & attribute register's 'BINV' bit[F] if BOXE' bit is '0'.
Green	Row attribute register's RG bit[7] if row attribute register's 'BOXE' Bit is '1', and character & attribute register's 'BOX1' bit[E] if 'BOXE' bit is '0'.
Red	Row attribute register's RR bit[6] if row attribute register's 'BOXE' bit is '1', and character & attribute register's 'BOX0' bit[D] if 'BOXE' bit is '0'.
Intensity	Character & attribute register's BLINK/FINT bit[9] Row attribute register's INTE bit[D] Row attribute register's RINT bit[5] If all 3 bits are set to '1', the raster intensity feature is enabled.

According to the 'BOXE' bit setting, raster color can be assigned in units of font or row. There is a trade-off in either case. If 'BOXE' Bit is set to '1', the box drawing feature can be carried out in units of font, but the raster color can only be assigned in units of row. On the other hand, if 'BOXE' bit is set to '0', the box drawing feature can't be carried out, but you can assign raster color in units of font.

Notes for When Making S1D2502B01 Fonts
Address 000h is appointed as blank data. RAM's initial values are all 0, and all bits are written as 0 when you erase the RAM, so blank data means the initial value. In other words, blank data means 'do nothing'. You don't need to write any data for the space font, except for 000h. It just needs to be an undotted area.

- **Other Color Effet**
  The row attribute register's 'BREN' bit's function is shown in the Figure below. If you set the 'BREN' bit of the row with the letter A as '0' after selecting A and B's raster color as black, the raster color black will be displayed. But if you set the 'BREN' bit of the row with the letter B as '1', the raster color black becomes invisible, so the back raster color (gray) is displayed as if it is the raster color.

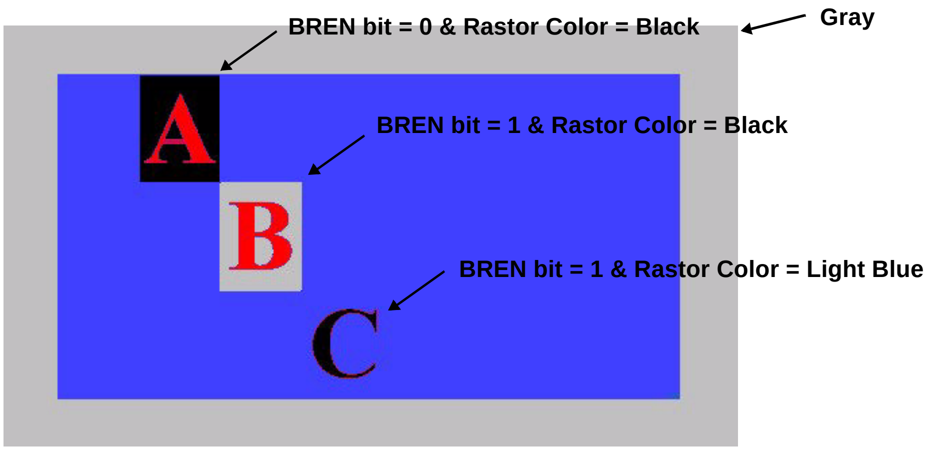


Figure 14. Color Effect by BREN Bit

Color blinking is using a selective control bit in blink mode to replace normal blinking with 8 different colors appearing in order on the font's character. Color blinking only replaces normal blinking, and blink time and blink duty are still applied at the same time. Therefore, if the blink duty is not set to off, only 3 ~ 4 colors may appear according to the blink duty, instead of all 8.

SIZING/POSITIONING

- **Character Size**
  Row attribute register's HZ bit[3:2] and VZ bit[1:0] control the character's vertical and horizontal size by factors of 1/2/3/4 in units of row. VZ is correctly expressed without regard to size since the next line is just pushed down in order, but HZ decides the column that the font occupies according to the size. For example, if HZ [1:0] = 0, 1, the font doubles in the horizontal direction, and one font takes up 2 columns. Therefore, the column address must move in the same amount as the HZ for the next font to be expressed correctly. in other words, if the horizontal size is doubled and takes up 2 columns, the next font must be put 2 columns back.

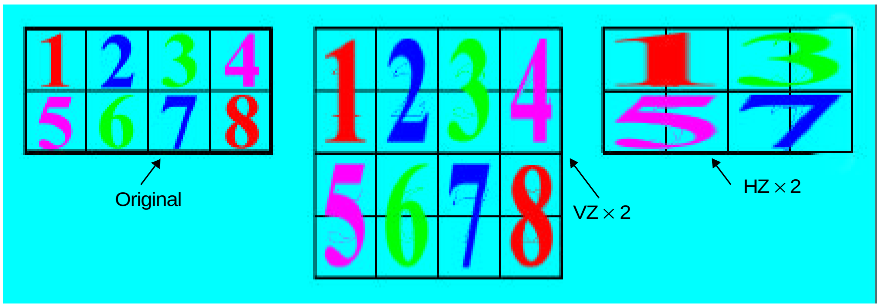


Figure 15. Character Size by VZ, HZ Bits

- **Character Height**
  Whereas the purpose of VZ[1:0] (Vertical Character Height) is to adjust the character's absolute size, the purpose of CH[5:0] (Character Height) is to output a uniformly sized OSD even if the resolution changes. To express a Character Height of CH = 18 ~ CH = 63 after receiving CH[5:0]'s input from the frame control register-1, decide on each line's repeating number (Standard Height CH = 18) and repeat the lines.

  The following Figure shows two examples of a height-controlled character. height control is carried out by repeating some of the lines.

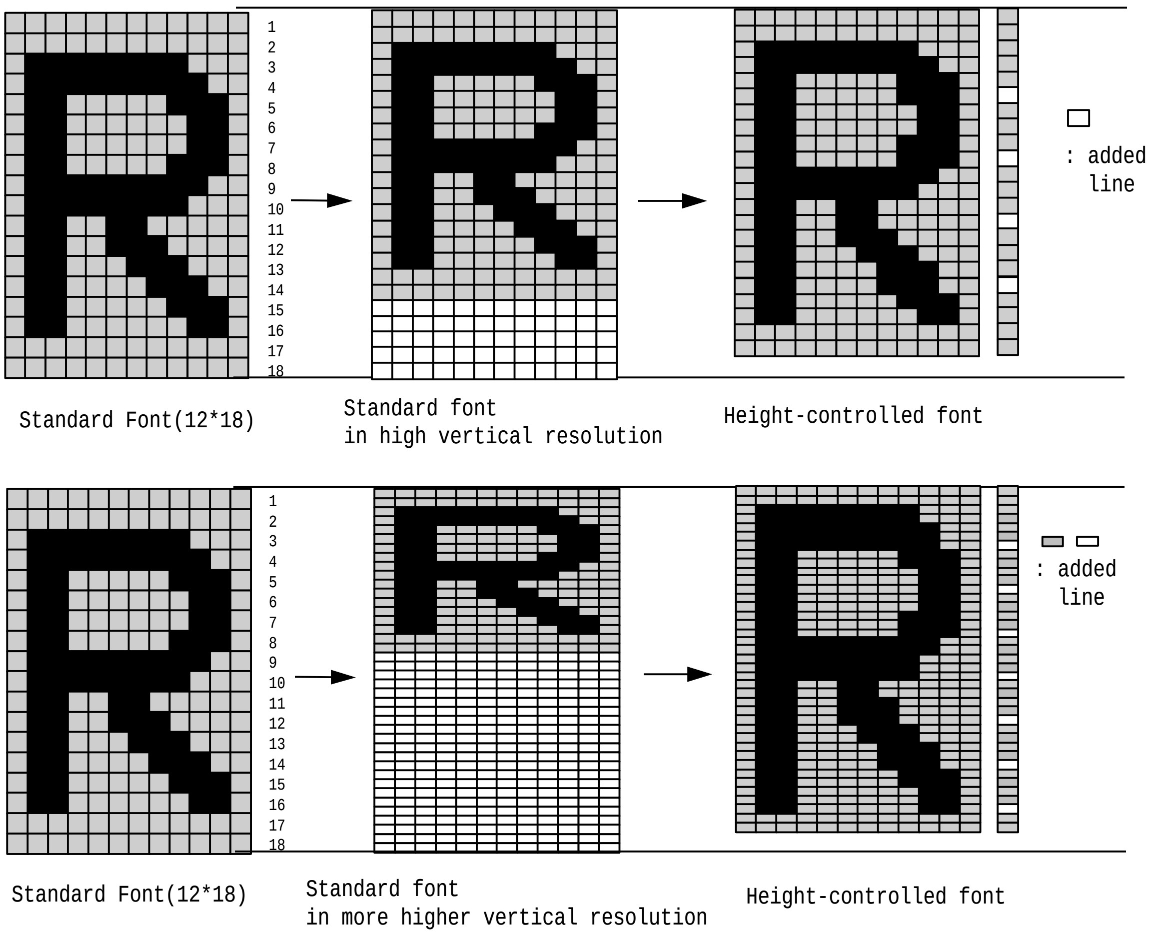


Figure 16. Character Height

Repeating line-number can be found by the following formula.

[# of the repeating lines = 2 + N × M],
where N = 1, 2, 3, ... and M = round{14 ¸ (CH[5:0]-18)}.

1. If CH[5:0] is greater than 32 and less than or equal to 46 (32 < CH[5:0] ≤ 46), all lines are repeated once or twice. The lines that are repeated twice are chosen by the following formula.

   [# of the repeating lines = 2 + N × M],

   where N = 1, 2, 3, ... and M = round {14 ≤ (CH[5:0]-32)}.

2. If CH[5:0] is greater than 46 and less than or equal to 60 (46 < CH[5:0] ≤ 60), all lines are repeated two or three times. The lines that are repeated three times are chosen by the following formula.

   [# of the repeating lines = 2 + N × M],

   where N = 1, 2, 3, ... and M = round {14 ≤ (CH[5:0]-46)}.

3. If CH[5:0] is greater than 60 and less than or equal to 64 (60 < CH[5:0] ≤ 64), all Lines are repeated three or four times. The lines that are repeated four times are chosen by the following formula.

   [# of the repeating lines = 2 + N x M],

   where N = 1, 2, 3, ... and M = round {14 ≤ (CH[5:0]-60)}.

CH's reference value is 18, and even if you input 0, it operates in the same way as when CH = 18. The repeating line-number is limited to 16. If the M value is less than or equal to 1, all lines of the standard font are repeated more than once.

Table 13. Repeating Line as Controlling by CH bits

Character Height	Repeating Line
CH = 18	-
CH = 19	9
CH = 20, 21	6, 13
CH = 22	5, 11, 17
CH = 23	4, 9, 14, 19
CH = 24	3, 7, 11, 15, 19, 21
CH = 25, 26, 27	3, 7, 11, 13, 15, 19, 22
CH = 28	3, 6, 9, 12, 14, 18, 20, 23, 25
CH = 29	3, 6, 9, 11, 13, 15, 18, 21, 23, 25, 26
CH = 30	3, 6, 8, 10, 12, 14, 16, 18, 20, 22, 25, 27
CH = 31	2, 5, 7, 9, 11, 13, 15, 17, 21, 23, 25, 27, 28
CH = 32, 33, 34, 35	2, 5, 7, 9, 11, 13, 15, 18, 21, 23, 25, 27, 28, 29
CH = 36	-
CH = 37	18

Table 13. Repeating Line as Controlling by CH bits

Character Height	Repeating Line (Continued)
CH = 38, 39	12, 25
CH = 40	10, 20, 30
CH = 41	8, 16, 24, 32
CH = 42	6, 12, 18, 24, 30, 36
CH = 43, 44, 45	6, 12, 18, 24, 30, 36, 41
CH = 46	4, 8, 12, 17, 21, 25, 29, 33, 37, 41
CH = 47	4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44
CH = 48	4, 8, 12, 16, 20, 23, 26, 29, 33, 37, 41, 45
CH = 49	4, 8, 12, 16, 19, 22, 25, 28, 31, 35, 39, 43, 47
CH = 50, 51, 52, 53	4, 8, 12, 15, 18, 21, 24, 27, 30, 33, 36, 40, 44, 48
CH = 54	-
CH = 55	27
CH = 56, 57	18, 36
CH = 58	14, 28, 42
CH = 59	12, 23, 34, 45
CH = 60	9, 18, 26, 34, 43, 52
CH = 61, 62, 63	8, 16, 23, 30, 37, 44, 51

- **Positioning**

  The frame control register-2's HP Bit [F:8] signifies delay of the horizontal display from the H-Sync reference edge to the character's 1st pixel location, and is controlled by multiplying HP [F:8]'s range value by 6. Also, VP bit[7:0] signifies the top margin height from the V-Sync reference edge, and is controlled by multiplying 4 to the VP [7:0]'s range value. Refer to the Figure shown below.

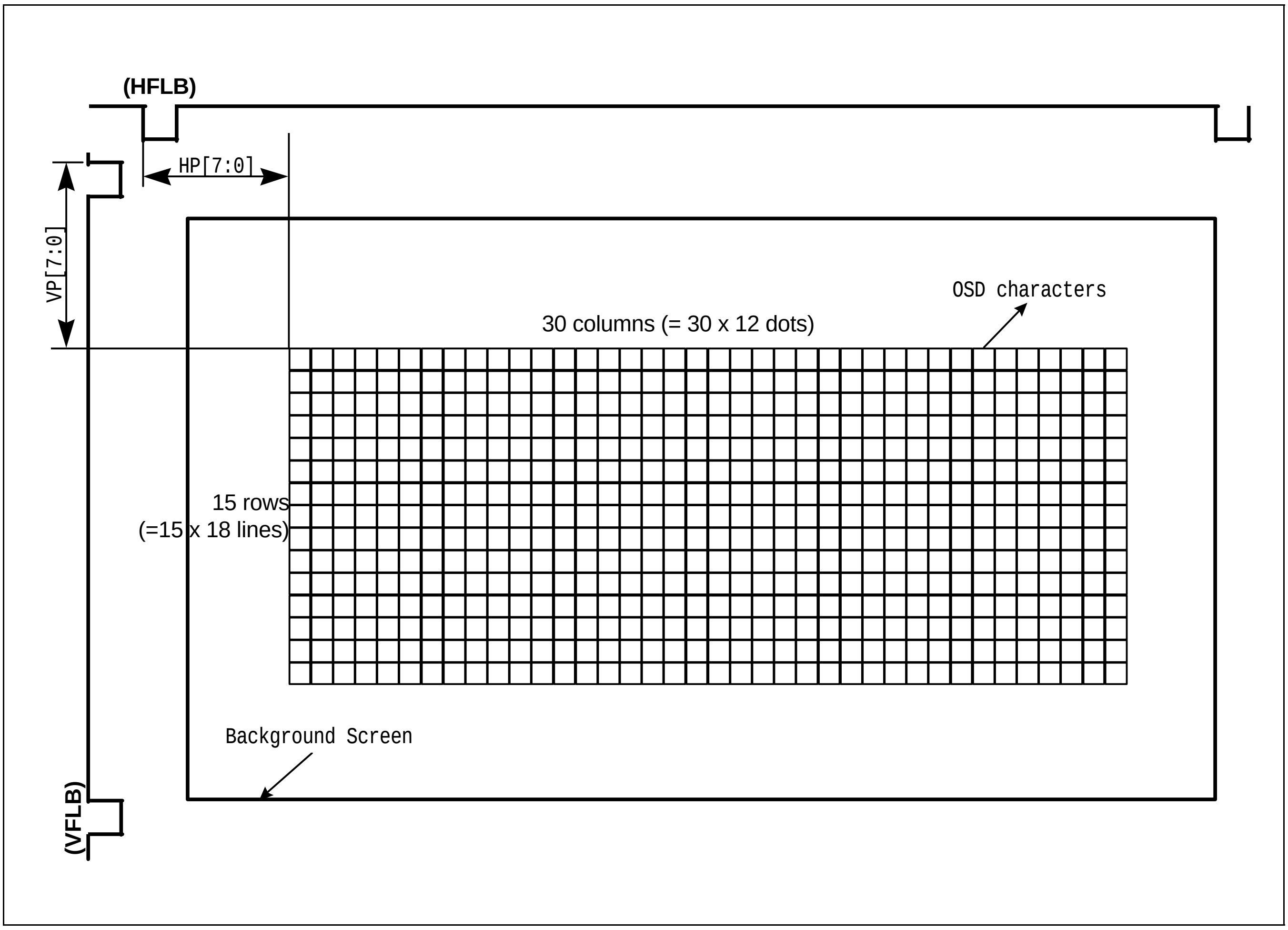


Figure 17. Frame Composition with the OSD Characters

VISUAL EFFECTS

- **Box Drawing**
  Set the row attribute register's boxe bit to '1' and enable the box feature. Then set the character & attribute register's BOX bit to select one of 4 modes. Or, use the character & attribute register's BINV bit to inverse the white and black areas of the box mode selected by the BOX bit.

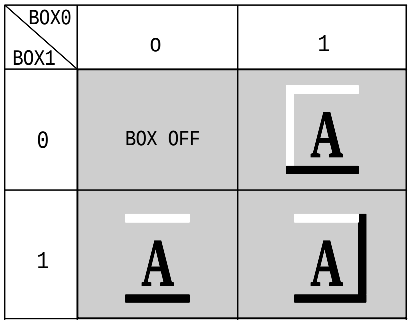
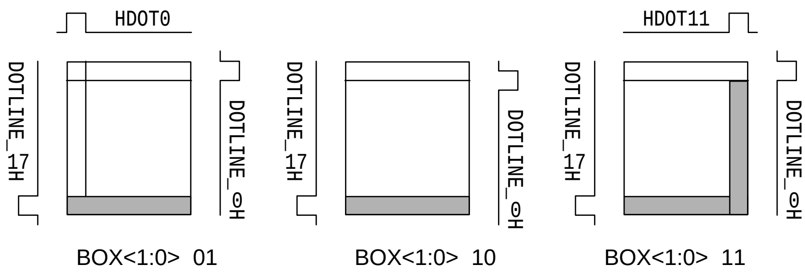


Figure 18. Box Drawing

The principle behind the boxing feature is shown below.



Out of the 12 horizontal dots and 18 vertical lines that make 1 character, make the first and 12th horizontal dots to HDOT0/HDOT11, and the first and 18th vertical lines to DOTLINE-0H/DOTLINE-17H in order to carry out box drawing for 1 dot outside the character.

- **Bordering/Shadowing**
  The character border and shadow can only be black. Character border is the effect where you make 1 pixel around the character, and character shadow is making 1 pixel to the right and below the character.

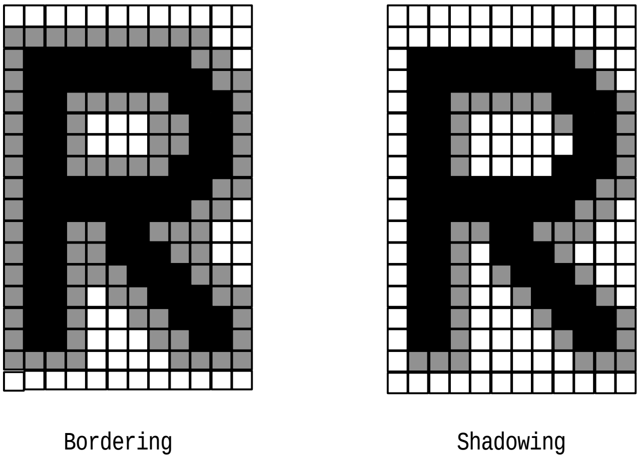


Figure 19. Character Bordering/Shdowing

- **Scrolling**
  Scrolling is slowly displaying or erasing a character from the top line to the bottom. This effect makes it look as if 1 character line is scrolling up or down.

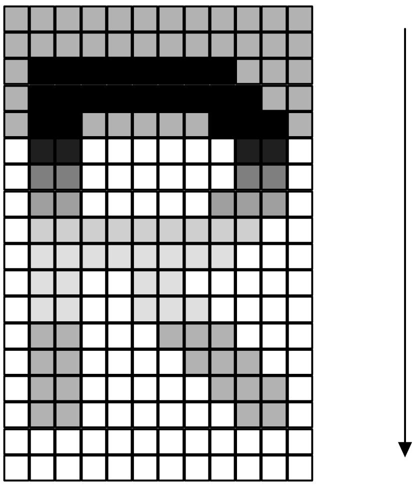


Figure 20. Scrolling

- **Fade-In/Fade-Out**
  Fade-in/fade-out is displaying from the center to the outside in units of font when OSD display is on/off. Each font's display is turned on/of without regard to size, in units of (12 × 18) dot.

  Also, to control the fade in/out time, the V_PULSE's 1/4, 1/8 clocks are used for counting. In other words, as control data, it takes 0.5sec if the frame control register - 0's 'FdeT' bit is 1, and 1sec if 0. If it is difficult to visualize the fade-in / fade-out feature with the explanation and diagrams in this document, write the control data to the OSD IC and verify the IC's operations. Like the scrolling feature, fade in/out can only be verified when OSD is enabled/disabled.

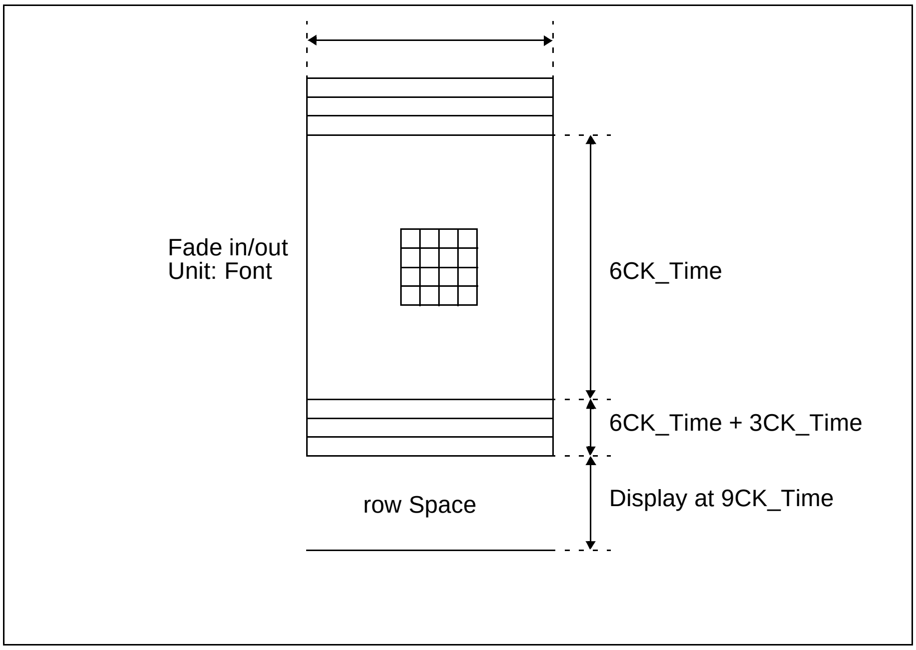


Figure 21. Fade-In/Fade-Out

PLL CONTROL

- **Introduction**

  PLL (Phase Lock Loop) is feedback controlled circuit that maintains a constant phase difference between a reference signal and an oscillator output signal.

  Generally, PLL is composed as follow Figure.

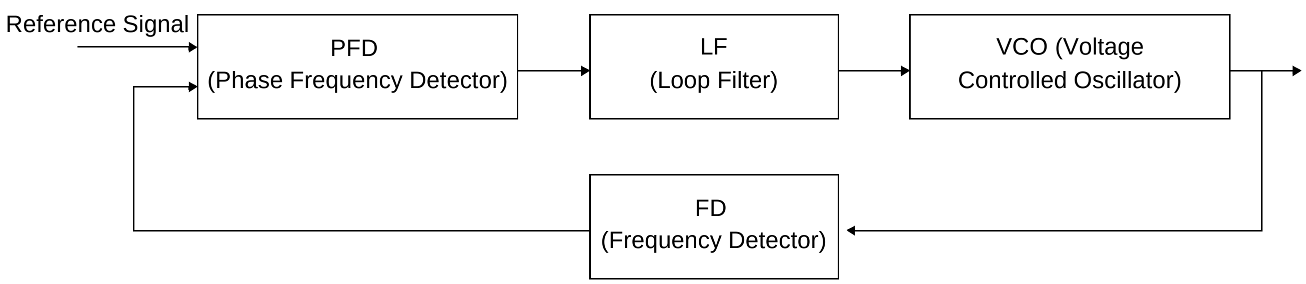


Figure 22. Block Diagram of General PLL

- PFD (Phase Frequency Detector)
  PFD compares the phase of the VCO output frequency, with the phase of a reference signal frequency output pulse is generated in proportion to that phase difference.

- LF (Loop Filter)
  LF smooths the output pulse of the phase detector and the resulting DC component is the VCO input.

- VCO (Voltage Controlled Oscillator)
  VCO is controlled by loop filter output. The output of the VCO is fed back to the phase frequency detector input for comparison which in turn controls the VCO oscillating frequency to minimize the phase difference.

- FD (Frequency Divider)
  FD divides too much different frequency that is oscillated from the VCO to compare it with reference signal frequency.

- **PLL of the S1D2502B01**
  PLL is composed of the phase detector, charge pump, VCO, and N-divider as 4 sub-blocks.

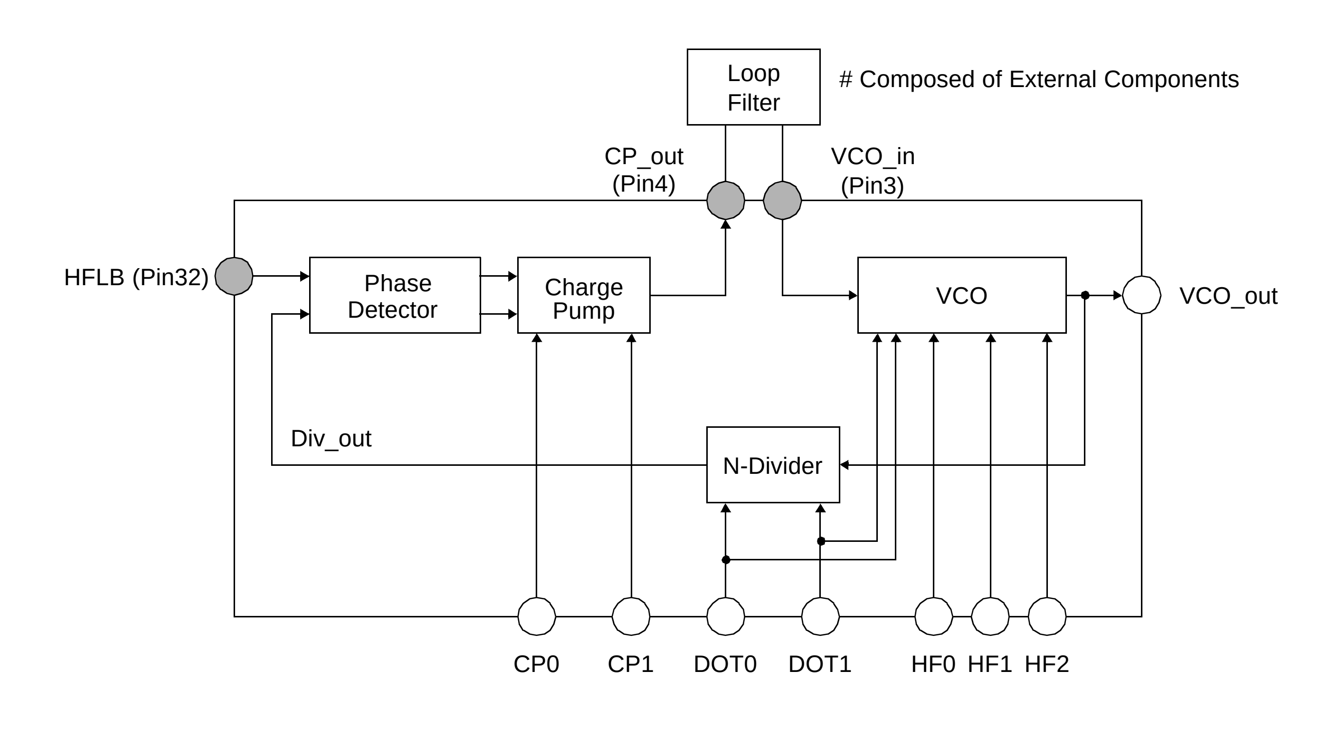
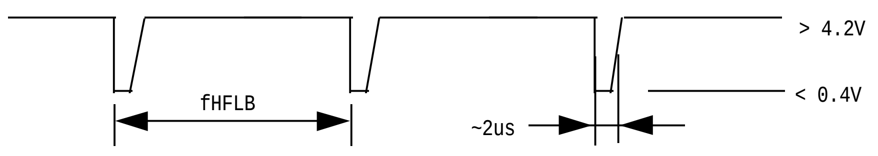


Figure 23. Block Diagram of the PLL Built in S1D2502B01

The following is the description of the input/output signals.

- **HFLB (Input)**
  Horizontal flyback signal is refrence signal of the PLL built in S1D2502B01.
  The HFLB signal's frequency range is 15 ~ 90kHz, so the PLL block must be a wide range PLL that can cover HFLB's entire frequency range.



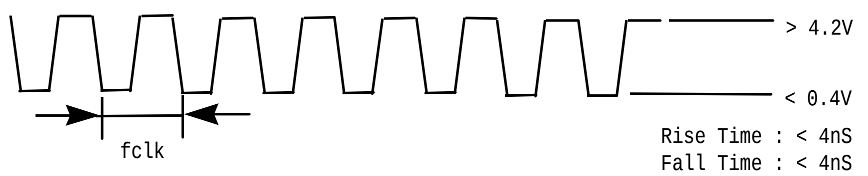
- VCO (Input)
  Error signal that passes through an external loop filter is input into VCO.
  Operation voltage range is 1-4V. You can raise immunity towards external noise by lowering VCO sensitivity. You can do this by making it have the maximum operation voltage range possible in the 5V power voltage.

- DOT0, 1 (Input)
  Mode control signal that controls the number of dots per line in the frame control register. There are 4 modes: 320, 480, 640, and 800 dots/line.
  According to your choice of mode, the OSD_PLL block's N-Divider is controlled by one of ÷320, ÷480, ÷640, or ÷800 Divider.

- HF0, 1, 2 (Input)
  The horizontal Sync frequency information is received from the micro controller through the frame control registers-1's bit C-A.

- CP0, 1 (Input)
  Charge Pump's output sourcing (or sinking) current control pin.
  This control data is received through frame control registers-1's bits E-D.

- VCO_OUT (Output)
  VCO output that becomes a system clock. It is the OSD R, G, B output signal's dot frequency, and the standard signal for OSD's various timings.
  Also, it is input into the N-Divider and makes a PLL loop



- CP_OUT (Output)
  Charge Pump circuit's output. input into external loop filter. It becomes one of 3 states according to the standard signal input into the phase detector (HFLB) and the divider output (Div_Out).

  - HFLB Div_Out is lead: Current sink
  - HFLB Lag: Current source
  - HFLB In-Phase: High impedence

TUNNING FACTORS OF THE S1D2502B01 PLL

- **PLL External Circuit**
  You may follow the recommendations for PCB art work and input/output signal characteristic improvement in recommendation.

  The external circuit that has the most influence on S1D2502B01 PLL block operation is pin 3 (VCO_IN) and pin 4 (CP_OUT)'s surrounding circuit. Refer to OSD PLL block.

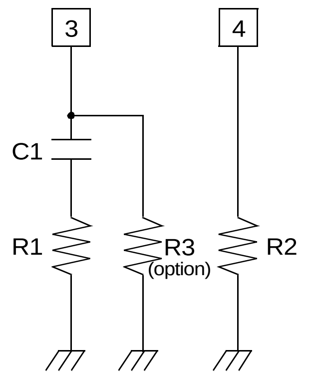


Figure 24. PLL External Circuit

Because the PLL circuit is basically a feedback circuit, there are many components that influence the characteristics. C1, R1, R2, and R3 do not have a localized effect.

As you can see, they are connected to the PLL control bits and influence the characteristics through their complicated relationships. The main functions of the time canstant and their reference values are as follows.

Table 14. Main Function of Time Constant in PLL External Circuit

Time Canstant	Recommended Value	Main Function
C1	562 (or 103, 223)	Influences the damping ratio and controls the PLL response time
R1	5.6KΩ(7.5KΩ)	Same as C1
R2	27KΩ (or 33KΩ)	Charge pump current adjustment
R3 (Option)	30MΩ (or 20MΩ)	Extend frequency range

- **PLL Control Bit**
  After configuring an external circuit using the recommended values, carry out programming using the recommended values for frequency range and control bits given in the Table below.

Table 15. Recommend Values of PLL Control Bit

Register Set	PLL Control Bit								
Freq. Range	**CP1**	**CP0**	**FPLL**	**HF2**	**HF1**	**HF0**	**DOT1**	**DOT0**	**Hex**
Below 40kHz	0	0	0	0	1	0	1	1	0B
40 - 50kHz	1	0	0	1	0	0	1	1	93
50 - 70kHz	1	0	0	1	0	1	1	1	97
Above 70kHz	1	0	0	1	1	1	1	1	9F

(Ref: 800 × 600, C1: 562, R1: 5.6K, R2: 27K, R3: 30M)

- **Locking Range**
  As you can see the figure below, it is 2.35V that measured voltage at pin-3 to optimize OSD quality. The proper voltage range is 1.5 ~ 3.25V.

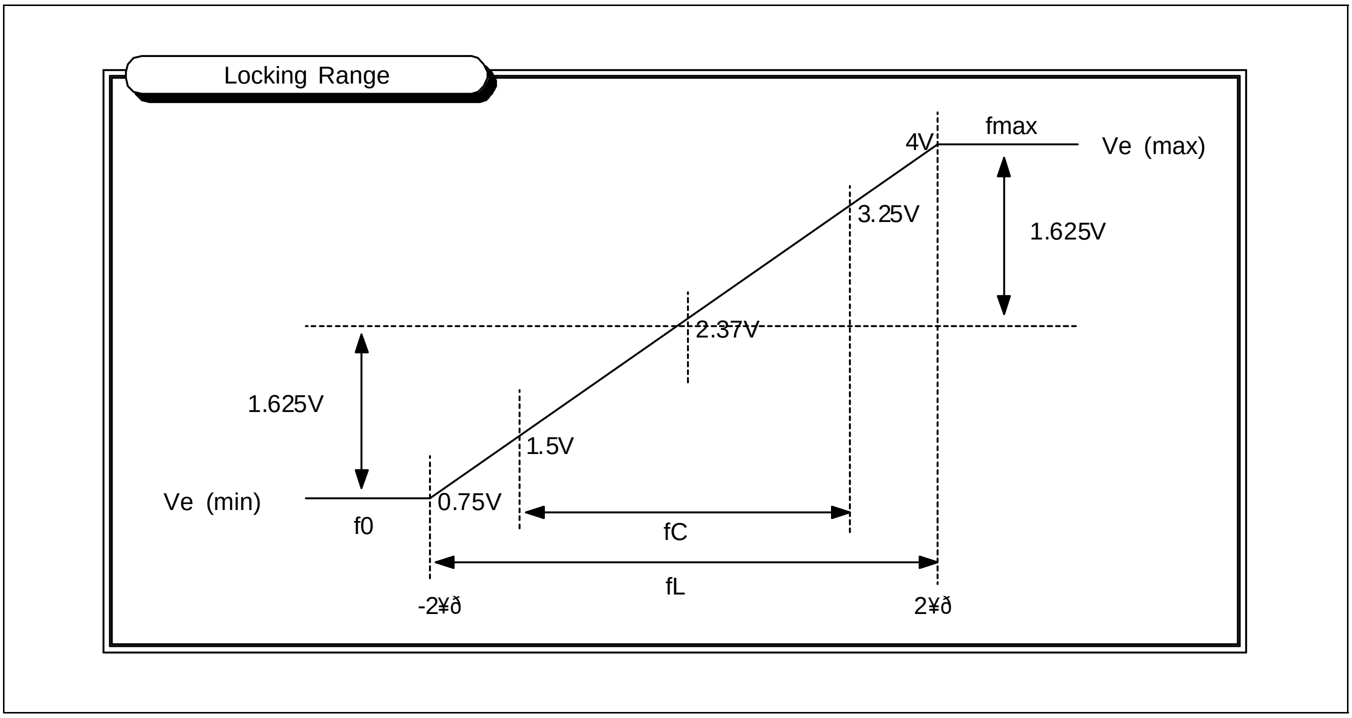


Figure 25. Locking Range

- **HF Bits Selection**
  HF bits is not selecting from out of 8 (2^3) steps uniformly, but selecting the step shown in figure below. In example, at 800 mode, there are 5 steps that the frequency range is controlled by HF bits.

Table 16. HF Bits Selection

DIV	DOT1	DOT0	HF2	HF1	HF0
320	0	0			
480	0	1			
640	1	0			
800	1	1			

After fixing time constants of the external circuit and PLL control bits except HF bits, if HF bits are stepped up, the voltage measured at pin-3 drops. On the contrary, if HF bits are stepped down, the voltage rises.

The voltage measured at pin-3 don't change by changing CP bits.

- **External Register at pin-4**

The external register at pin-4 is the factor that changes greatly at PLL tunning. The initial value of this external register value is decided as follows.

At first, the external register is replaced variable-register (about 50KΩ range).

and then, set the lowest PLL control bits at the lowest frequency allowed by set.
and then, change variable-register to be 2.35V that optimum voltage is locking.
and then, measure register value at this time.

also, set the highest PLL control bits at the highest frequency allowed by set.

and then, change variable-register to be 2.35V that optimum voltage is locking.
and then, measure register value at this time.

You may decide the average of these two registers' value to initial value.

The table below shows that other factors change as changing external register's value.

Fixing Factor	Variable Factor	Change	Voltage	Current	Lock Range
Time constants of the external circuit and PLL control bits except	Rext	↑	↑	↓	↓ (shift)
		↓	↓	↑	↑ (shift)

RECOMMENDATION

5V Power Routing

S1D2502B01's OSD part power is composed of analog VDD and digital VDD. To eliminate clock noise influence in the digital block, you need to separate the analog VDDA and digital VDD.

(BD102 use: Refer to Application Circuit)

12V Power Routing

Because S1D2502B01 is a wideband AMP of above 150MHz, 12V power significantly affects the video characteristics. The effects from the inductance and capacitance are different for each board, and , therefore, some tuning is required to obtain the optimum performance. The output power, VCC2, must be separated from VCC1 and VCC3 using a coil, which is parallel-connected to the damping resistor.The appropriate coil value is between 20uH - 200uH. Parallel-connected a variable resistor to the coil and control its resistance to obtain the optimum video waveform.

(Moreover, BD103 can tune using a coil and variable resistor to obtain the optimum video waveform.
L103, R124, BD103: Refer to application circuit)

VCC1, VCC3 12V Power

Use a 104 capacitor and large capacitor greater than 470uH for the power filter capacitor.

12V Output Stage Power VCC2

Do not use the power filter capacitor.

5V Digital Power VDD

Don't use a coil or magnetic core to the VDD input. Make the power filter capacitor, an electric capacitor of greater than 50uF, single and connect it to VSS, the digital GND.

Output Stage GND2

Care must be taken during routing because it ,as an AMP output stage GND, is an important factor of video oscillation. R/G/B clamp cap and R/G/B load resistor must be placed as close as possible to the GND2 pin. GND2 must be arranged so that it has the minimum GND loop, which at one point must be connected to the main GND.

Digital GND VSS

When this is to be connected directly to the GND2, it can cause the OSD clock noise, so the loop connection should be routed as far away as possible. If the OSD clock noise affects the screen, separate VSS GND from all GND and connect it to the main board using a bead. Again, the bead connection point should be placed as far away as possible to the GND2.

Analog Block

The PLL built in to S1D2502B01 is sensitive to noise due to the wide range PLL characteristics. Therefore, you need to isolate the analog block in the following manner. First make a separate land for the analog block (pin2 - pin6)'s ground, and connect it to the main ground through a 1MΩ resistor. The analog GND of both sides of a double faced PCB must be separated from the main ground. (Separate pin 2's 5V analog GND, which is the GND for OSD PLL, from the main and digital GNDs and connect it to the main GND using about 1MΩ resistor. GND for pins 2 - 6 is the No. 2 VSSA GND.)

I^2C Control Line (SCL, SDA Line)

I^2C communication noise (noise generated in the OSD display pattern when data is transmitted in the I^2C line) may be generated because of an I^2C control line that passes near the analog block. The I^2C control lines near S1D2502B01 must be separated from the analog block as much as possible.

Furthermore, the I^2C bus interference can be prevented by inserting a series resistor in the line.

Horizontal Flyback Signal

Display jittering can be generated if the horizontal signal (HFLB) input to S1D2502B01 is not a clean signal.

We recommend a short path and shielded cable for obtaining a clean signal.

Generally, the input horizontal signal (HFLB) is generated by using a high voltage horizontal flyback signal. The effect from the high voltage flyback signal can be reduced by separating the R115 and R117 GND, which determines the flyback signal slice level, from the transistor GND, which generates the actual S1D2502B01 input horizontal signal. Furthermore, the flyback signal sharpness must be maintained by minimizing the values of R115, R116 and R117 resistors, which set the horizontal signal slice level. values.

(R115, R116, R117: Refer to application circuit)

HFLB Input Signal Generator

You can correct the circuit by reducing the resistors that sets the slice level of the horizontal signal in the HFLB-generating circuit.

APPLICATION BOARD CIRCUIT

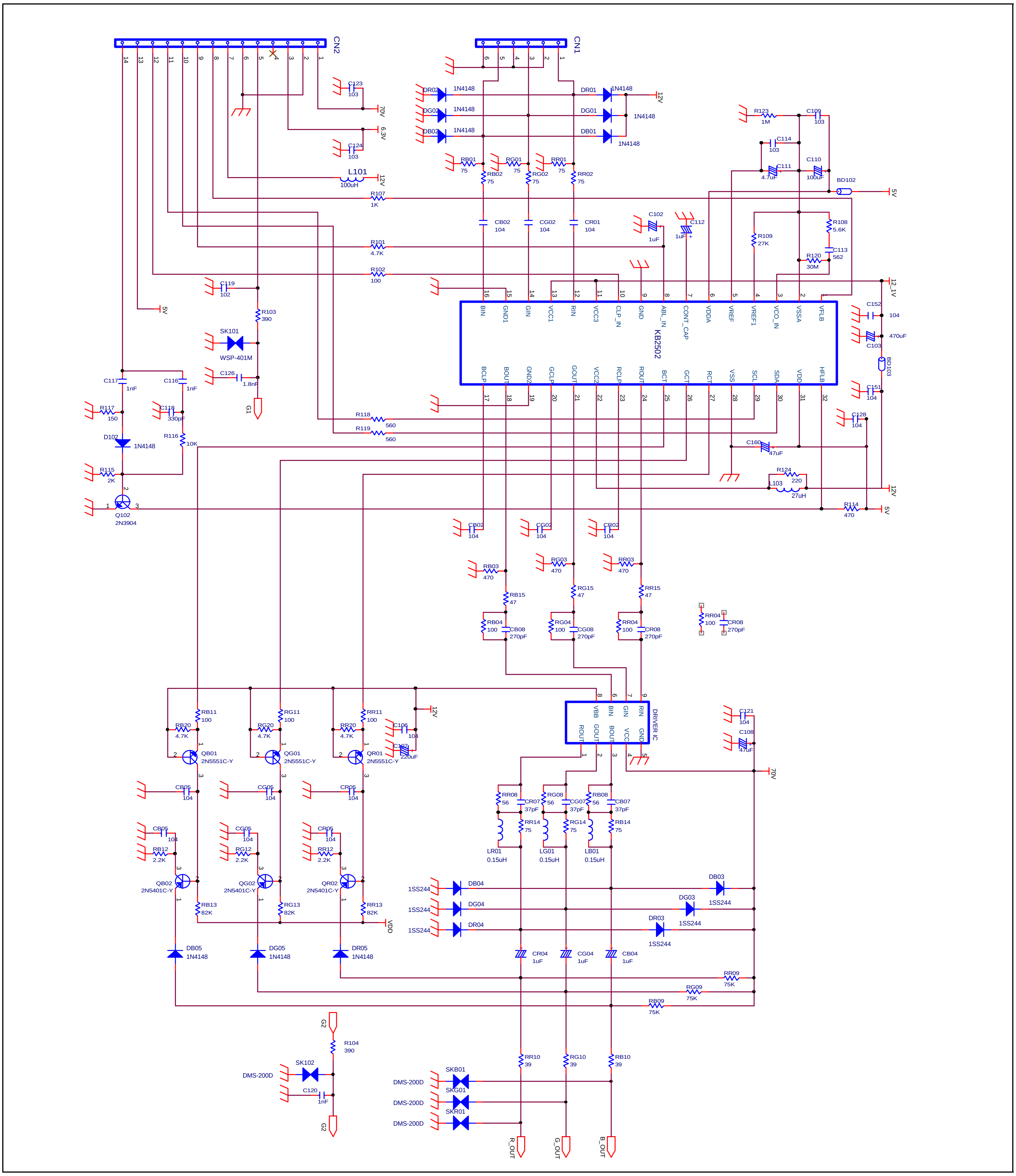


Figure 26. Application Board Circuit

TYPICAL APPLICATION CIRCUIT

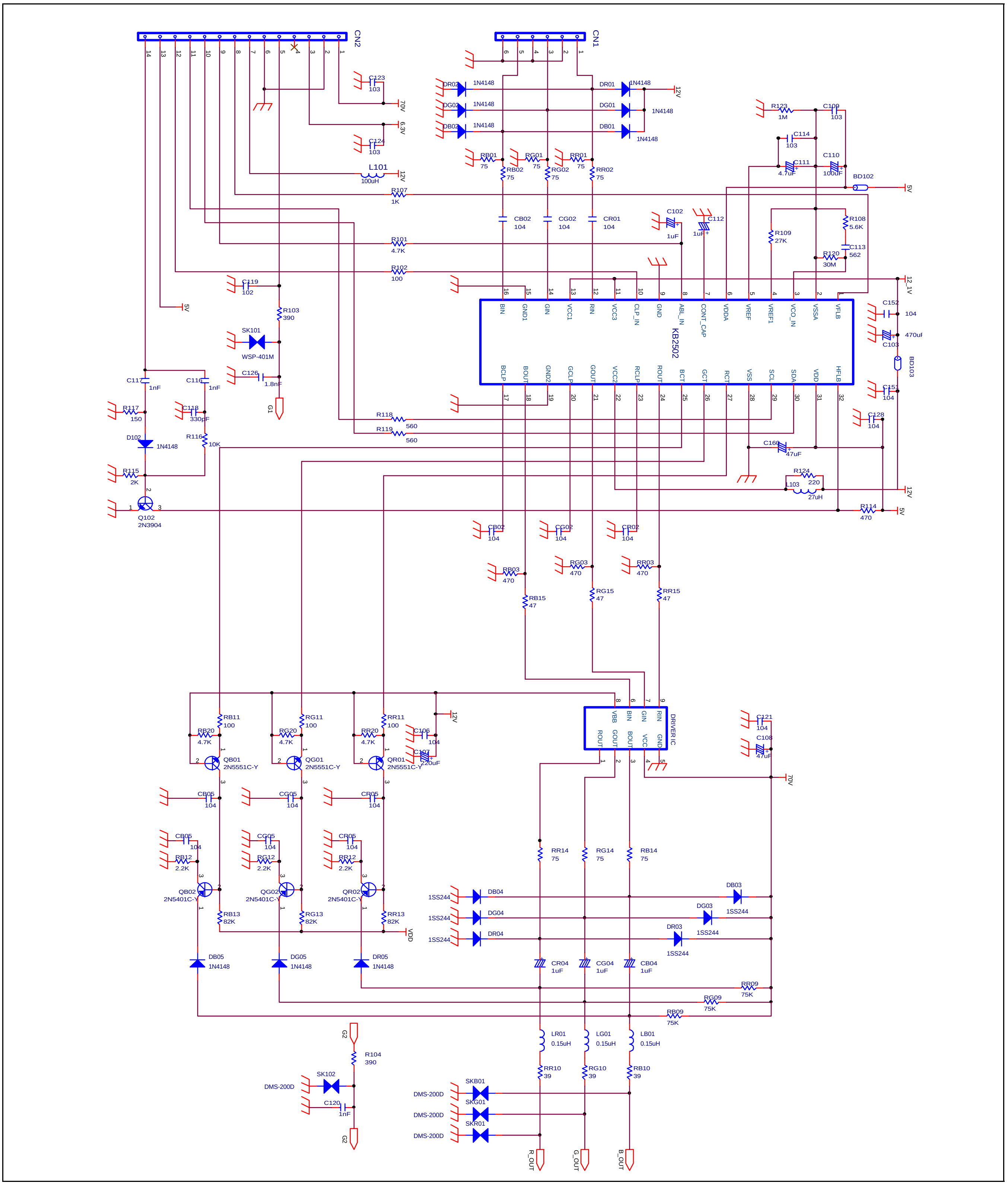


Figure 27. Typical Application Circuit

SAMSUNG ELECTRONICS

ROM FONTS

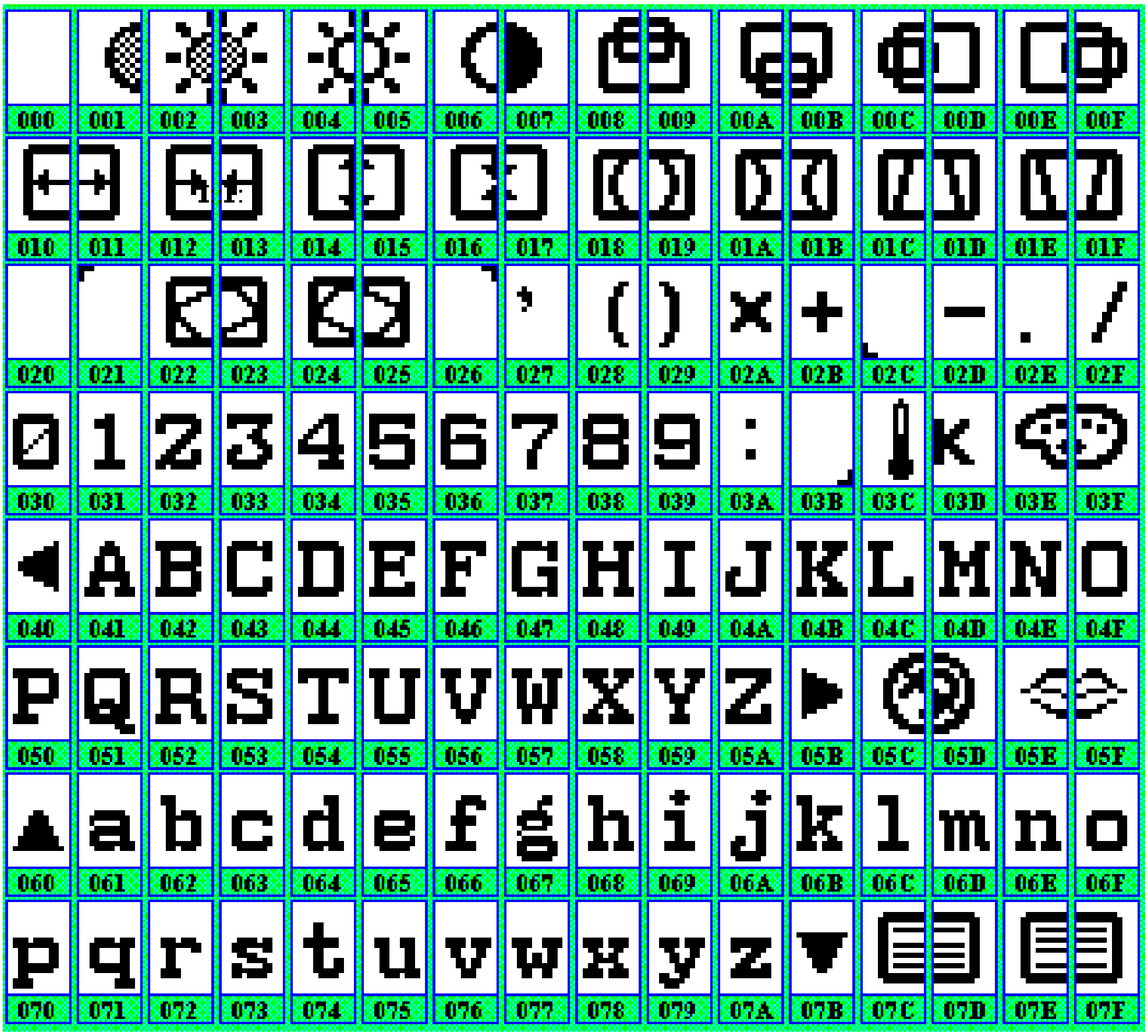
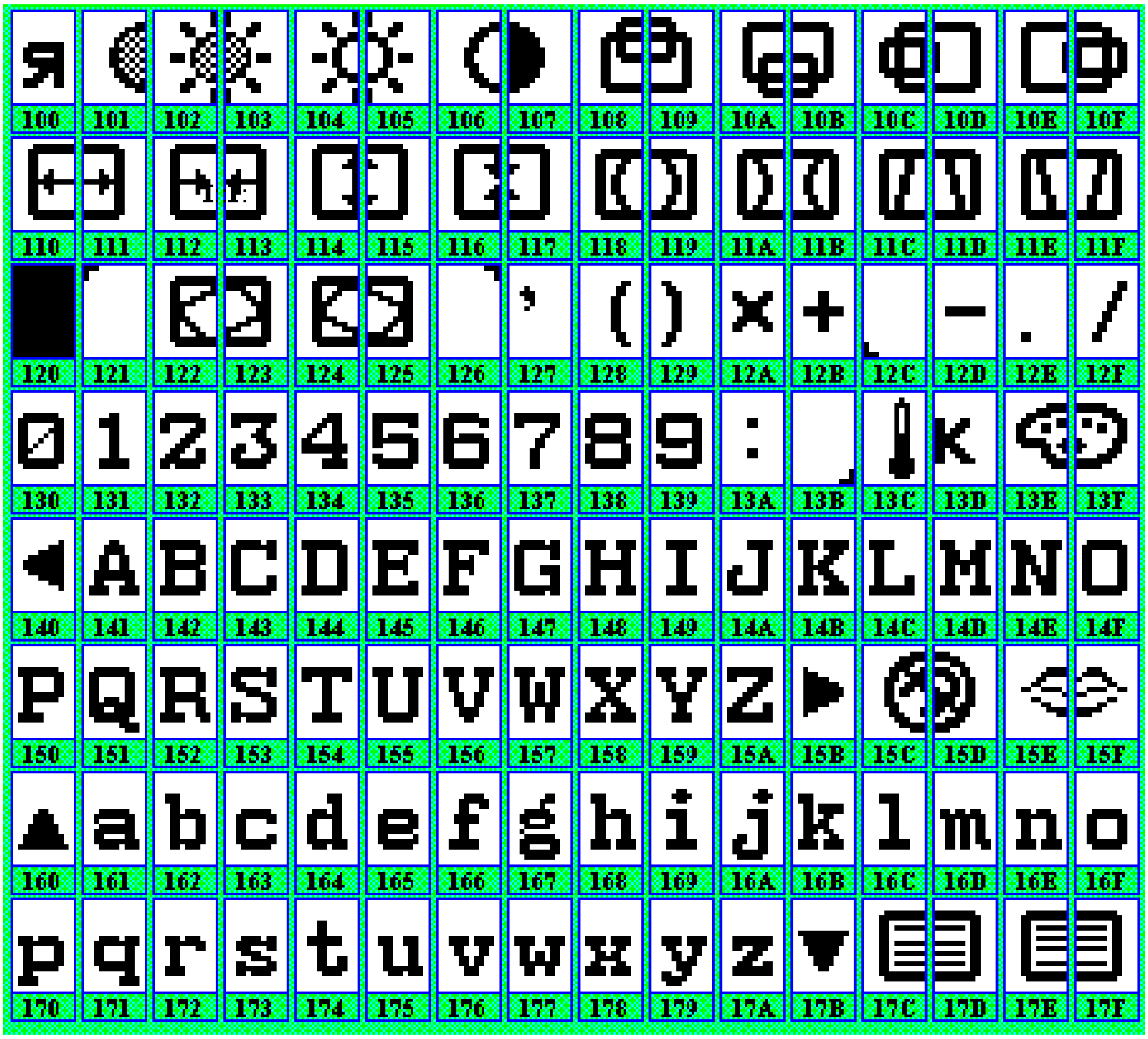
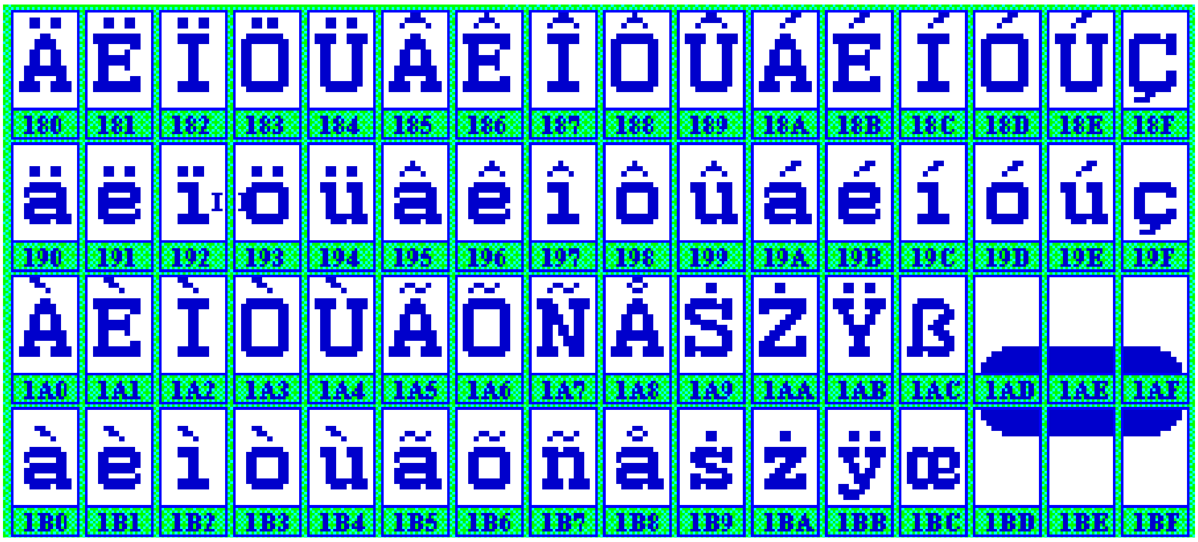


Figure 28. ROM Fonts


080 081 082 083 084 085 086 087 088 089 08A 08B 08C 08D 08E 08F
090 091 092 093 094 095 096 097 098 099 09A 09B 09C 09D 09E 09F
0A0 0A1 0A2 0A3 0A4 0A5 0A6 0A7 0A8 0A9 0AA 0AB 0AC 0AD 0AE 0AF
0B0 0B1 0B2 0B3 0B4 0B5 0B6 0B7 0B8 0B9 0BA 0BB 0BC 0BD 0BE 0BF
0C0 0C1 0C2 0C3 0C4 0C5 0C6 0C7 0C8 0C9 0CA 0CB 0CC 0CD 0CE 0CF
0D0 0D1 0D2 0D3 0D4 0D5 0D6 0D7 0D8 0D9 0DA 0DB 0DC 0DD 0DE 0DF
0E0 0E1 0E2 0E3 0E4 0E5 0E6 0E7 0E8 0E9 0EA 0EB 0EC 0ED 0EE 0EF
0F0 0F1 0F2 0F3 0F4 0F5 0F6 0F7 0F8 0F9 0FA 0FB 0FC 0FD 0FE 0FF


100 101 102 103 104 105 106 107 108 109 10A 10B 10C 10D 10E 10F
110 111 112 113 114 115 116 117 118 119 11A 11B 11C 11D 11E 11F
120 121 122 123 124 125 126 127 128 129 12A 12B 12C 12D 12E 12F
130 131 132 133 134 135 136 137 138 139 13A 13B 13C 13D 13E 13F
140 141 142 143 144 145 146 147 148 149 14A 14B 14C 14D 14E 14F
150 151 152 153 154 155 156 157 158 159 15A 15B 15C 15D 15E 15F
160 161 162 163 164 165 166 167 168 169 16A 16B 16C 16D 16E 16F
170 171 172 173 174 175 176 177 178 179 17A 17B 17C 17D 17E 17F


180 181 182 183 184 185 186 187 188 189 18A 18B 18C 18D 18E 18F
190 191 192 193 194 195 196 197 198 199 19A 19B 19C 19D 19E 19F
1A0 1A1 1A2 1A3 1A4 1A5 1A6 1A7 1A8 1A9 1AA 1AB 1AC 1AD 1AE 1AF
1B0 1B1 1B2 1B3 1B4 1B5 1B6 1B7 1B8 1B9 1BA 1BB 1BC 1BD 1BE 1BF