S71WS512N to S71WS512P

Migrating from the S71WS512N to the S71WS512P

Application Note

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1. Introduction

Migrating from the S71WS512N to the monolithic S71WS512P is a simple process; however, the user should be aware of a few differences between these two parts. These differences are the result of the S71WS512N using two S29WS256N die in series while the S71WS512P uses a single S29WS512P configuration. This application note describes these differences in detail so users currently using the S71WS512N configuration can plan ahead and include the necessary software to ensure a smooth migration to the S71WS512P. Both software and hardware considerations are covered. Table 1.1 shows a comparison of the key features between the two flash device cores.

Table 1.1 Comparison of Key Features

Futures	S29WS256N	S29WS512P
Technology	MirrorBit™	MirrorBit™
Process Rule	110 nm	90 nm
V_{CC}	1.70 V to 1.95 V	1.70 V to 1.95 V
V_{IO} (V_{CCQ})	$=V_{CC}$	$=V_{CC}$
Max Density	256 Mb	**512 Mb**
Configuration Register	CR0-CR15	CR0.0 - CR0.15, CR1.0 - CR1.15
Sector Architecture	16 K-words Small Sector 64 K-words Large Sector	16 K-words Small Sector 64 K-words Large Sector
Bank Architecture	16 Bank Structure	16 Bank Structure
Bank Size	2 Mb	**4 Mb**
Boot Option	Top / Bottom / Dual	Top / Bottom / Dual
Common Flash Interface (CFI)	Yes	Yes
Simultaneous Read/Write	Yes	Yes
Asynchronous Read Mode	Yes	Yes
Page Mode Read	Yes	Yes
Page Size	4-words	**8-words**
Synchronous (Burst) Read Mode	Yes	Yes
Burst Frequency	54 MHz / 66 MHz / 80 MHz	54 MHz / 66 MHz / 80 MHz / **108 MHz**
Burst Length	8 / 16 / 32 Continuous	8 / 16 / 32 Continuous
Single Word / Write Buffer Program	Yes	Yes
Write Buffer Size	32-words	32-words
Program Suspend / Program Resume	Yes	Yes
Sector Erase / Chip Erase	Yes	Yes
Erase Suspend / Erase Resume	Yes	Yes
Unlock Bypass / Fast Mode	Yes	Yes
Accelerated Program / Chip Erase	Yes	Yes
Sector Protection	Hardware: WP# Software: ASP	Hardware: WP# Software: ASP
Secured Silicon Area	128-words factory locked 128-words customer lockable	128-words factory locked 128-words customer lockable

2. Performance Characteristics

The 90 nm MirrorBit™ technology, on which the S29WS512P is based, allows performance improvements over the S29WS256N, which is based on 110 nm MirrorBit technology. Table 2.1 shows the performance comparison between the two devices.

Table 2.1 Performance Comparison

Access Time		S29WS256N	S29WS512P
Read Access Time VCC=1.70 V to 1.95 V CL=30pF	Max. Async. Access (t_{ACC})	80 ns	80 ns
	Max. Async. Page Access (t_{PACC})	20 ns	20 ns
	Max. Sync. Burst Access (t_{BACC})	9 ns	**7 ns**
Single Word Programming Time	Typ	40 µs	**30 µs**
	Max (See Note)	400 µs	**150 µs**
Total 32-Words Buffer Programming Time	Typ	300 µs	**192 µs**
	Max (See Note)	3000 µs	**960 µs**
Effective Word Programming Time	Typ	9.4 µs	**6 µs**
	Max (See Note)	94 µs	**30 µs**
Sector Erase Time	Typ	150 ms: 16 K-words 600 ms: 64 K-words	150 ms: 16 K-words 600 ms: 64 K-words
	Max (See Note)	2000 ms: 16 K-words 3500 ms: 64 K-words	**1750 ms: 16 K-words** **3000 ms: 64 K-words**

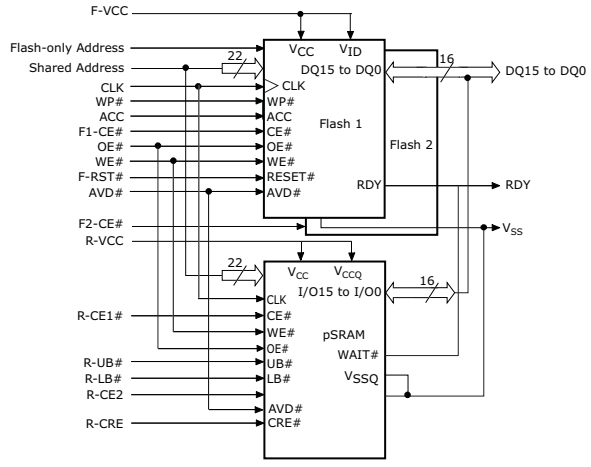
Note:
Under worst case conditions of 90°C. V_{CC} = 1.70 V. 100,000 cycles.

3. Electrical Specification Changes

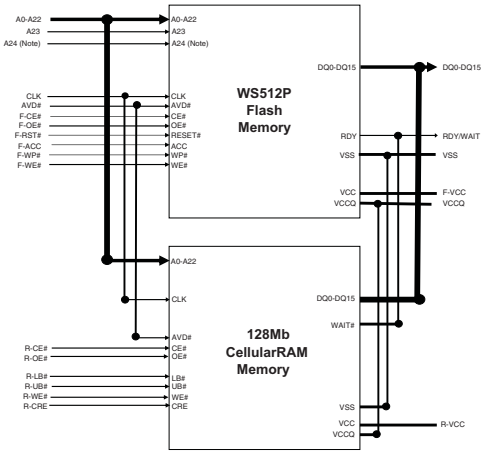
I/O Descriptions - Package and Pin Layout

There are also a few hardware changes required for the migration. Since the entire S29WS512P is addressed with a single chip select, address line A24 has to be connected. Note that some systems may require a pull down resistor on A24. The two block diagrams in Figure 3.1 illustrate these changes.

Figure 3.1 Block Diagrams



S71WS-N



S71WS-P

Note:
Pull down resistor may be required for some systems.

V_{CC} and V_{CCQ} Ramp

On the WS512P, V_{CC} and V_{CCQ} (V_{IO}) must ramp up simultaneously. This restriction is not required on the S71WS512N. Regarding V_{CC} ramp rates, the WS512P places no restriction on V_{CC}; (Some earlier revisions of the WS256N required the ramp rate to be greater than 1 V/100 µs, or a RESET pulse would have to be issued.

Table 3.1 shows parameters that have been changed in the S29WS512P.

Table 3.1 V_{CC} / RESET# / CE# Timing Parameter Comparison

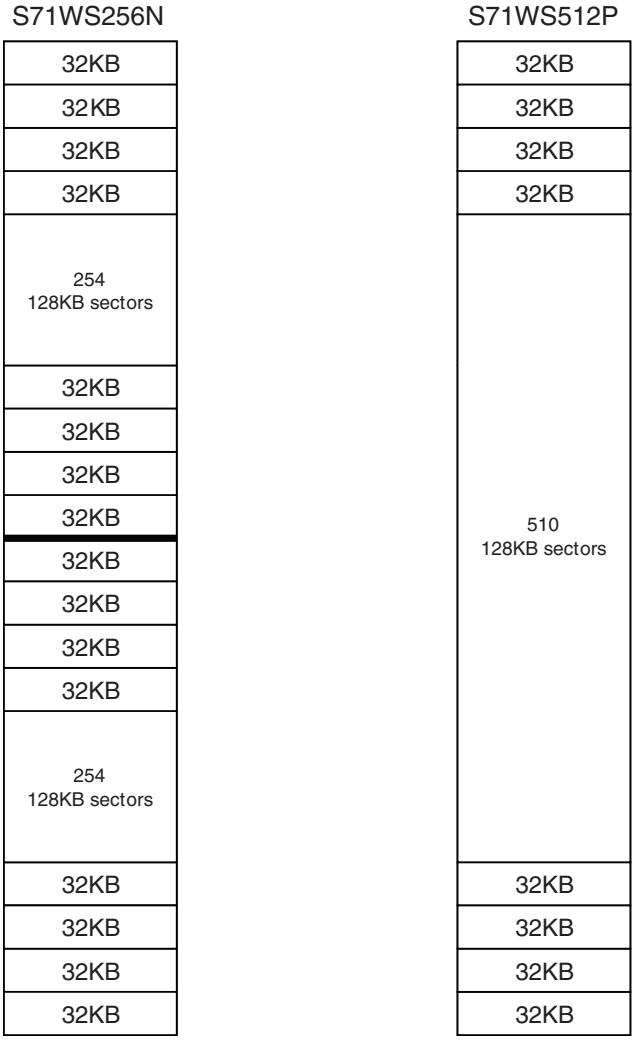
Parameter	Description	S29WS256N	S29WS512P
t_{VCS}	V_{CC} Setup Time	1 ms	30 µs
t_{RPH}	RESET# Low to CE# Low	N/A	10 µs

4. Basic Architectural Changes

4.1 Sector Architecture

Both the S29WS256N and the S29WS512P feature sectors of the same size, that is, 128 KB sectors and the smaller 32 KB (boot) sectors. However, the S71WS512N contains a total of 16 small flash sectors, while the S71WS512P contains only 8 small flash sectors. Figure 4.1 illustrates this.

Figure 4.1 Flash Sector Architecture of the S71WS256N and S71WS512P



When designing software compatible with both devices, users must account for the 8 additional boot sectors in the S71WS256N, situated logically in the middle of the sector map.

4.2 Bank Architecture

The flash core of the S71WS512N consists of a total of 32 banks, each of which is 2 MB. The flash core of the S71WS512P contains a total of 16 banks, each of which is 4 MB. This variation may be important to consider in cases where the simultaneous read/write feature of the devices is being used to ensure that the proper bank boundaries are accounted for in both cases.

4.3 Chip select

Since the S71WS512N employs two chip selects (one chip select addresses one 32 MB region), it is possible to configure the address range to be non-contiguous for the two 32 MB regions. However, the S71WS512P is a monolithic device that can be addressed with only one chip select and has a contiguous address range. If the S71WS512N is configured with an address gap after the first 32 MB, users must ensure that the software can also handle a contiguous address range in the S71WS512P.

4.4 Burst Configuration Register

The S71WS512N has two configuration registers (see Table 4.1) of the same type (one in each die) that need to be configured individually for proper operation of the device. The S71WS512P has two different types of configuration registers. The S71WS512P has an additional configuration register (see Table 4.2) in which two bit fields are used. CR1.0 is used to provide additional programmable wait states. In addition, CR 0.6, can be used to select zero hold mode. Finally, the configuration registers must be programmed in order (CR0 first and then CR1) or programming will be ignored.

Table 4.1 S29WS256N Configuration Register

CR Bit	Function							Settings			
CR 15	Set Device Read Mode							0: Burst Read Mode 1: Asynchronous Read Mode			
CR 14	Reserved							0: All Others 1: S29WS256N at 6 or 7 Wait Settings			
		2nd	3rd	4th	5th	6th	7th	Initial data is valid on the 2nd (3rd, 4th...9th) rising CLK edge after addresses are latched.			
CR 13	Programmable Wait State	0	0	0	0	1	1				
CR 12		0	0	1	1	0	0				
CR 11		0	1	0	1	0	1				
CR 10	RDY Polarity							0: RDY signal active LOW 1: RDY signal active HIGH (Default)			
CR 9	Reserved							1: Default			
CR 8	RDY							0: RDY active 1-clock cycle before data 1: RDY active with data			
CR 7	Reserved							1: Default			
CR 6	Reserved							1: Default			
CR 5	Reserved							0: Default			
CR 4	Reserved							0: Default			
CR 3	Burst Wrap Around							0: No Wrap Around Burst 1: Wrap Around Burst (Default)			
								Continuous (Default)	8-Word Linear Burst	16-Word Linear Burst	32-Word Linear Burst
CR 2	Burst Length							0	0	0	1
CR 1								0	1	1	0
CR 0								0	0	1	0

Table 4.2 S29WS512P Configuration Register

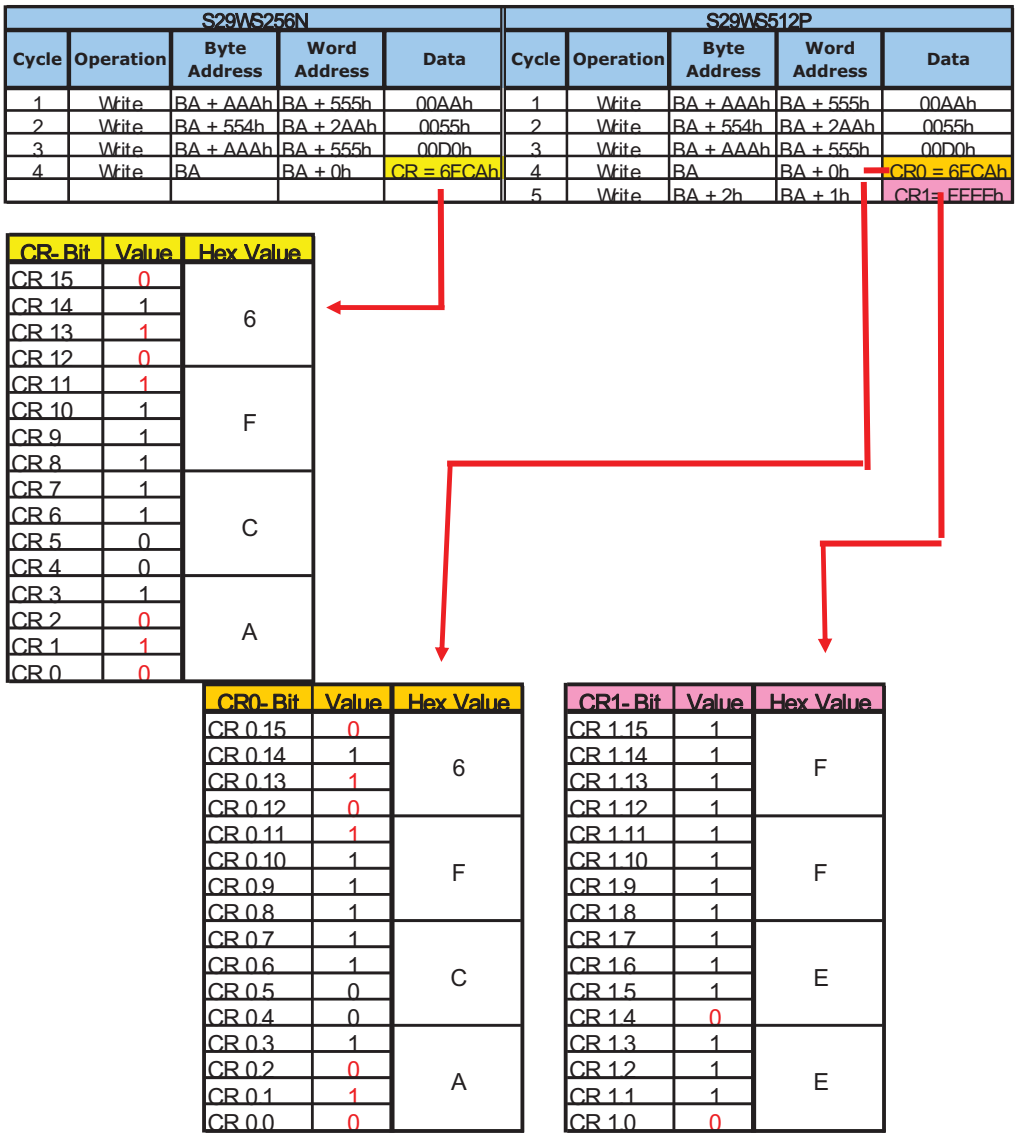
CR Bit	Function									Settings			
CR 0.15	Set Device Read Mode									0: Burst Read Mode 1: Asynchronous Read Mode			
CR 0.14	Reserved									0: Reserved 1: Reserved (Default)			
		2nd	3rd	4th	5th	6th	7th	8th	9th	Initial data is valid on the 2nd (3rd, 4th...9th) rising CLK edge after addresses are latched.			
CR 1.0	Programmable Wait State	0	0	0	0	0	0	1	1				
CR 0.13		0	0	0	0	1	1	0	0				
CR 0.12		0	0	1	1	0	0	0	0				
CR 0.11		0	1	0	1	0	1	0	1				
CR 0.10	RDY Polarity									0: RDY signal active LOW 1: RDY signal active HIGH (Default)			
CR 0.9	Reserved									1: Default			
CR 0.8	RDY									0: RDY active 1-clock cycle before data 1: RDY active with data			
CR 0.7	Reserved									1: Default			
CR 0.6	Mode of Operation									0: Zero Hold Mode 1: Legacy Mode (Default)			
CR 0.5	Data Rate									0: Default			
CR 0.4	RDY Function									0: Default			
CR 0.3	Burst Wrap Around									0: No Wrap Around Burst 1: Wrap Around Burst (Default)			
										Continuous (Default)	8-Word Linear Burst	16-Word Linear Burst	32-Word Linear Burst
CR 0.2	Burst Length									0	0	0	1
CR 0.1										0	1	1	0
CR 0.0										0	0	1	0
CR 1.15	Reserved									1: Default			
CR 1.14	Reserved									1: Default			
CR 1.13	Reserved									1: Default			
CR 1.12	Reserved									1: Default			
CR 1.11	Reserved									1: Default			
CR 1.10	Reserved									1: Default			
CR 1.9	Reserved									1: Default			
CR 1.8	Reserved									1: Default			
CR 1.7	Reserved									1: Default			
CR 1.6	Reserved									1: Default			
CR 1.5	Reserved									1: Default			
CR 1.3	Reserved									1: Default			
CR 1.2	Reserved									1: Default			
CR 1.1	Reserved									1: Default			

Table 4.3 Configuration Register Access Command Comparison

	Command	Cycles	Bus Cycles											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
S29WS256N	Set Configuration Register	4	555	AA	2AA	55	555	D0	X00	CR				
	Read Configuration Register	4	555	AA	2AA	55	555	C6	X00	CR				
S29WS512P	Set Configuration Register	5	555	AA	2AA	55	555	D0	X00	CR0	X01	CR1		
	Read Configuration Register	4	555	AA	2AA	55	555	C6	X0 or X1	CR0 or CR1				

Figure 4.2 shows an example of how to set the configuration register for 80 MHz 8-Burst with Wrap Read (7-Wait), RDY Active-*H* 1 cycle prior.

Figure 4.2 Example Configuration Register Settings



4.5 Page Mode Read

Both devices are capable of page mode reads, which provides random read access speed for locations within a page. Table 4.4 shows the page size comparison differences between the S71WS512N and the S71WS512P.

Table 4.4 Page Size Comparison

Description	S71WS256N	S71WS512P
Page Size	4-word	8-word (See Note)

Note:
Supports 8-word cache fill.

4.6 Autoselect Device ID

For ease of identification, the two devices have separate device ID codes (see Table 4.5). The Device ID can be retrieved using the Autoselect command sequence.

Table 4.5 Device ID Comparison

Description	Autoselect Address	Read Data (S71WS512N)	Read Data (S71WS512P)
Device ID, Word 1	(BA) + 01h	227Eh	227Eh
Device ID, Word 2	(BA) + 0Eh	2230h	223Dh - Single CE
Device ID, Word 3	(BA) + 0Fh	2200h	2200h

4.7 Write Buffer Programming

The S71WS512P limits the user to loading addresses starting from the minimum address in a sequential order when using write buffer programming, while the S71WS256N is a little more flexible, allowing addresses to be loaded non-sequentially.

4.8 CFI

Since these two devices differ in performance, device geometry and other features, some entries in their corresponding CFI tables are different. Those entries that are different in the two devices are listed in Table 4.6.

Table 4.6 CFI Comparison

Address	Description
0x1Fh	Typical timeout per single byte/word write
0x23h	Max timeout for byte/word write
0x24h	Max timeout for buffer write
0x27h	Device Size
0x31h - 0x34h	Erase Block Region 2 information
0x45h	Silicon Technology
0x4A	Simultaneous operation; Number of sectors in all banks except boot bank
0x4c	Page Mode Type
0x4f	Top/Bottom Boot Sector Flag
0x52h	Secured Silicon Sector (customer OTP area) size
0x58-0x67	Region Information for all banks – sectors in each bank

4.9 Summary

While the majority of the command set and features relevant to software remain consistent between the S71WS512N and S71WS512P, users should consider the differences outlined in this application note to ensure a smooth migration path without the need to change software.

5. Appendix 1

This section details parameter comparisons between the S29WS256N and the S29WS512P.

Table 5.1 Absolute Maximum Ratings

S29WS256N		S29WS512P	
Parameter	**Max**	**Parameter**	**Max**
Storage Temperature Plastic Packages	-65°C to +150°C	Storage Temperature Plastic Packages	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +125°C	Ambient Temperature with Power Applied	-65°C to +125°C
Voltage with Respect to Ground: All Inputs and I/Os except as noted below	-0.5 V to V_{CC} + 0.5 V	Voltage with Respect to Ground: All Inputs and I/Os except as noted below	-0.5 V to V_{CC} + 0.5 V
V_{CC}	-0.5 V to 2.5 V	V_{CC}	-0.5 V to 2.5 V
ACC	-0.5 V to 2.5 V	ACC	-0.5 V to 2.5 V
Output Short Circuit Current	100 mA	Output Short Circuit Current	100 mA

Table 5.2 Operating Ranges

S29WS256N		S29WS512P	
Parameter	**Max**	**Parameter**	**Max**
Ambient Temperature (TA)	-25°C to +85°C	Ambient Temperature (TA)	-25°C to +85°C
V_{CC} Supply Voltages	+1.70 V to + 1.95 V	V_{CC} Supply Voltages	+1.70 V to + 1.95 V

Table 5.3 S29WS256N DC Characteristics

Parameter	Description	Note	Min.	Typ	Max	Unit
I_{LI}	Input Load Circuit				+1	µA
I_{LO}	Output Leakage Current				+1	µA
I_{CCB}	V_{CC} Active Burst Read Current: Burst Length = 8	54 MHz		27	54	mA
		66 MHz		28	60	mA
		80 MHz		30	66	mA
		108 MHz		—	—	mA
	V_{CC} Active Burst Read Current: Burst Length = 16	54 MHz		28	48	mA
		66 MHz		30	54	mA
		80 MHz		32	60	mA
		108 MHz		—	—	mA
	V_{CC} Active Burst Read Current: Burst Length = Continuous	54 MHz		29	42	mA
		66 MHz		32	48	mA
		80 MHz		34	54	mA
		108 MHz		—	—	mA
	V_{CC} Active Burst Read Current: Burst Length = 8	54 MHz		32	36	mA
		66 MHz		35	42	mA
		80 MHz		38	48	mA
		108 MHz		—	—	mA
I_{CC1}	V_{CC} Active Asynchronous Read Current	10 MHz		34	45	mA
		5 MHz		17	26	mA
		1 MHz		4	7	mA
I_{CC2}	V_{CC} Active Write Current	V_{ACC}		1	5	µA
		V_{CC}		24	52.5	mA
I_{CC3}	V_{CC} Standby Current	V_{ACC}		1	5	µA
		V_{CC}		20	70	µA
I_{CC4}	V_{CC} Reset Current			70	250	µA
I_{CC5}	V_{CC} Active Current (Read While Write)			50	60	µA
I_{CC6}	V_{CC} Sleep Current			2	70	µA
I_{CC7}	V_{CC} Active Page Read Current 4-words			10	15	mA
I_{ACC}	Accelerated Program Current	V_{ACC}		6	20	mA
		V_{CC}		14	20	mA
V_{IL}	Input Low Voltage		-0.5		0.4	V
V_{IH}	Input High Voltage		V_{CC} - 0.4		V_{CC} + 0.4	V
V_{OL}	Output Low Voltage				0.1	V
V_{OH}	Output High Voltage		V_{CC}			V
V_{HH}	Voltage for Accelerated Program		8.5		9.5	V
V_{LKO}	Low V_{CC} Lock-out Voltage				1.4	V

Table 5.4 S29WS512P DC Characteristics

Parameter	Description	Note	Min.	Typ	Max	Unit
I_{LI}	Input Load Circuit				+1	µA
I_{LO}	Output Leakage Current				+1	µA
I_{CCB}	V_{CC} Active Burst Read Current: Burst Length = 8	54 MHz		—	—	—
		66 MHz		—	—	—
		80 MHz		—	—	—
		108 MHz		36	54	mA
	V_{CC} Active Burst Read Current: Burst Length = 16	54 MHz		—	—	—
		66 MHz		—	—	—
		80 MHz		—	—	—
		108 MHz		32	48	mA
	V_{CC} Active Burst Read Current: Burst Length = Continuous	54 MHz		—	—	—
		66 MHz		—	—	—
		80 MHz		—	—	—
		108 MHz		28	42	mA
	V_{CC} Active Burst Read Current: Burst Length = 8	54 MHz		—	—	—
		66 MHz		—	—	—
		80 MHz		—	—	—
		108 MHz		24	36	mA
I_{CC1}	V_{CC} Active Asynchronous Read Current	10 MHz		40	80	mA
		5 MHz		20	40	mA
		1 MHz		10	20	mA
I_{CC2}	V_{CC} Active Write Current	V_{ACC}		1	5	µA
		V_{CC}		20	40	mA
I_{CC3}	V_{CC} Standby Current	V_{ACC}		1	5	µA
		V_{CC}		20	40	µA
I_{CC4}	V_{CC} Reset Current			30	60	µA
I_{CC5}	V_{CC} Active Current (Read While Write)			40	60	µA
I_{CC6}	V_{CC} Sleep Current			5	20	µA
I_{CC7}	V_{CC} Active Page Read Current 4-words			10	15	mA
I_{ACC}	Accelerated Program Current	V_{ACC}		7	10	mA
		V_{CC}		15	20	mA
V_{IL}	Input Low Voltage		-0.5		0.4	V
V_{IH}	Input High Voltage		V_{CC} - 0.4		V_{CC} + 0.4	V
V_{OL}	Output Low Voltage				0.1	V
V_{OH}	Output High Voltage		V_{CC} - 0.1			V
V_{HH}	Voltage for Accelerated Program		8.5		9.5	V
V_{LKO}	Low V_{CC} Lock-out Voltage				1.4	V

Table 5.5 DC Characteristics Comparison

DC Characteristics		S29WS256N	S29WS512P
Ambient Temperature		-25°C to 85°C	-25°C to 85°C
Supply Voltage		+1.70 V to +1.95 V	+1.70 V to +1.95 V
V_{IL} (Input Low Voltage): V_{CC} = 1.8 V		-0.5 V / 0.4 V (Typ/Max)	-0.5 V / 0.4 V (Typ/Max)
V_{IH} (Input High Voltage): V_{CC} = 1.8 V		V_{CC} - 0.4 V / V_{CC} + 0.4 V (Typ/Max)	V_{CC} - 0.4 V / V_{CC} + 0.4 V (Typ/Max)
V_{OL} (Output Low Voltage): I_{OL} = 100 µA, V_{CC} = V_{CC}min = V_{CC}		0.1 V (Max)	0.1 V (Max)
V_{OH} (Output High Voltage): I_{OL} =100 µA, V_{CC} = V_{CC}min = V_{CC}		V_{CC} (Min)	V_{CC} - 0.1 V (Min)
V_{HH} (Voltage for Accelerated Program)		8.5 V - 9.5 V (Min/Max)	8.5 V - 9.5 V (Min/Max)
V_{LKO} (Low Vcc Lock-out Voltage)		1.4 V (Max)	1.4 V (Max)
V_{CC} Active Current V_{CC} =1.70-1.95 V	Standby	20 mA/70 mA (Typ/Max)	20 mA/40 mA (Typ/Max)
	Async. Read 54 MHz	17 mA/26 mA (Typ/Max)	20 mA/40 mA (Typ/Max)
	Page Read	10 mA/15 mA (Typ/Max)	10 mA/15 mA (Typ/Max)
	Burst Read 8-word Max-Freq.	80 MHz: 30 mA/66 mA (Typ/Max)	108 MHz: 36 mA/54 mA (Typ/Max)
	Burst Read 16-word Max-Freq	80 MHz: 32 mA/60 mA (Typ/Max)	108 MHz: 32 mA/48 mA (Typ/Max)
	Prog/Erase Current	24 mA/52.5 mA (Typ/Max)	20 mA/40 mA (Typ/Max)

6. AC Characteristics

Table 6.1 S29WS256N Asynchronous Read

Parameter	Description		Mode		54 MHz	66 MHz	80 MHz	108 MHz	Unit
t_{CE}	Access Time from CE# Low		—	Max	80			—	ns
t_{ACC}	Asynchronous Access Time		—	Max	80			—	ns
t_{AVDP}	AVD# Low Time		—	Min	8			—	ns
t_{AAVDS}	Address Setup Time to Rising Edge of AVD#		—	Min	4			—	ns
t_{AAVDH}	Address Hold Time from Rising Edge of AVD#		—	Min	7	6		—	ns
t_{OE}	Output Enable to Output Valid		—	Max	13.5			—	ns
t_{OEH}	Output Enable Hold Time	Read	—	Min	0			—	ns
		Toggled and Data# Polling	—	Min	10			—	ns
t_{OEZ}	Output Enable to High Z		—	Max	10			—	ns
t_{CAS}	CE# Setup Time to AVD#		—	Min	0			—	ns
t_{PACC}	Intra Page Access Time		—	Max	—				ns

Table 6.2 S29WS512P Asynchronous Read

Parameter	Description		Mode		54 MHz	66 MHz	80 MHz	108 MHz	Unit
t_{CE}	Access Time from CE# Low		Zero Hold	Max	83				ns
			Legacy		80				
t_{ACC}	Asynchronous Access Time		Zero Hold	Max	83				ns
			Legacy		80				
t_{AVDP}	AVD# Low Time		—	Min	8	8	8	7.5	ns
t_{AAVDS}	Address Setup Time to Rising Edge of AVD#		Zero Hold	Min	4	4	4	3.5	ns
			Legacy	Min	8	8	8	7.5	ns
t_{AAVDH}	Address Hold Time from Rising Edge of AVD#		Zero Hold	Min	7	6	6	4	ns
			Legacy	Min	0	0	0	0	ns
t_{OE}	Output Enable to Output Valid			Max	6				ns
t_{OEH}	Output Enable Hold Time	Read		Min	0	0	0	0	ns
		Toggled and Data# Polling		Min	10	10	10	6	ns
t_{OEZ}	Output Enable to High Z			Max	10	10	10	7	ns
t_{CAS}	CE# Setup Time to AVD#			Min	0	0	0	0	ns
t_{PACC}	Intra Page Access Time			Max	20	20	20	20	ns

Table 6.3 S29WS256N Synchronous Burst Read

Parameter	Description	Mode		54 MHz	66 MHz	80 MHz	108 MHz	Unit
t_{IACC}	Synchronous Access Time		Max	80			—	ns
t_{BACC}	Burst Access Time Valid Clock to Output Delay		Max	13.5	11.2	9	—	ns
t_{ACS}	Address Setup Time to Clock		Min	5	4		—	ns
t_{ACH}	Address Hold Time from Clock		Min	7	6		—	ns
t_{BDH}	Data Hold Time		Min	4	3		—	ns
$t_{RDY} = t_{CR}$	Chip Enable to RDY Active		Max	13.5	11.2	9	—	ns
t_{OE}	Output Enable to RDY Low		Max	13.5	11.2		—	ns
t_{CEZ}	Chip Enable to High Z		Max	10			—	ns
t_{OEZ}	Output Enable to High Z		Max	10			—	ns
t_{CES}	CE# Setup Time to Clock		Min	4			—	ns
t_{RACC}	Ready Access Time from Clock		Max	13.5	11.2	9	—	ns
t_{CAS}	CE# Setup Time to AVD#		Min	0			—	ns
t_{AVC}	AVD# Low to Clock Setup Time		Min	4			—	ns
t_{AVD}	AVD# Pulse		Min	8			—	ns

Table 6.4 S29WS512P Synchronous Burst Read

Parameter	Description	Mode		54 MHz	66 MHz	80 MHz	108 MHz	Unit
t_{IACC}	Synchronous Access Time	Legacy	Max	80				ns
		Zero Hold		83				
t_{BACC}	Burst Access Time Valid Clock to Output Delay		Max	13.5	11.2	9	7	ns
t_{ACS}	Address Setup Time to Clock	Legacy	Min	5	4	4	3.5	ns
		Zero Hold		6	6	6	6	
t_{ACH}	Address Hold Time from Clock	Legacy	Min	6	6	5	5	ns
		Zero Hold		0	0	0	0	
t_{BDH}	Data Hold Time		Min	4	3	3	2	ns
$t_{RDY} = t_{CR}$	Chip Enable to RDY Active		Max	7				ns
t_{OE}	Output Enable to RDY Low		Max	13.5	11.2	9	7	ns
t_{CEZ}	Chip Enable to High Z		Max	10	10	10	7	ns
t_{OEZ}	Output Enable to High Z		Max	10	10	10	7	ns
t_{CES}	CE# Setup Time to Clock		Min	4	4	4	3.5	ns
t_{RACC}	Ready Access Time from Clock		Max	13.5	11.2	9	6	ns
t_{CAS}	CE# Setup Time to AVD#		Min	0	0	0	0	ns
t_{AVC}	AVD# Low to Clock Setup Time		Min	4	4	4	5	ns
t_{AVD}	AVD# Pulse		Min	8	8	8	6	ns

Table 6.5 S29WS256N Erase / Programming Performance

Parameter		Description			54 MHz	66 MHz	80 MHz	108 MHz	Unit
JEDEC	Standard								
t_{AVAV}	t_{WC}	Write Cycle Time		Min	80			—	ns
t_{AVWL}	t_{AS}	Address Setup Time	Synchronous	Min	5			—	ns
			Asynchronous		0			—	ns
t_{WLAX}	t_{AH}	Address Hold Time	Synchronous	Min	9			—	ns
			Asynchronous		20			—	
	t_{AVDP}	AVD# Low Time		Min	8			—	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	45	20		—	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0			—	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write		Min	0			—	ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0			—	ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0			—	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	30			—	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	20			—	ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0			—	ns
	t_{VID}	V_{ACC} Rise and Fall Time		Min	500			—	ns
	t_{VIDS}	V_{ACC} Setup Time (During Accelerated Programming)		Min	1			—	µs
t_{ELWL}	t_{CS}	CE# Setup Time to WE#		Min	5			—	ns
	t_{AVSW}	AVD# Setup Time to WE#		Min	5			—	ns
	t_{AVHW}	AVD# Hold Time to WE#		Min	5			—	ns
	t_{AVSC}	AVD# Setup Time to CLK		Min	5			—	ns
	t_{AVHC}	AVD# Hold Time to CLK		Min	5			—	ns
	t_{SEA}	Sector Erase Accept Time-out		Max	50			—	µs
	t_{ESL}	Erase Suspend Latency		Max	20			—	µs
	t_{PSL}	Program Suspend Latency		Max	20			—	µs
	t_{ASP}	Toggle Time During Erase within a Protected Sector		Typ	0			—	µs
	t_{PSP}	Toggle Time During Programming Within a Protected Sector		Typ	0			—	µs
	t_{CSW}	Clock Setup Time to WE#		Min	5			—	ns
	t_{WEP}	Noise Pulse Margin on WE#		Max	3			—	ns

Table 6.6 S29WS512P Erase / Programming Performance

Parameter		Description			54 MHz	66 MHz	80 MHz	108 MHz	Unit
JEDEC	Standard								
t_{AVAV}	t_{WC}	Write Cycle Time		Min	60				ns
t_{AVWL}	t_{AS}	Address Setup Time	Synchronous (Legacy Mode)	Min	5	5	5	3.5	ns
			Asynchronous (Legacy Mode)		2	2	2	2	
			Synchronous (Zero Hold Mode)		9	9	9	6	
			Asynchronous (Zero Hold Mode)		6	6	6	6	
t_{WLAX}	t_{AH}	Address Hold Time	Synchronous (Legacy Mode)	Min	7	7	6	5	ns
			Asynchronous (Legacy Mode)		7	7	6	5	
			Synchronous (Zero Hold Mode)		0	0	0	0	
			Asynchronous (Zero Hold Mode)		0	0	0	0	
	t_{AVDP}	AVD# Low Time		Min	6				ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	20				ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write		Min	0				ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	25				ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	20				ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0				ns
	t_{VID}	V_{ACC} Rise and Fall Time		Min	500				ns
	t_{VIDS}	V_{ACC} Setup Time (During Accelerated Programming)		Min	1				µs
t_{ELWL}	t_{CS}	CE# Setup Time to WE#		Min	4				ns
	t_{AVSW}	AVD# Setup Time to WE#		Min	4				ns
	t_{AVHW}	AVD# Hold Time to WE#		Min	4				ns
	t_{AVSC}	AVD# Setup Time to CLK	Legacy Mode	Min	5	5	5	3	ns
			Zero Hold Mode		6	6	6	6	
	t_{AVHC}	AVD# Hold Time to CLK	Legacy Mode	Min	5	5	5	3	ns
			Zero Hold Mode		0	0	0	0	
	t_{SEA}	Sector Erase Accept Time-out		Min	50				µs
	t_{ESL}	Erase Suspend Latency		Min	20				µs
	t_{PSL}	Program Suspend Latency		Min	20				µs
	t_{ASP}	Toggle Time During Erase within a Protected Sector		Typ	0				µs
	t_{PSP}	Toggle Time During Programming Within a Protected Sector		Typ	0				µs
	t_{CSW}	Clock Setup Time to WE#		—	—				—
	t_{WEP}	Noise Pulse Margin on WE#		Max	3				ns

7. Appendix 2

Table 7.1 Wait State Requirements

S29WS256N		S29WS512P
Wait State Requirement	**Max Frequency**	**Wait State Requirement**
2	0.1 MHz < Freq ≤ 14 MHz	2
3	14 MHz < Freq ≤ 27 MHz	3
4	27 MHz < Freq ≤ 40 MHz	4
5	40 MHz < Freq ≤ 54 MHz	5
6	54 MHz < Freq ≤ 67 MHz	6
7	67 MHz < Freq ≤ 80 MHz	7
—	80 MHz < Freq ≤ 95 MHz	8
—	95 MHz < Freq ≤ 108 MHz	9

Figure 7.1 Latency Table for Initial Wait

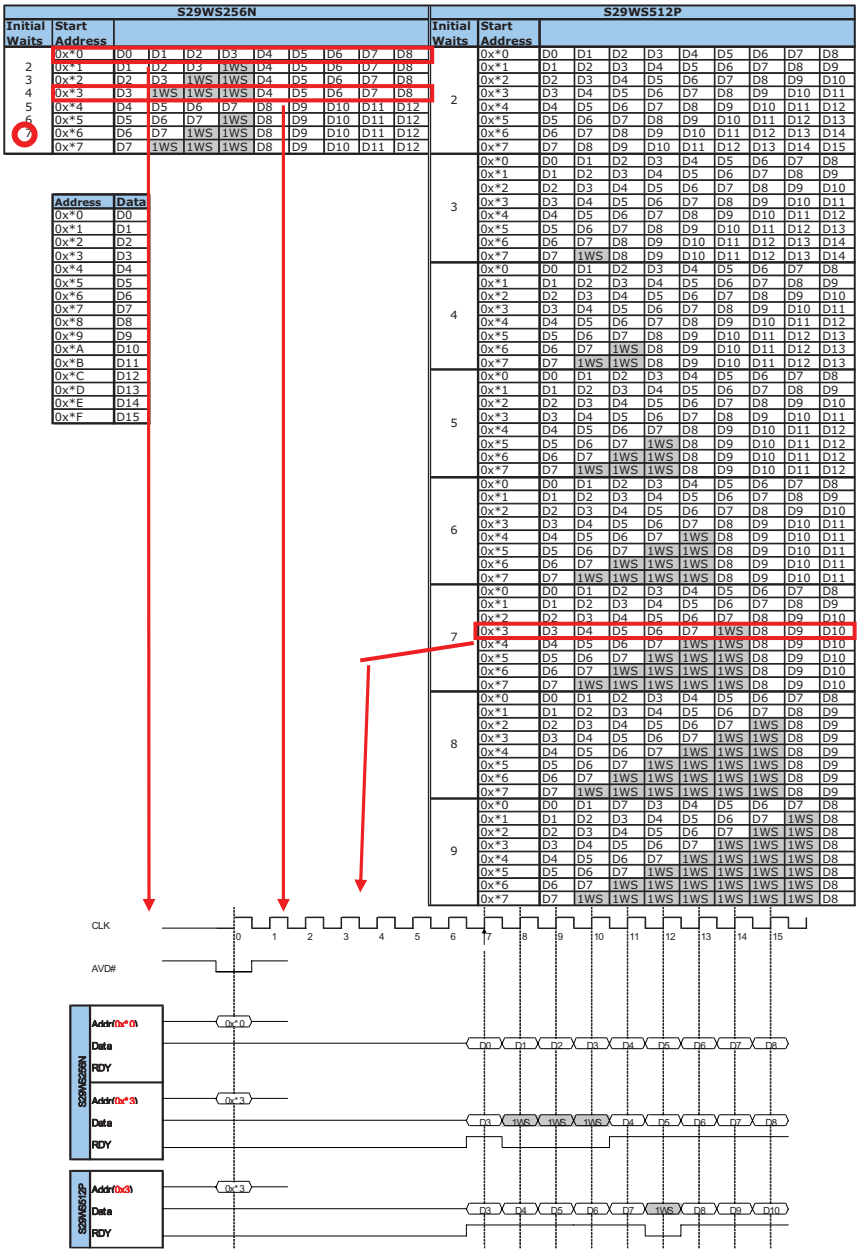


Figure 7.2 Latency Table for 128 Words Boundary Crossing

Address	Data
0x0	D0
0x1	D1
.	.
0x78	D120
0x79	D121
0x7A	D122
0x7B	D123
0x7C	D124
0x7D	D125
0x7E	D126
0x7F	D127
0x80	D128
0x81	D129
0x82	D130
0x83	D131
0x84	D132
0x85	D133
0x86	D134
0x87	D135
0x88	D136

S29WS256N														
Initial Waits	Start Address													
2	0x78	D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	
	0x79	D121	D122	D123	1WS	D124	D125	D126	D127	D128	D129	D130	D131	
	0x7A	D122	D123	1WS	1WS	D124	D125	D126	D127	D128	D129	D130	D131	
	0x7B	D123	1WS	1WS	1WS	D124	D125	D126	D127	D128	D129	D130	D131	
	0x7C	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7D	D125	D126	D127	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7E	D126	D127	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7F	D127	1WS	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
3	0x78	D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	
	0x79	D121	D122	D123	1WS	D124	D125	D126	D127	D128	D129	D130	D131	
	0x7A	D122	D123	1WS	1WS	D124	D125	D126	D127	D128	D129	D130	D131	
	0x7B	D123	1WS	1WS	1WS	D124	D125	D126	D127	D128	D129	D130	D131	
	0x7C	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7D	D125	D126	D127	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7E	D126	D127	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7F	D127	1WS	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
4	0x78	D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	
	0x79	D121	D122	D123	1WS	D124	D125	D126	D127	D128	D129	D130	D131	
	0x7A	D122	D123	1WS	1WS	D124	D125	D126	D127	D128	D129	D130	D131	
	0x7B	D123	1WS	1WS	1WS	D124	D125	D126	D127	D128	D129	D130	D131	
	0x7C	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7D	D125	D126	D127	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7E	D126	D127	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7F	D127	1WS	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
5	0x78	D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	
	0x79	D121	D122	D123	1WS	D124	D125	D126	D127	D128	D129	D130	D131	
	0x7A	D122	D123	1WS	1WS	D124	D125	D126	D127	D128	D129	D130	D131	
	0x7B	D123	1WS	1WS	1WS	D124	D125	D126	D127	D128	D129	D130	D131	
	0x7C	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7D	D125	D126	D127	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7E	D126	D127	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7F	D127	1WS	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
6	0x78	D120	D121	D122	D123	D124	D125	D126	D127	1WS	D128	D129	D130	
	0x79	D121	D122	D123	1WS	D124	D125	D126	D127	1WS	D128	D129	D130	
	0x7A	D122	D123	1WS	1WS	D124	D125	D126	D127	1WS	D128	D129	D130	
	0x7B	D123	1WS	1WS	1WS	D124	D125	D126	D127	1WS	D128	D129	D130	
	0x7C	D124	D125	D126	D127	1WS	D128	D129	D130	D131	D132	D133	D134	
	0x7D	D125	D126	D127	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	
	0x7E	D126	D127	1WS	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	
	0x7F	D127	1WS	1WS	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	
7	0x78	D120	D121	D122	D123	D124	D125	D126	D127	1WS	1WS	D128	D129	
	0x79	D121	D122	D123	1WS	D124	D125	D126	D127	1WS	1WS	D128	D129	
	0x7A	D122	D123	1WS	1WS	D124	D125	D126	D127	1WS	1WS	D128	D129	
	0x7B	D123	1WS	1WS	1WS	D124	D125	D126	D127	1WS	1WS	D128	D129	
	0x7C	D124	D125	D126	D127	1WS	1WS	D128	D129	D130	D131	D132	D133	
	0x7D	D125	D126	D127	1WS	1WS	1WS	D128	D129	D130	D131	D132	D133	
	0x7E	D126	D127	1WS	1WS	1WS	1WS	D128	D129	D130	D131	D132	D133	
	0x7F	D127	1WS	1WS	1WS	1WS	1WS	D128	D129	D130	D131	D132	D133	

S29WS512P														
Initial Waits	Start Address													
2	0x78	D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	
	0x79	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	
	0x7A	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	
	0x7B	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	
	0x7C	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7D	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	D136	
	0x7E	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	
	0x7F	D127	1WS	D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	
3	0x78	D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	
	0x79	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	
	0x7A	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	
	0x7B	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	
	0x7C	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7D	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	D136	
	0x7E	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	
	0x7F	D127	1WS	D128	D129	D130	D131	D132	D133	D134	D135	D136	D137	
4	0x78	D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	
	0x79	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	
	0x7A	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	
	0x7B	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	
	0x7C	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7D	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	D136	
	0x7E	D126	D127	1WS	D128	D129	D130	D131	D132	D133	D134	D135	D136	
	0x7F	D127	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	D135	D136	
5	0x78	D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	
	0x79	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	
	0x7A	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	
	0x7B	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	
	0x7C	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7D	D125	D126	D127	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7E	D126	D127	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
	0x7F	D127	1WS	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	D135	
6	0x78	D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	
	0x79	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	
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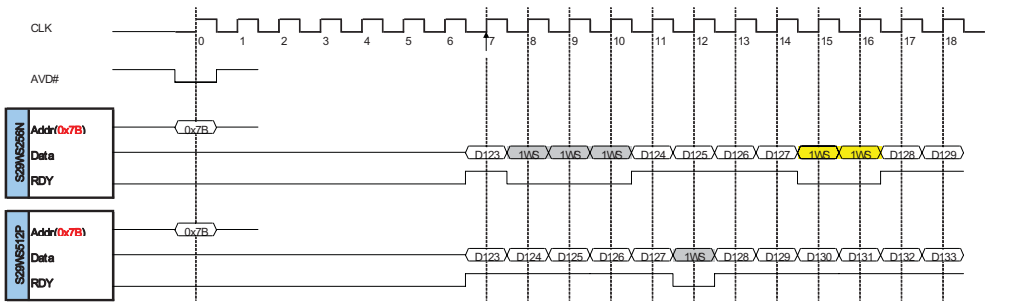
	0x7B	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	
	0x7C	D124	D125	D126	D127	1WS	D128	D129	D130	D131	D132	D133	D134	
	0x7D	D125	D126	D127	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	
	0x7E	D126	D127	1WS	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	
	0x7F	D127	1WS	1WS	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	
7	0x78	D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	
	0x79	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	
	0x7A	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	
	0x7B	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	D133	D134	
	0x7C	D124	D125	D126	D127	1WS	D128	D129	D130	D131	D132	D133	D134	
	0x7D	D125	D126	D127	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	
	0x7E	D126	D127	1WS	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	
	0x7F	D127	1WS	1WS	1WS	1WS	D128	D129	D130	D131	D132	D133	D134	
8	0x78	D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	
	0x79	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	D132	
	0x7A	D122	D123	D124	D125	D126	D127	1WS	D128	D129	D130	D131	D132	
	0x7B	D123	D124	D125	D126	D127	1WS	1WS	D128	D129	D130	D131	D132	
	0x7C	D124	D125	D126	D127	1WS	1WS	1WS	D128	D129	D130	D131	D132	
	0x7D	D125	D126	D127	1WS	1WS	1WS	1WS	D128	D129	D130	D131	D132	
	0x7E	D126	D127	1WS	1WS	1WS	1WS	1WS	D128	D129	D130	D131	D132	
	0x7F	D127	1WS	1WS	1WS	1WS	1WS	1WS	D128	D129	D130	D131	D132	
9	0x78	D120	D121	D122	D123	D124	D125	D126	D127	D128	D129	D130	D131	
	0x79	D121	D122	D123	D124	D125	D126	D127	1WS	D128	D129	D130	D131	
	0x7A	D122	D123	D124	D125	D126	D127	1WS	1WS	D128	D129	D130	D131	
	0x7B	D123	D124	D125	D126	D127	1WS	1WS	1WS	D128	D129	D130	D131	
	0x2C	D124	D125	D126	D127	1WS	1WS	1WS	1WS	D128	D129	D130	D131	
	0x7D	D125	D126	D127	1WS	1WS	1WS	1WS	1WS	D128	D129	D130	D131	
	0x7E	D126	D127	1WS	1WS	1WS	1WS	1WS	1WS	D128	D129	D130	D131	
	0x7F	D127	1WS	1WS	1WS	1WS	1WS	1WS	1WS	D128	D129	D130	D131	



8. Revision History

Section	Description
Revision 01 (October 3, 2006)	
	Initial release

Colophon

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