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PRODUCT OVERVIEW

OVERVIEW

The S3C7324 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With features such as LCD direct drive capability, 4-channel A/D converter, 24-bit AM/FM frequency counter and watch timer, the S3C7324 offers an excellent design solution for a wide variety of applications that require LCD functions and audio applications.

Up to 32 pins of the 64-pin QFP package, it can be dedicated to I/O. Five vectored interrupts provide fast response to internal and external events. In addition, the S3C7324's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

OTP

The S3C7324 microcontroller is also available in OTP (One Time Programmable) version, S3P7324. The S3P7324 microcontroller has an on-chip 4-Kbyte one-time-programmable EPROM instead of masked ROM. The S3P7324 is comparable to S3C7324, both in function and in pin configuration.

FEATURES

Memory

- 256 × 4-bit RAM
- 4096 × 8-bit ROM

I/O Pins

- Input only: 8 pins
- I/O: 16 pins
- Output only: 8 pins sharing with segment driver outputs

LCD Controller/Driver

- Maximum 14-digit LCD direct drive capability
- 28 segment and 4 common pins
- Display modes: Static, 1/2 duty (1/2 bias), 1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias)
- Internal resistor circuit for LCD bias

8-Bit Basic Timer

- Programmable interval timer
- Watchdog timer

8-Bit Timer

- Programmable 8-bit timer

Watch Timer

- Real-time and interval time measurement
- Four frequency outputs to BUZ pin
- Clock source generation for LCD

24-Bit Frequency Counter (FC)

- Level = 300mVpp (Min.)
- AMF input range = 0.5 MHz to 10 MHz
- FMF input range = 30 MHz to 150 MHz

A/D Converter

- 4-channels with 8-bit resolution
- 17 μ s (Min.) conversion speed

Bit Sequential Carrier

- Support 16-bit serial data transfer in arbitrary format

Interrupts

- Two internal vectored interrupts
- Three external vectored interrupts
- Two quasi-interrupts

Memory-Mapped I/O Structure

- Data memory bank 15

Two Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (main system clock stops)
- Subsystem clock stops

Oscillation Sources

- Crystal, ceramic, or RC for main system clock
- Crystal or external oscillator for subsystem clock
- Main system clock frequency: 4.19 MHz (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 μ s at 4.19 MHz (main)
- 122 μ s at 32.768 kHz (subsystem)

Operating Temperature

- -40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V at 3 MHz
- 3.0 V to 5.5 V at FC mode

Package Type

- 64-pin QFP

BLOCK DIAGRAM

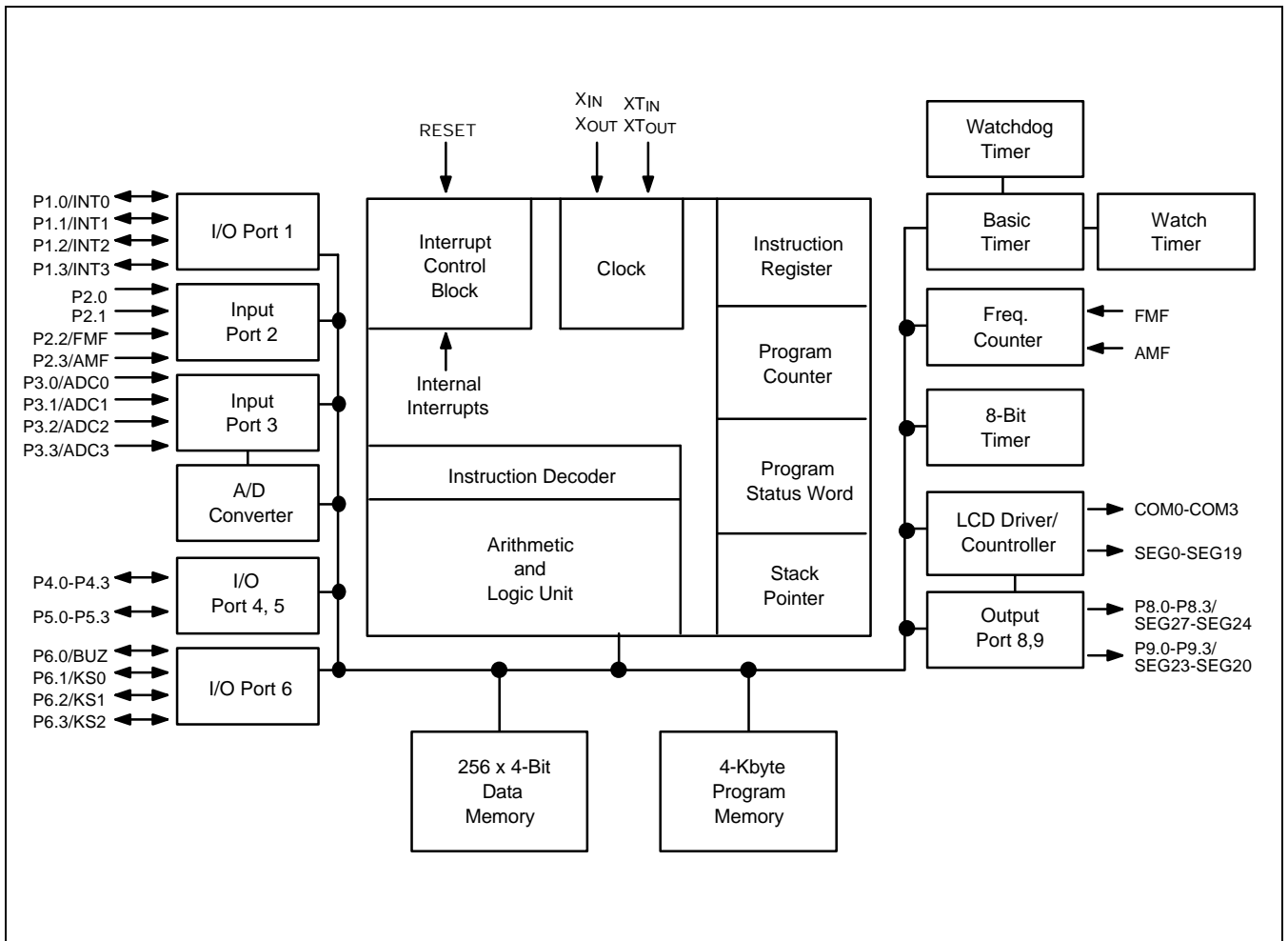


Figure 1-1. S3C7324 Simplified Block Diagram

PIN ASSIGNMENTS

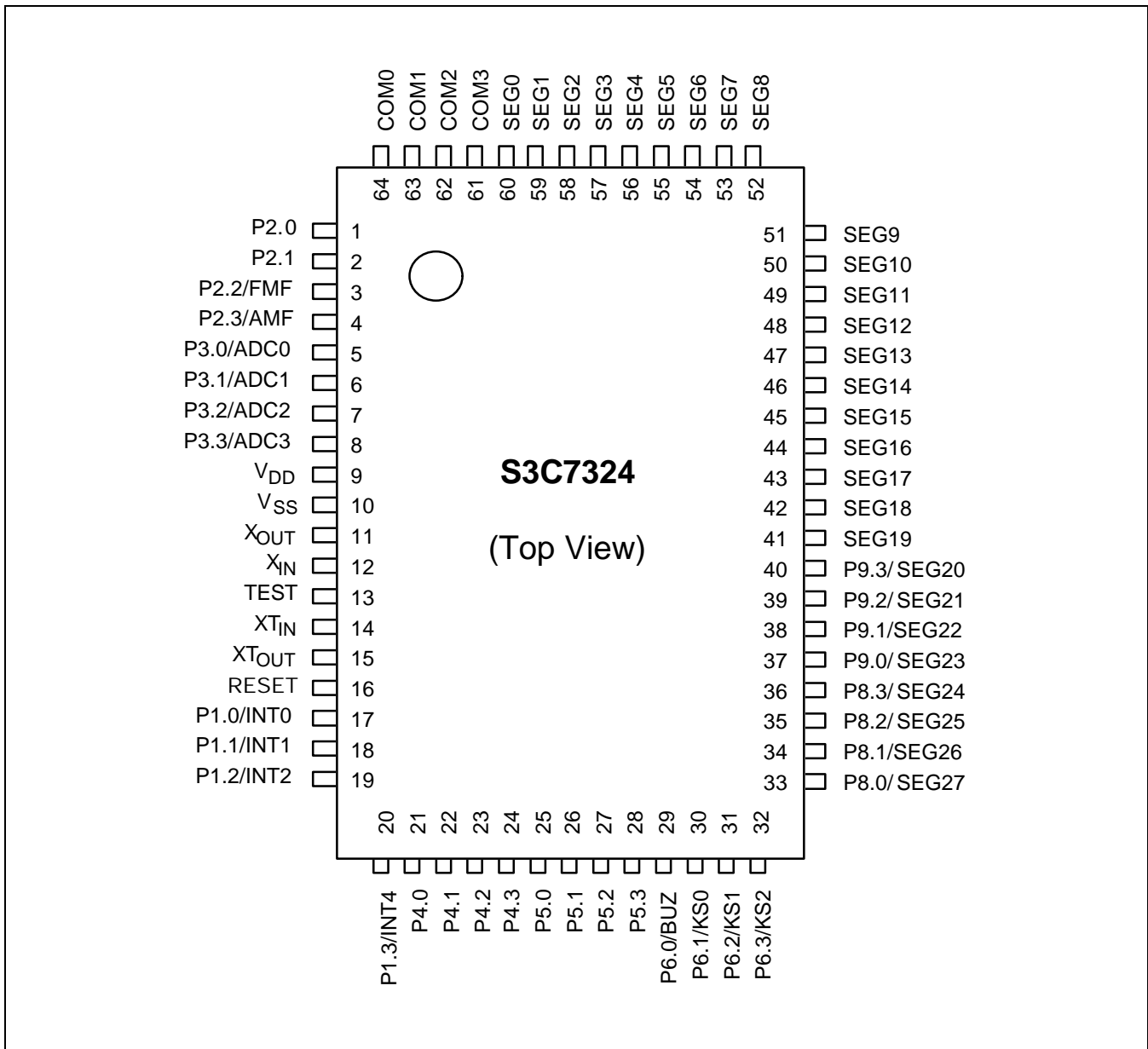


Figure 1-2. S3C7324 64-QFP Pin Assignment

PIN DESCRIPTIONS

Table 1-1. S3C7324 Pin Descriptions

| Pin Name | Pin Type | Description | Number | Share Pin | Reset Value | Circuit Type |
|--------------------------------------|----------|---|----------------------|------------------------------|-------------|--------------------------|
| P1.0 P1.1 P1.2 P1.3 | I/O | 4-bit I/O port. 1-bit or 4-bit read, write, and test are possible. Each pin can be specified as input or output port. Pull-up resistors can be configured by software. | 17 18 19 20 | INT0 INT1 INT2 INT4 | Input | D-4 |
| P2.0 P2.1 P2.2 P2.3 | I | 4-bit input port. 1-bit and 4-bit read and test are possible. Pull-up resistors can be configured by software. | 1 2 3 4 | – – FMF AMF | Input | A-4 A-4 B-4 B-4 |
| P3.0 P3.1 P3.2 P3.3 | I | 4-bit input port. 1-bit and 4-bit read and test are possible Pull-up resistors can be configured by software. | 5 6 7 8 | ADC0 ADC1 ADC2 ADC3 | Input | F-13 |
| P4.0–P4.3 P5.0–P5.3 | I/O | 4-bit I/O ports. N-channel open-drain output up to 5 V. 1-bit and 4-bit read, write, and test are possible. Ports 4 and 5 can be paired to support 8-bit data. Pull-up resistors can be configured by software. | 21–24 25–28 | – – | Input | E-2 |
| P6.0 P6.1 P6.2 P6.3 | I/O | 1-bit and 4-bit read, write, and test are possible. Each pin can be specified as input or output port. Pull-up resistors can be configured by software. | 29 30 31 32 | BUZ KS0 KS1 KS2 | Input | D-2 D-4 D-4 D-4 |
| SEG0–SEG19 | O | LCD segment signal output | 60–61 | – | Output | H-16 |
| P8.0–P8.3 P9.0–P9.3 | O | 4-bit output ports. 1-bit and 4-bit write and test are possible. Ports 8 and 9 can be paired to support 8-bit data. | 33–36 37–40 | SEG27– SEG20 | Output | H-16 |
| COM0–COM3 | O | LCD common signal output | 64–61 | – | Output | H-16 |
| V _{DD} | – | Main power supply | 9 | – | – | – |
| V _{SS} | – | Main ground | 10 | – | – | – |
| X _{OUT} , X _{IN} | – | Crystal, ceramic, or RC oscillator pins for main system clock. (For external clock input, use X _{IN} and input X _{IN} 's reverse phase to X _{OUT}) | 11,12 | – | – | – |
| XT _{OUT} , XT _{IN} | – | Crystal oscillator pin for a subsystem clock. (For external clock input, use XT _{IN} and input XT _{IN} 's reverse phase to XT _{OUT}) | 15,14 | – | – | – |

Table 1-1. S3P7324 Pin Descriptions (Continued)

| Pin Name | Pin Type | Description | Number | Share Pin | Reset Value | Circuit Type |
|--------------|----------|--|----------|------------------------|-------------|--------------|
| SEG20–SEG27 | O | LCD segment signal output | 40–33 | P9.0–P9.3 P8.0–P8.3 | Output | H-16 |
| ADC0–ADC3 | I | ADC input ports | 5–8 | P3.0–P3.3 | Input | F-13 |
| FMF AMF | I | External FM/AM frequency inputs | 3 4 | P2.2 P2.3 | Input | B-4 |
| INT4 | I | External interrupt input with detection of rising or falling edges. | 20 | P1.3 | Input | A-4 |
| INT2 | I | Quasi-interrupt with detection of rising edge signals. | 19 | P1.2 | Input | A-4 |
| INT1 INT0 | I | External interrupt. The triggering edges for INT0 and INT1 are able to be selected. Only INT0 is synchronized with the system clock. | 18 17 | P1.1 P1.0 | Input | A-4 |
| BUZ | O | 2, 4, 8, or 16 kHz frequency output for buzzer sound with 4.19 MHz main system clock. | 29 | P6.0 | Input | D-2 |
| KS0–KS2 | I | Quasi-interrupt input with falling edge detection. | 30–32 | P6.1–P6.3 | Input | D-4 |
| RESET | I | System reset signal | 16 | – | Input | B |
| TEST | – | System test pin(must be connected to V_{SS}) | 13 | – | – | – |

NOTE: Pull-up resistors for all I/O ports automatically disabled if they are configured to output mode.

PIN CIRCUIT DIAGRAMS

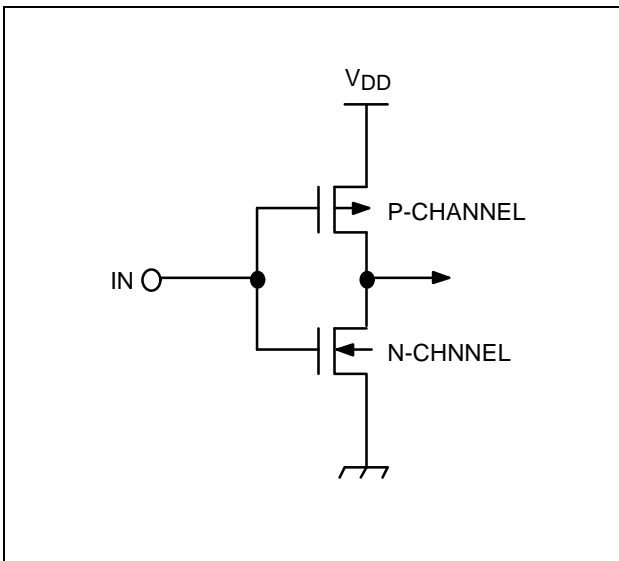


Figure 1-3. Pin Circuit Type A

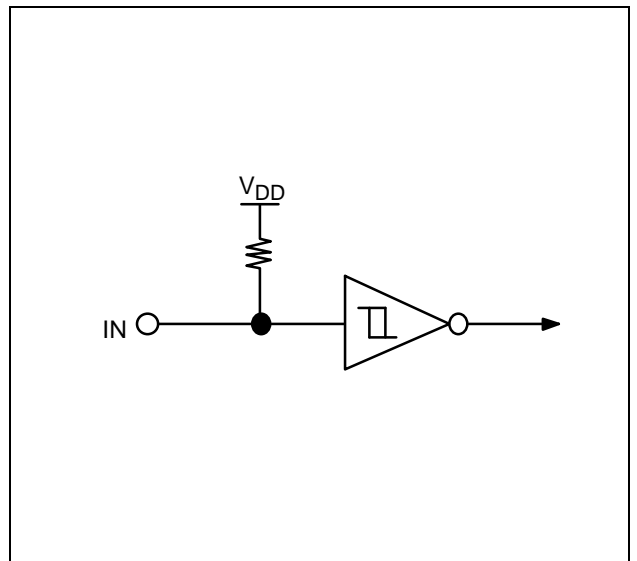


Figure 1-5. Pin Circuit Type B

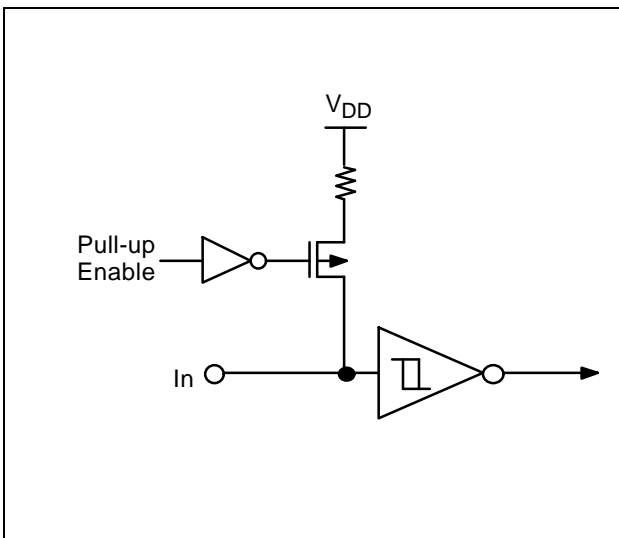


Figure 1-4. Pin Circuit Type A-4

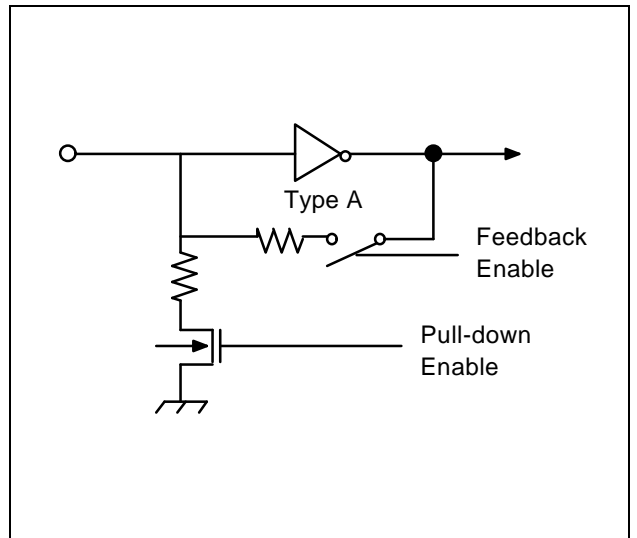


Figure 1-6. Pin Circuit Type B-4

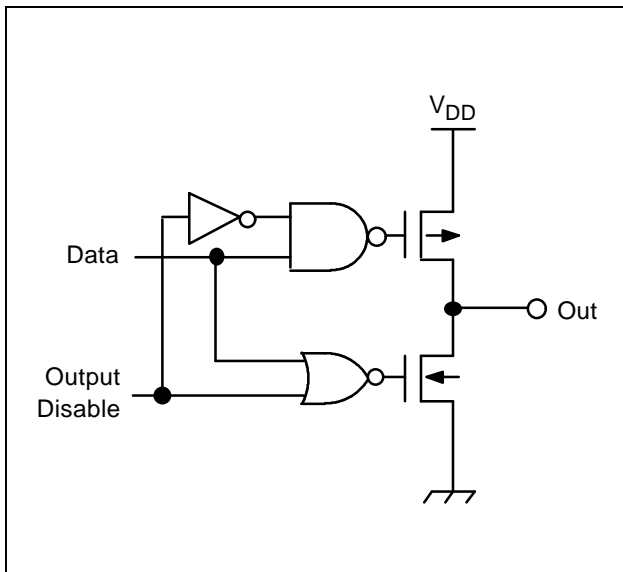


Figure 1-7. Pin Circuit Type C

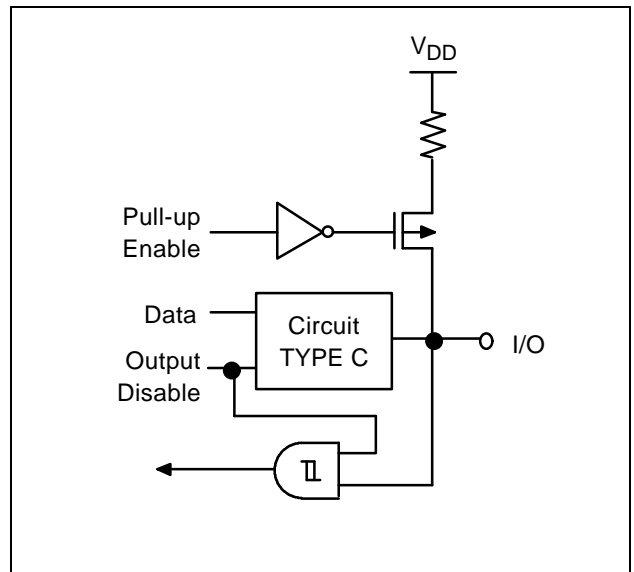


Figure 1-9. Pin Circuit Type D-4

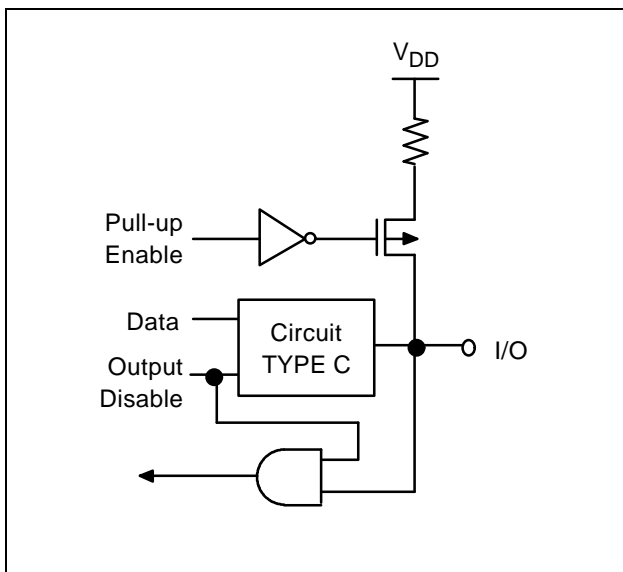


Figure 1-8. Pin Circuit Type D-2

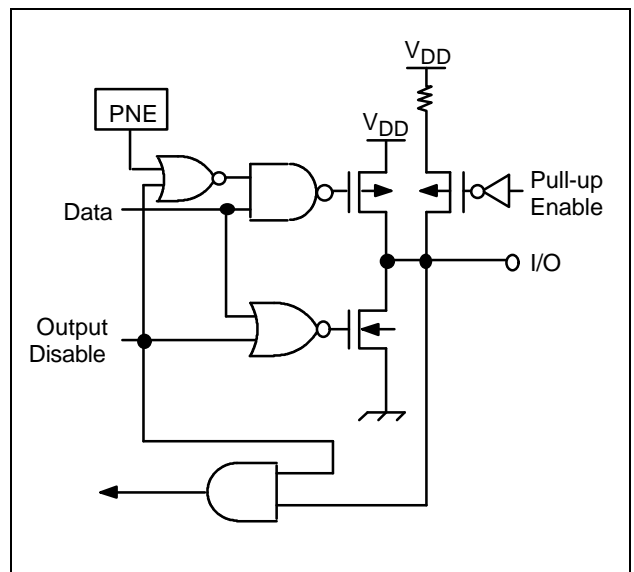


Figure 1-10. Pin Circuit Type E-2

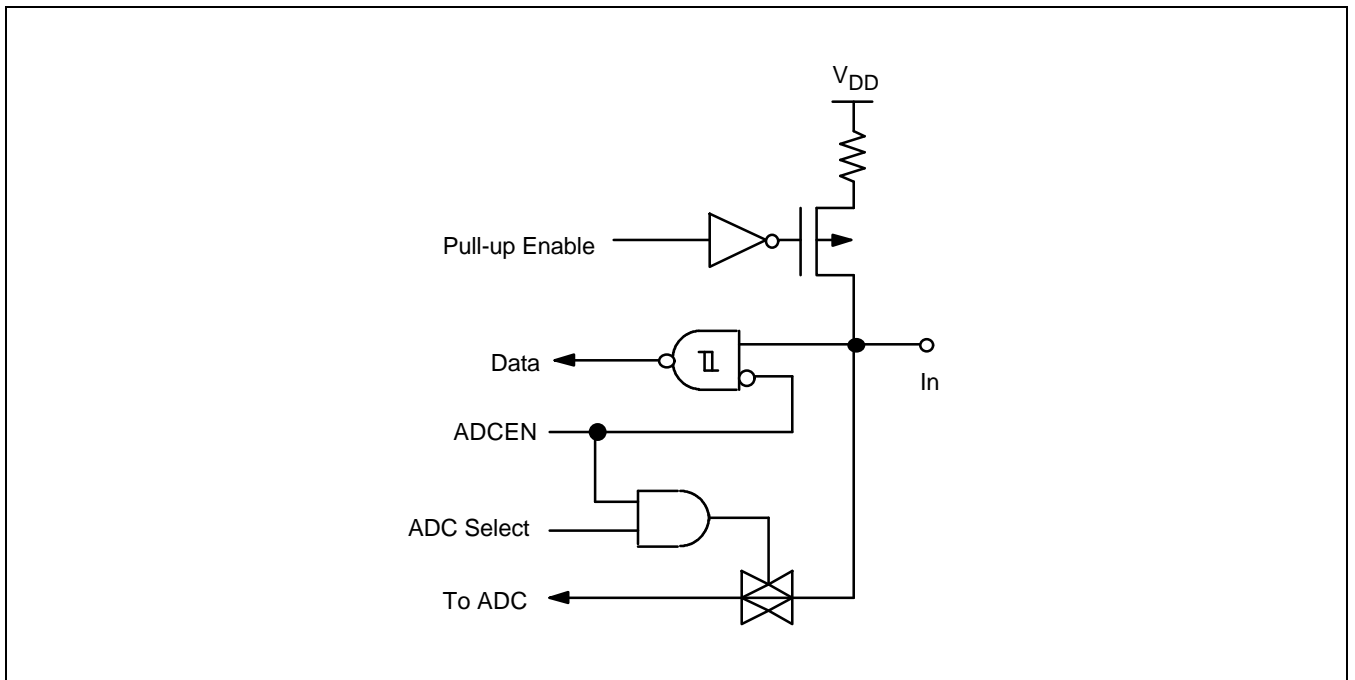


Figure 1-11. Pin Circuit Type F-13

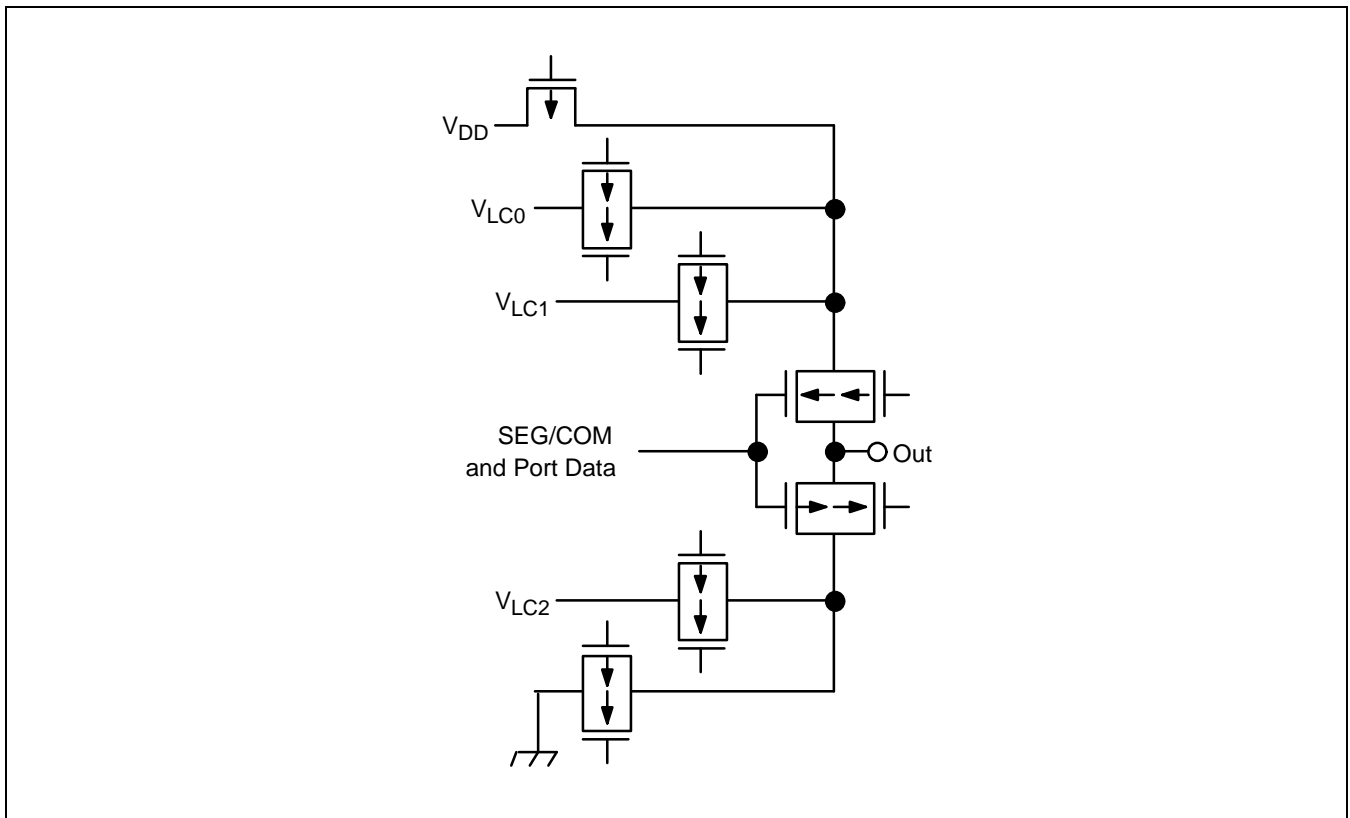


Figure 1-12. Pin Circuit Type H-16

15 ELECTRICAL DATA

OVERVIEW

In this section, information on S3C7324 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

Standard Electrical Characteristics

- Absolute maximum ratings
- D.C. electrical characteristics
- Main system clock oscillator characteristics
- Subsystem clock oscillator characteristics
- I/O capacitance
- A.C. electrical characteristics
- Operating voltage range

Miscellaneous Timing Waveforms

- A.C timing measurement point
- Clock timing measurement at X_{IN}
- Clock timing measurement at XT_{IN}
- Input timing for RESET
- Input timing for external interrupts

Stop Mode Characteristics and Timing Waveforms

- RAM data retention supply voltage in stop mode
- Stop mode release timing when initiated by RESET
- Stop mode release timing when initiated by an interrupt request

Table 15-1. Absolute Maximum Ratings

 $(T_A = 25\text{ }^\circ\text{C})$

| Parameter | Symbol | Conditions | Rating | Units |
|-----------------------|-----------|-------------------------------------|-------------------------|------------------|
| Supply Voltage | V_{DD} | – | – 0.3 to + 6.5 | V |
| Input Voltage | V_{IN} | All I/O ports | – 0.3 to $V_{DD} + 0.3$ | |
| Output Voltage | V_O | – | – 0.3 to $V_{DD} + 0.3$ | |
| Output Current High | I_{OH} | One I/O port active | – 15 | mA |
| | | All I/O ports active | – 30 | |
| Output Current Low | I_{OL} | One I/O port active | + 30 (Peak value) | |
| | | | + 15 (note) | |
| | | Total value for ports 1, 4, 5 and 6 | + 100 (Peak value) | |
| | | | + 60 (note) | |
| Operating Temperature | T_A | – | – 40 to + 85 | $^\circ\text{C}$ |
| Storage Temperature | T_{stg} | – | – 65 to + 150 | |

NOTE: The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 15-2. D.C. Electrical Characteristics

 $(T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------|-----------|--|----------------|-----|--------------|-------|
| Input high voltage | V_{IH1} | All input pins except those specified below | $0.7 V_{DD}$ | – | V_{DD} | V |
| | V_{IH2} | P1, P3, RESET, P2.0–1 and P6.1–3 | $0.8 V_{DD}$ | | V_{DD} | |
| | V_{IH3} | X_{IN} , X_{OUT} , XT_{IN} , and XT_{OUT} | $V_{DD} - 0.1$ | | V_{DD} | |
| Input low voltage | V_{IL1} | All input pins except those specified below | – | – | $0.3 V_{DD}$ | V |
| | V_{IL2} | P1, P3, RESET, P2.0–1 and P6.1–3 | | | $0.2 V_{DD}$ | |
| | V_{IL3} | X_{IN} , X_{OUT} , XT_{IN} , and XT_{OUT} | | | 0.1 | |
| Output high voltage | V_{OH1} | $V_{DD} = 4.5\text{ V}$ to 5.5 V $I_{OH} = -1\text{ mA}$ Ports 1, 4, 5, and 6 | $V_{DD} - 1.0$ | – | – | V |
| | V_{OH2} | $V_{DD} = 4.5\text{ V}$ to 5.5 V $I_{OH} = -100\text{ }\mu\text{A}$ Port 8 and 9 | $V_{DD} - 2.0$ | | | |

Table 15-2. D.C. Electrical Characteristics (Continued)

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|------------------------------------|-------------------|---|-----|-----|-----|-------|
| Output low voltage | V _{OL1} | V _{DD} = 4.5 V to 5.5 V I _{OL} = 15 mA, Ports 1, 4, 5, and 6 | – | 0.4 | 2 | V |
| | V _{OL2} | V _{DD} = 4.5 V to 5.5 V I _{OL} = 100 μA ; Ports 8 and 9 | – | – | 1 | |
| Input high leakage current (note) | I _{LIH1} | V _{IN} = V _{DD} All input pins | – | – | 3 | μA |
| Input low leakage current (note) | I _{LIL1} | V _{IN} = 0 V All input pins | – | – | –3 | |
| Output high leakage current (note) | I _{LOH1} | V _{OUT} = V _{DD} All output pins | – | – | 3 | |
| Output low leakage current (note) | I _{LOL} | V _{OUT} = 0 V All output pins | | | –3 | |
| Pull-up resistor | R _{L1} | V _{IN} = 0 V; V _{DD} = 5 V Ports 1, 2, 3, 4, 5, and 6 | 20 | 40 | 80 | KΩ |
| | | V _{DD} = 3 V | 30 | 95 | 200 | |
| | R _{L2} | V _{IN} = 0 V; V _{DD} = 5 V RESET | 100 | 230 | 400 | |
| | | V _{DD} = 3 V | 200 | 480 | 800 | |

NOTE: Except for X_{IN}, X_{OUT}, XT_{IN}, and XT_{OUT}

Table 15-2. D.C. Electrical Characteristics (Continued)

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|-------------------------------|-------------------|---|------|------|------|-------|
| LCD voltage dividing resistor | R _{LCD} | T _A = 25 °C | 60 | 84 | 130 | KΩ |
| COM output impedance | R _{COM} | V _{DD} = 5 V | - | 3 | 6 | |
| | | V _{DD} = 3 V | | 5 | 15 | |
| SEG output impedance | R _{SEG} | V _{DD} = 5 V | - | 3 | 6 | |
| | | V _{DD} = 3 V | | 5 | 15 | |
| COM output voltage deviation | V _{DC} | V _{DD} = 5 V (V _{LC0} -COMi) I _o = ± 15μA (I = 0-3) | - | ± 45 | ± 90 | mV |
| SEG output voltage deviation | V _{DS} | V _{DD} = 5 V (V _{LC0} -SEGi) I _o = ± 15μA (I = 0-27) | - | ± 45 | ± 90 | |
| Oscillator feedback resistor | R _{OSC1} | V _{DD} = 5.0 V; T _A = 25; X _{IN} = V _{DD} , X _{OUT} = 0 V | 300 | 600 | 1500 | KΩ |
| | R _{OSC2} | V _{DD} = 5.0 V; T _A = 25; X _{TIN} = V _{DD} , X _{TOUT} = 0 V | 1230 | 2630 | 4000 | |

Table 15-2. D.C. Electrical Characteristics (Concluded)

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

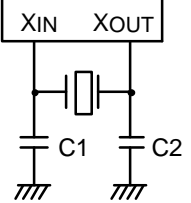
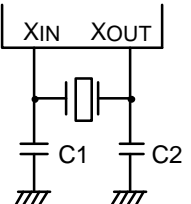
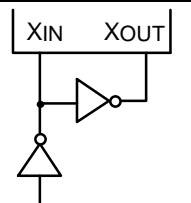
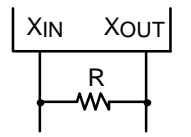
| Parameter | Symbol | Conditions | Min | Typ | Max | Units | |
|---------------------------------|--|--|--|---------|-----|-------|----|
| Supply Current ⁽¹⁾ | I _{DD1} | Main operating: FC enable PCON = 0011B, SCMOD = 0000B Crystal oscillator C1 = C2 = 22 pF V _{DD} = 5 V ± 10% | 4.19 MHz | – | 5.2 | 10 | mA |
| | | I _{DD2} ⁽²⁾ | Main operating: PCON = 0011B, SCMOD = 0000B Crystal oscillator C1 = C2 = 22 pF V _{DD} = 5 V ± 10% | 6.0 MHz | – | 3.5 | |
| | 4.19 MHz | | | 2.5 | | 5.5 | |
| | V _{DD} = 3 V ± 10% | | 6.0 MHz | 1.6 | 4 | | |
| | | | 4.19 MHz | 1.2 | 3 | | |
| | I _{DD3} ⁽²⁾ | Main idle mode ⁽³⁾ : PCON = 0111B, SCMOD = 0000B Crystal oscillator C1 = C2 = 22 pF V _{DD} = 5 V ± 10% | 6.0 MHz | – | 1.0 | 2.5 | |
| | | | 4.19 MHz | | 0.9 | 2.0 | |
| | | V _{DD} = 3 V ± 10% | 6.0 MHz | 0.5 | 1.0 | | |
| | | | 4.19 MHz | 0.4 | 0.8 | | |
| | I _{DD4} ⁽²⁾ | Sub operating mode: PCON = 0011B, SCMOD = 1001B V _{DD} = 3 V ± 10% 32 kHz crystal oscillator | – | 15 | 30 | uA | |
| | I _{DD5} ⁽²⁾ | Sub idle mode: PCON = 0111B, SCMOD = 1001B V _{DD} = 3 V ± 10% 32 kHz crystal oscillator | – | 6 | 15 | | |
| | I _{DD6} ⁽²⁾ | Stop mode: CPU = fxt/4, SCMOD = 1101B V _{DD} = 5 V ± 10% | – | 0.5 | 3 | | |
| I _{DD7} ⁽²⁾ | Stop mode: CPU = fx/4, SCMOD = 0100B V _{DD} = 5 V ± 10% | – | | | | | |

NOTES:

- Supply current does not include current drawn through internal pull-up resistors and LCD voltage dividing resistors.
- AMF or FMF is a normal input mode.
- Data includes the power consumption for sub-system clock oscillation.

Table 15-3. Main System Clock Oscillator Characteristics

(T_A = -40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

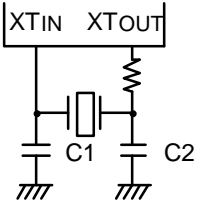
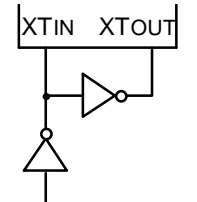
| Oscillator | Clock Configuration | Parameter | Test Condition | Min | Typ | Max | Units |
|--------------------|---|---|---|------|-----------------|-----|-------|
| Ceramic Oscillator |  | Oscillation frequency (1) | – | 0.4 | – | 6.0 | MHz |
| | | Stabilization time (2) | Stabilization occurs when V _{DD} is equal to the minimum oscillator voltage range. | – | – | 4 | ms |
| Crystal Oscillator |  | Oscillation frequency (1) | – | 0.4 | – | 6.0 | MHz |
| | | Stabilization time (2) | V _{DD} = 2.7 V to 5.5 V | – | – | 10 | ms |
| | | | V _{DD} = 1.8 V to 2.7 V | – | – | 30 | |
| External Clock |  | X _{IN} input frequency (1) | – | 0.4 | – | 6.0 | MHz |
| | | X _{IN} input high and low level width (t _{XH} , t _{XL}) | – | 83.3 | – | – | ns |
| RC Oscillator |  | Frequency (1) | V _{DD} = 5 V R = 15 KΩ, V _{DD} = 5 V R = 25 KΩ, V _{DD} = 3 V | 0.4 | – 2.0 1.0 | 2.5 | MHz |

NOTES:

- Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
- Stabilization time is the interval required for oscillator stabilization after a power-on occurs, or when stop mode is terminated.

Table 15-4. Subsystem Clock Oscillator Characteristics

($T_A = -40\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C}$, $V_{DD} = 1.8\text{ V to } 5.5\text{ V}$)

| Oscillator | Clock Configuration | Parameter | Test Condition | Min | Typ | Max | Units |
|--------------------|---|--|--|-----|--------|-----|---------------|
| Crystal Oscillator |  | Oscillation frequency (1) | – | 32 | 32.768 | 35 | kHz |
| | | Stabilization time (2) | $V_{DD} = 2.7\text{ V to } 5.5\text{ V}$ | – | 1.0 | 2 | s |
| | | | $V_{DD} = 1.8\text{ V to } 2.7\text{ V}$ | – | – | 10 | |
| External Clock |  | XT_{IN} input frequency (1) | – | 32 | – | 100 | kHz |
| | | XT_{IN} input high and low level width (t_{XTL} , t_{XTH}) | – | 5 | – | 15 | μs |

NOTES:

- Oscillation frequency and XT_{IN} input frequency data are for oscillator characteristics only.
- Stabilization time is the interval required for oscillator stabilization after a power-on occurs.

Table 15-5. Input/Output Capacitance

 $(T_A = 25\text{ }^\circ\text{C}, V_{DD} = 0\text{ V})$

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|--------------------|-----------|---|-----|-----|-----|-------|
| Input capacitance | C_{IN} | $f_{CLK} = 1\text{ MHz}$; Unmeasured pins are returned to V_{SS} | – | – | 15 | pF |
| Output capacitance | C_{OUT} | | – | – | 15 | pF |
| I/O capacitance | C_{IO} | | – | – | 15 | pF |

Table 15-6. A.C. Electrical Characteristics

 $(T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}, V_{DD} = 1.8\text{ V to } 5.5\text{ V})$

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------------------|----------------------|--|------|-----|-----|---------------|
| Instruction cycle time (1) | t_{CY} | $V_{DD} = 2.7\text{ V to } 5.5\text{ V}$ | 0.67 | – | 64 | μs |
| | | $V_{DD} = 1.8\text{ V to } 5.5\text{ V}$ | 1.3 | | 64 | |
| Interrupt input high, low width | t_{INTH}, t_{INTL} | INT0 | (2) | – | – | μs |
| | | INT1, INT2, INT4, KS0–KS2 | 10 | | | |
| RESET Input Low Width | t_{RSL} | Input | 10 | – | – | μs |

NOTES:

1. Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock/4 (fx/4) source.
2. Minimum value for INT0 is based on a clock of $2t_{CY}$ or $128/f_{xx}$ as assigned by the IMOD0 register setting.

Table 15-6. A.C. Electrical Characteristics (continued)

 $(T_A = -10\text{ }^\circ\text{C to } +70\text{ }^\circ\text{C}, V_{DD} = 3.5\text{ V to } 5.5\text{ V})$

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------------|-----------|------------|----------|--------------------|----------|------------------|
| A/D converting Resolution | – | – | 8 | 8 | 8 | bits |
| Absolute accuracy | – | – | – | – | ± 2 | LSB |
| AD conversion time | t_{CON} | – | 17 | $34/f_{xx}$ (note) | – | μs |
| Analog input voltage | V_{IAN} | – | V_{SS} | – | V_{DD} | V |
| Analog input impedance | R_{AN} | – | 2 | 1000 | – | $\text{M}\Omega$ |

NOTE: fxx stands for the system clock (fx or fxt).

Table 15-6. A.C. Electrical Characteristics (continued)

($T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ to 5.5 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|------------------------------|-----------|--|-----|-----|----------|-------|
| Input voltage (peak to peak) | V_{IN} | AMF/FMF mode, sine wave input | 0.3 | – | V_{DD} | V |
| Frequency | f_{AMF} | AMF mode, sine wave input; $V_{IN} = 300\text{mV}_{P-P}$ | 0.5 | – | 10 | MHz |
| | f_{FMF} | FMF mode, sine wave input; $V_{IN} = 300\text{mV}_{P-P}$ | 30 | | 150 | |

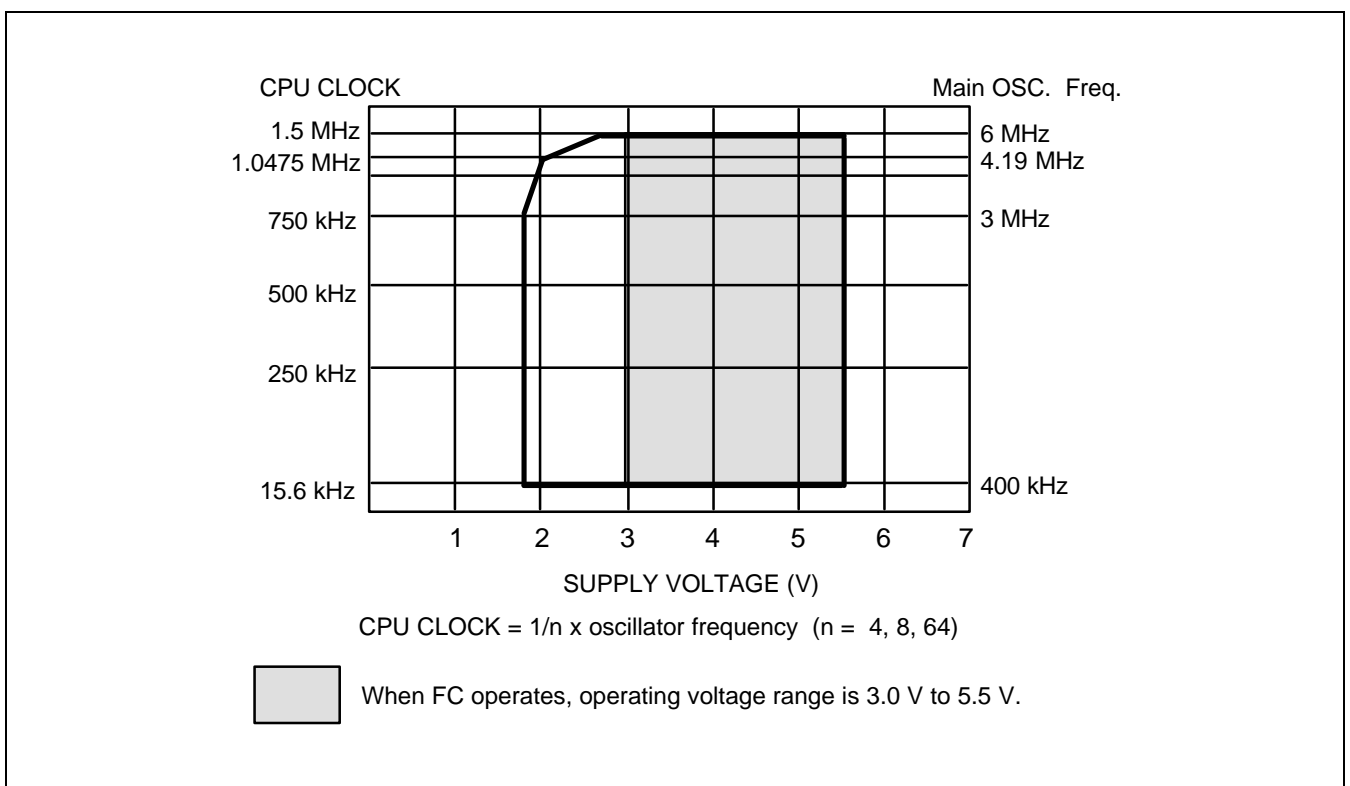


Figure 15-1. Standard Operating Voltage Range

Table 15-7. RAM Data Retention Supply Voltage in Stop Mode

($T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------|------------|---------------------------|-----|-----|-----|---------------|
| Data retention supply voltage | V_{DDDR} | Normal operation | 1.8 | – | 5.5 | V |
| Data retention supply current | I_{DDDR} | $V_{DDDR} = 1.8\text{ V}$ | – | 0.1 | 1 | μA |

TIMING WAVEFORMS

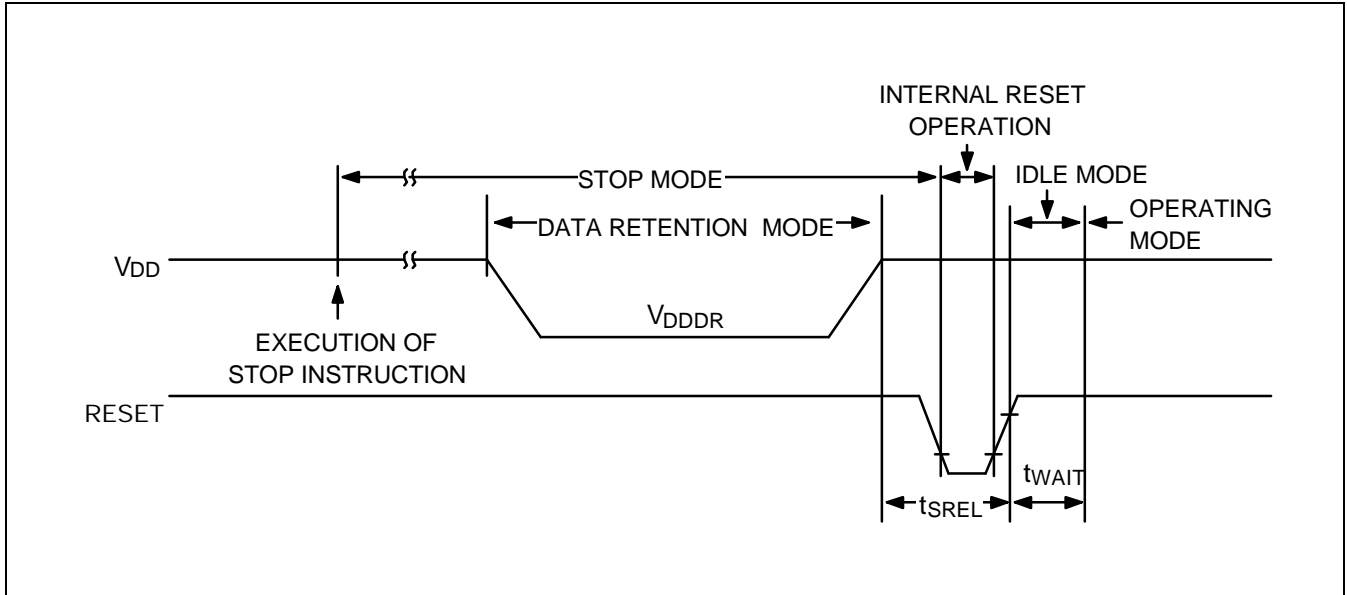


Figure 15-2. Stop Mode Release Timing When Initiated by RESET

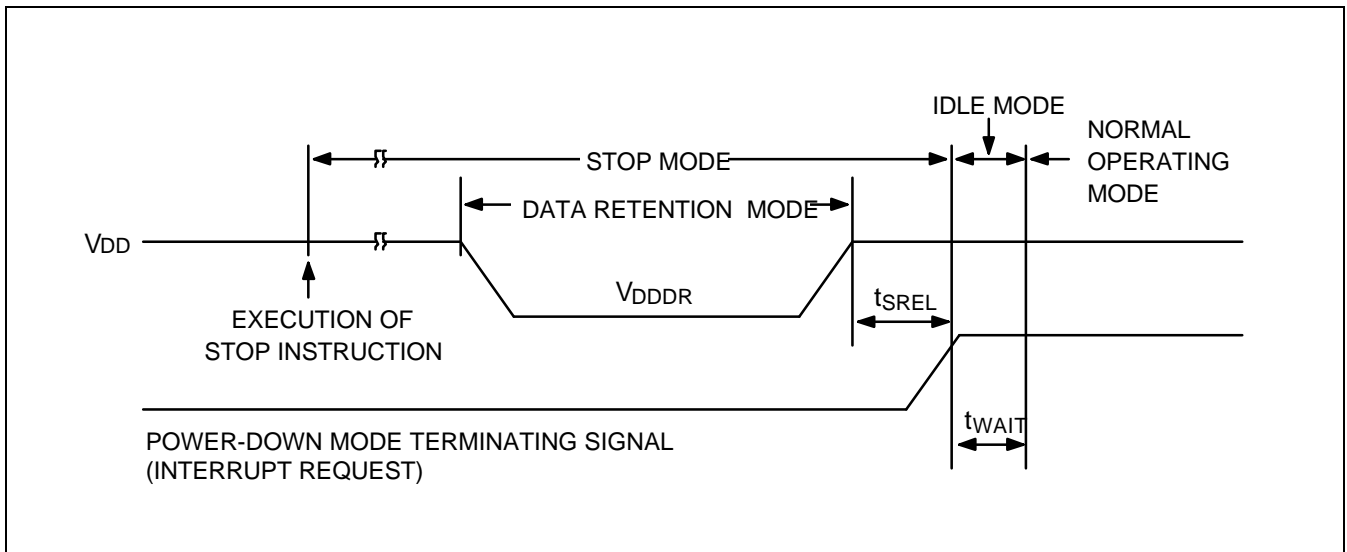


Figure 15-3. Stop Mode Release Timing When Initiated by an Interrupt Request

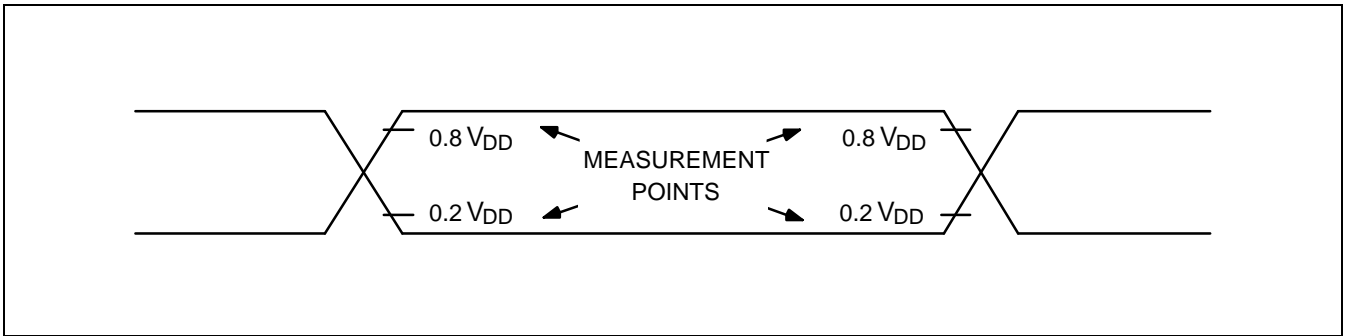


Figure 15-4. A.C. Timing Measurement Points (Except for X_{in} and XT_{in})

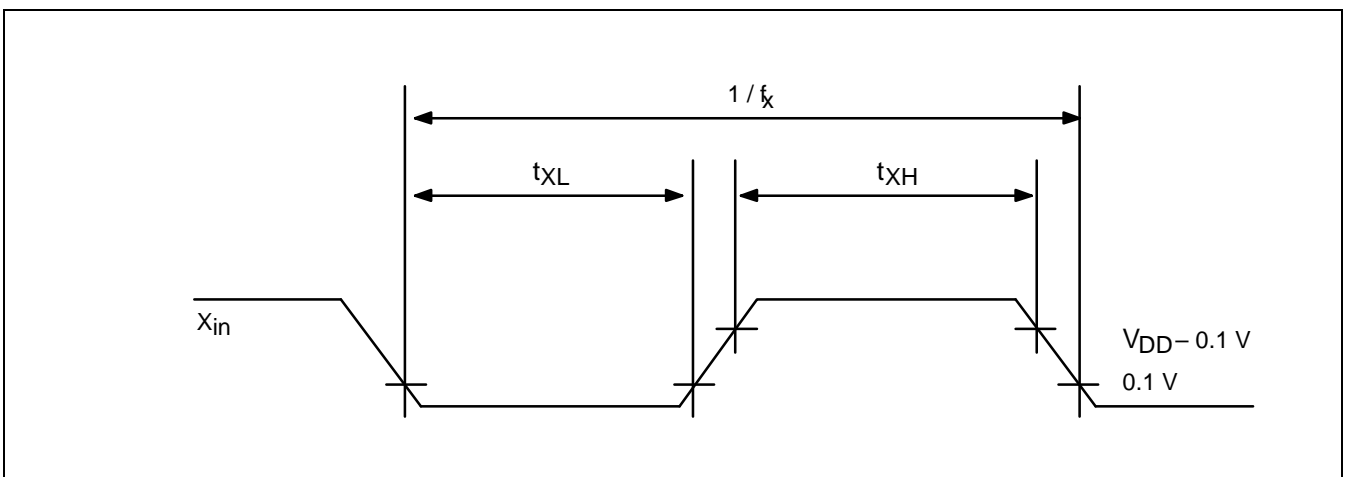


Figure 15-5. Clock Timing Measurement at X_{in}

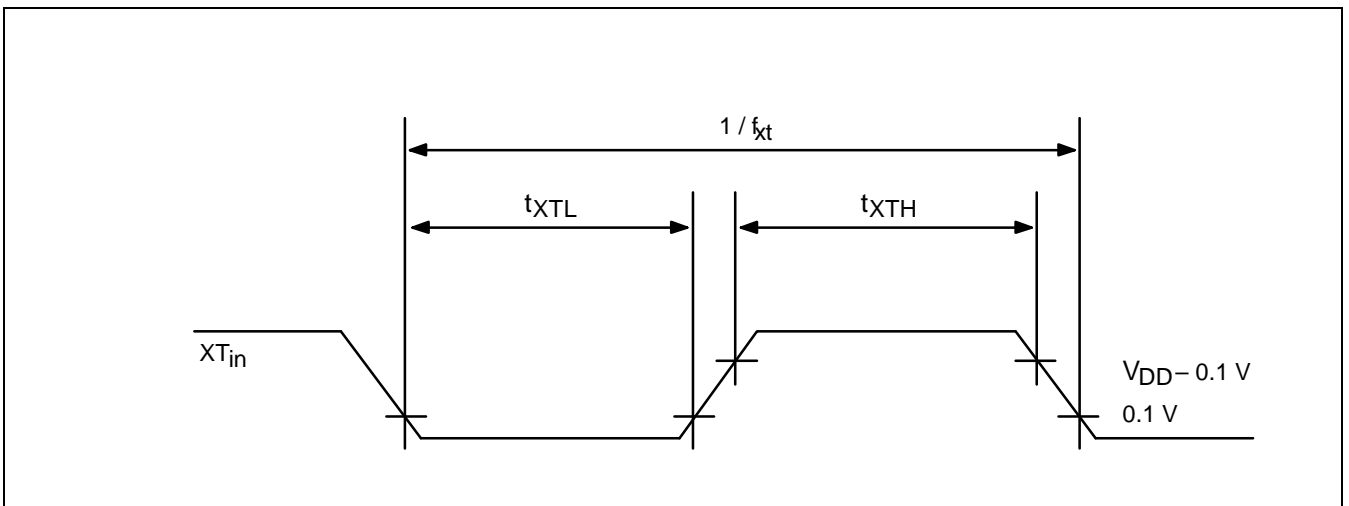


Figure 15-6. Clock Timing Measurement at XT_{in}

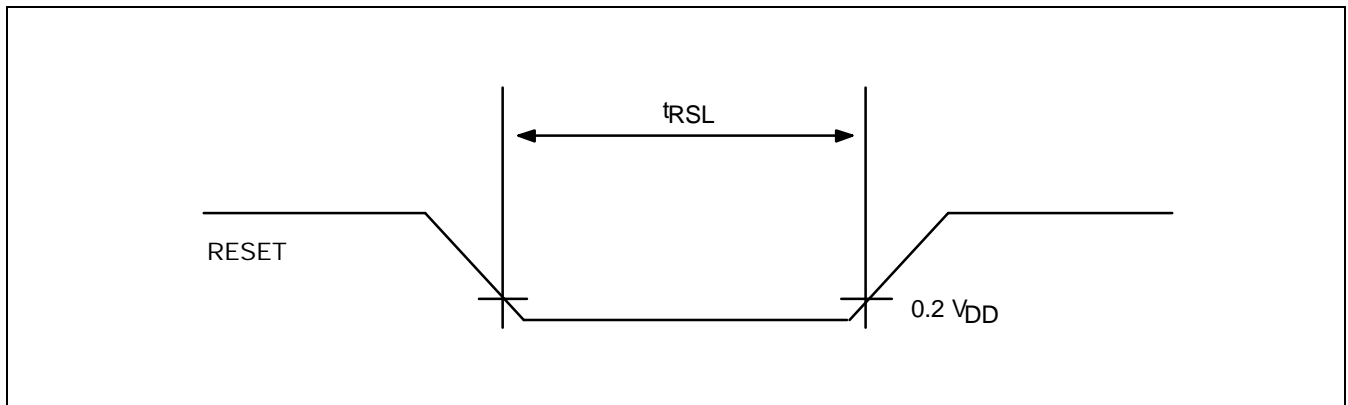


Figure 15-7. Input Timing for RESET Signal

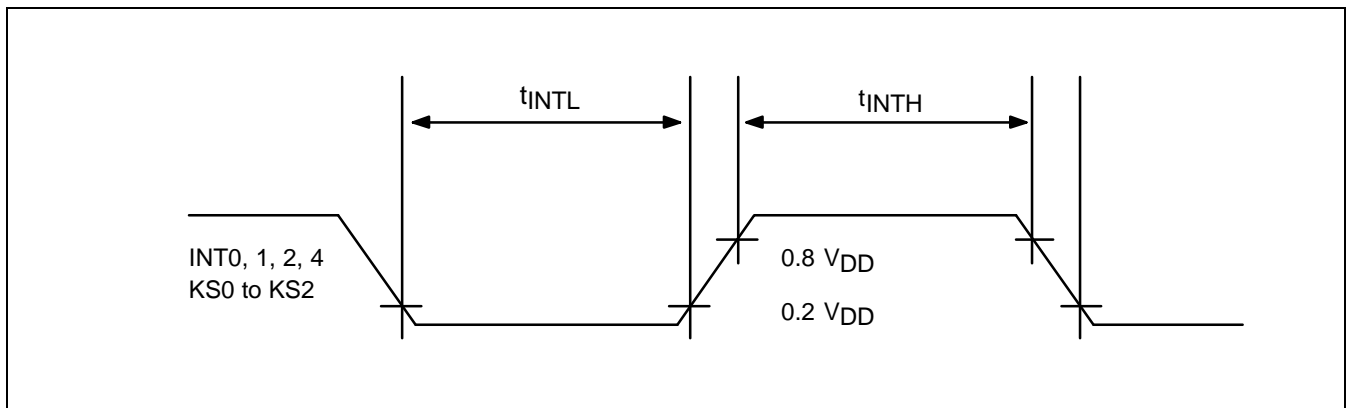


Figure 15-8. Input Timing for External Interrupts and Quasi-Interrupts

16

MECHANICAL DATA

OVERVIEW

The S3C7324 microcontroller is available in a 64-pin QFP package (Samsung: 64-QFP-1420F). Package dimensions are shown in Figure 16-1.

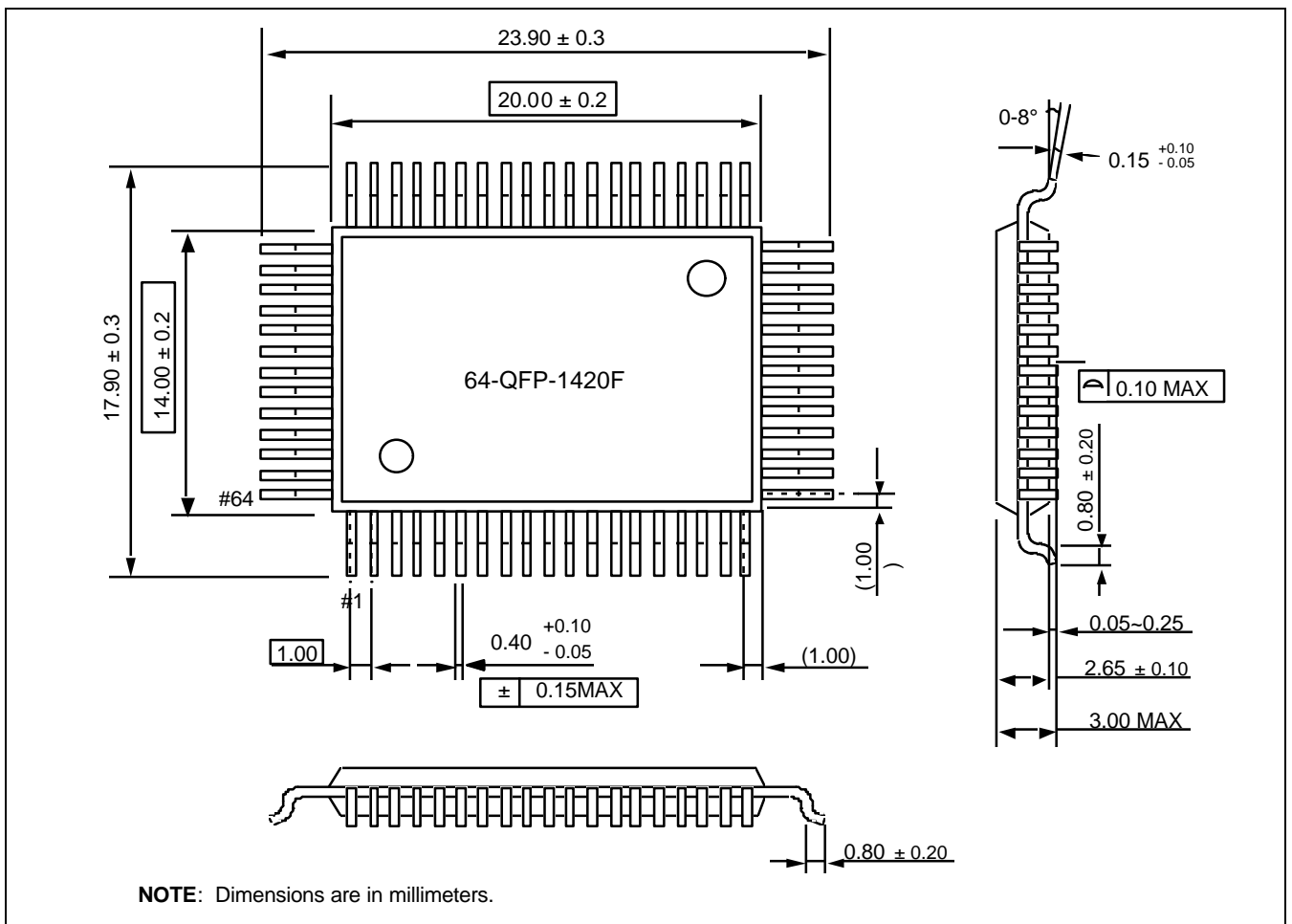


Figure 16-1. 64-QFP-1420F Package Dimensions

17

S3P7324 OTP

OVERVIEW

The S3P7324 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C7324 microcontroller. It has an on-chip EPROM instead of masked ROM. The EPROM is accessed by a serial data format.

The S3P7324 is fully compatible with the S3C7324, both in function and in pin configuration. Because of its simple programming requirements, the S3P7324 is ideal for use as an evaluation chip for the S3C7324.

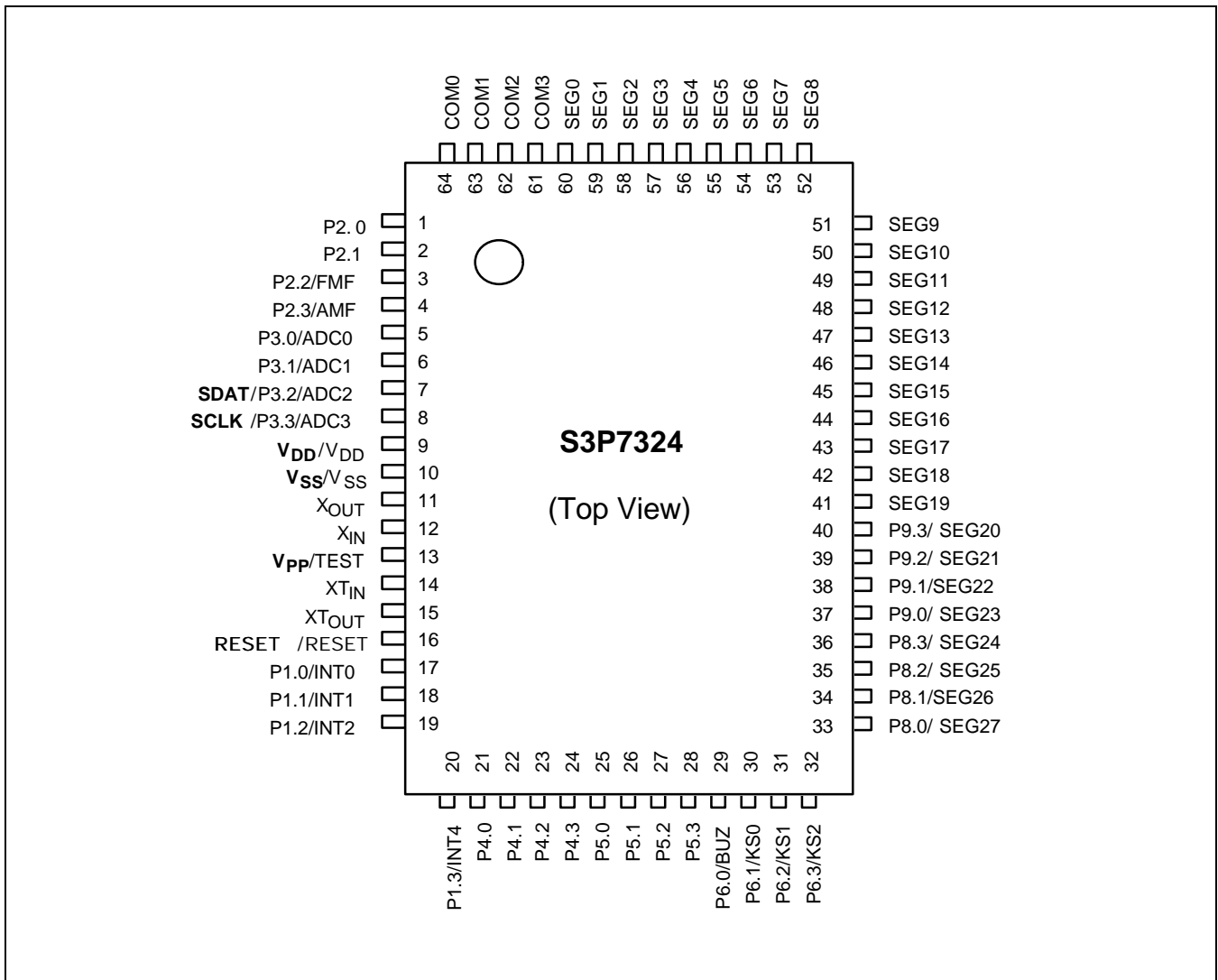


Figure 17-1. S3P7324 Pin Assignments (64-QFP)

Table 17-1. Pin Descriptions Used to Read/Write the EPROM

| Main Chip | During Programming | | | |
|----------------------------------|----------------------------------|---------|-----|--|
| Pin Name | Pin Name | Pin No. | I/O | Function |
| P3.2 | SDAT | 7 | I/O | Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input or push-pull output port. |
| P3.3 | SCLK | 8 | I/O | Serial clock pin. Input only pin. |
| TEST | V _{PP} (TEST) | 13 | I | Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. |
| RESET | RESET | 16 | I | Chip initialization |
| V _{DD} /V _{SS} | V _{DD} /V _{SS} | 9/10 | I | Logic power supply pin. V _{DD} should be tied to +5 V during programming. |

Table 17-2. Comparison of S3P7324 and S3C7324 Features

| Characteristic | S3P7324 | S3C7324 |
|--------------------------------------|--|---|
| Program Memory | 4K bytes EPROM | 4K bytes mask ROM |
| Operating Voltage (V _{DD}) | 2.0 V to 5.5 V at 4.19 MHz 1.8 V to 5.5 V at 3 MHz | 2.0 V to 5.5 V at 4.19 MHz 1.8 V to 5.5 V at 3 MHz |
| OTP Programming Mode | V _{DD} = 5 V, V _{PP} (TEST) = 12.5 V | – |
| Pin Configuration | 64 QFP | 64 QFP |
| EPROM Programmability | User Program 1 time | Programmed at the factory |

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (TEST) pin of the S3P7324, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 17-3 below.

Table 17-3. Operating Mode Selection Criteria

| V _{DD} | V _{PP} (TEST) | REG/MEM | Address (A15-A0) | R/W | Mode |
|-----------------|------------------------|---------|------------------|-----|-----------------------|
| 5 V | 5 V | 0 | 0000H | 1 | EPROM read |
| | 12.5 V | 0 | 0000H | 0 | EPROM program |
| | 12.5 V | 0 | 0000H | 1 | EPROM verify |
| | 12.5 V | 1 | 0E3FH | 0 | EPROM read protection |

NOTE: "0" means low level; "1" means high level.

Table 17-4. D.C. Electrical Characteristics

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------|------------------|---|-----------------------|-----|---------------------|-------|
| Input high voltage | V _{IH1} | All input pins except those specified below | 0.7 V _{DD} | - | V _{DD} | V |
| | V _{IH2} | P1, P3, RESET, P2.0-1 and P6.1-3 | 0.8 V _{DD} | | V _{DD} | |
| | V _{IH3} | X _{IN} , X _{OUT} , XT _{IN} , and XT _{OUT} | V _{DD} - 0.1 | | V _{DD} | |
| Input low voltage | V _{IL1} | All input pins except those specified below | - | - | 0.3 V _{DD} | V |
| | V _{IL2} | P1, P3, RESET, P2.0-1 and P6.1-3 | | | 0.2 V _{DD} | |
| | V _{IL3} | X _{IN} , X _{OUT} , XT _{IN} , and XT _{OUT} | | | 0.1 | |
| Output high voltage | V _{OH1} | V _{DD} = 4.5 V to 5.5 V I _{OH} = -1 mA Ports 1, 4, 5, and 6 | V _{DD} - 1.0 | - | - | V |
| | V _{OH2} | V _{DD} = 4.5 V to 5.5 V I _{OH} = -100 μA Port 8 and 9 | V _{DD} - 2.0 | | | |

Table 17-4. D.C. Electrical Characteristics (Continued)

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|-------------------|---|-----|-----|-----|-------|
| Output low voltage | V _{OL1} | V _{DD} = 4.5 V to 5.5 V I _{OL} = 15 mA, Ports 1, 4, 5, and 6 | - | 0.4 | 2 | V |
| | V _{OL2} | V _{DD} = 4.5 V to 5.5 V I _{OL} = 100 μA ; Ports 8 and 9 | - | - | 1 | |
| Input high leakage current ^(note) | I _{LIH1} | V _{IN} = V _{DD} All input pins | - | - | 3 | μA |
| Input low leakage current ^(note) | I _{LIL1} | V _{IN} = 0 V All input pins | - | - | -3 | |
| Output high leakage current ^(note) | I _{LOH1} | V _{OUT} = V _{DD} All output pins | - | - | 3 | |
| Output low leakage current ^(note) | I _{LOL} | V _{OUT} = 0 V All output pins | - | - | -3 | |
| Pull-up resistor | R _{L1} | V _{IN} = 0 V; V _{DD} = 5 V Ports 1, 2, 3, 4, 5, and 6 | 20 | 40 | 80 | KΩ |
| | | V _{DD} = 3 V | 30 | 95 | 200 | |
| | R _{L2} | V _{IN} = 0 V; V _{DD} = 5 V RESET | 100 | 230 | 400 | |
| | | V _{DD} = 3 V | 200 | 480 | 800 | |

NOTE: Except for X_{IN}, X_{OUT}, XT_{IN}, and XT_{OUT}

Table 17-4. D.C. Electrical Characteristics (Continued)

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|-------------------------------|-------------------|---|------|------|------|-------|
| LCD voltage dividing resistor | R _{LCD} | T _A = 25 °C | 60 | 84 | 130 | KΩ |
| COM output impedance | R _{COM} | V _{DD} = 5 V | - | 3 | 6 | |
| | | V _{DD} = 3 V | | 5 | 15 | |
| SEG output impedance | R _{SEG} | V _{DD} = 5 V | - | 3 | 6 | |
| | | V _{DD} = 3 V | | 5 | 15 | |
| COM output voltage deviation | V _{DC} | V _{DD} = 5 V (V _{LCO} -COMi) I _o = ± 15μA (I = 0-3) | - | ± 45 | ± 90 | mV |
| SEG output voltage deviation | V _{DS} | V _{DD} = 5 V (V _{LCO} -SEGi) I _o = ± 15μA (I = 0-27) | - | ± 45 | ± 90 | |
| Oscillator feedback resistor | R _{OSC1} | V _{DD} = 5.0 V; T _A = 25; X _{IN} = V _{DD} , X _{OUT} = 0 V | 300 | 600 | 1500 | KΩ |
| | R _{OSC2} | V _{DD} = 5.0 V; T _A = 25; X _{TIN} = V _{DD} , X _{TOUT} = 0 V | 1230 | 2630 | 4000 | |

Table 17-4. D.C. Electrical Characteristics (Concluded)

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

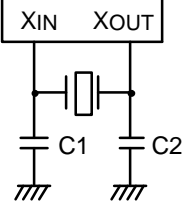
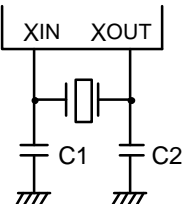
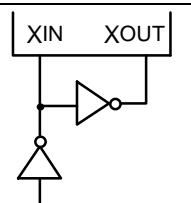
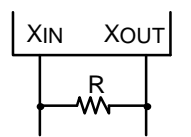
| Parameter | Symbol | Conditions | Min | Typ | Max | Units | |
|---------------------------------|---|--|--|---------|-----|-------|----|
| Supply Current ⁽¹⁾ | I _{DD1} | Main operating: FC enable PCON = 0011B, SCMOD = 0000B Crystal oscillator C1 = C2 = 22 pF V _{DD} = 5 V ± 10% | 4.19 MHz | – | 5.2 | 10 | mA |
| | | I _{DD2} ⁽²⁾ | Main operating: PCON = 0011B, SCMOD = 0000B Crystal oscillator C1 = C2 = 22 pF V _{DD} = 5 V ± 10% | 6.0 MHz | – | 3.5 | |
| | 4.19 MHz | | | 2.5 | | 5.5 | |
| | V _{DD} = 3 V ± 10% | | 6.0 MHz | 1.6 | 4 | | |
| | | | 4.19 MHz | 1.2 | 3 | | |
| | I _{DD3} ⁽²⁾ | Main idle mode ⁽³⁾ : PCON = 0111B, SCMOD = 0000B Crystal oscillator C1 = C2 = 22 pF V _{DD} = 5 V ± 10% | 6.0 MHz | – | 1.0 | 2.5 | |
| | | | 4.19 MHz | | 0.9 | 2.0 | |
| | | V _{DD} = 3 V ± 10% | 6.0 MHz | 0.5 | 1.0 | | |
| | | | 4.19 MHz | 0.4 | 0.8 | | |
| | I _{DD4} ⁽²⁾ | Sub operating mode: PCON = 0011B, SCMOD = 1001B V _{DD} = 3 V ± 10% 32 kHz crystal oscillator | | – | 15 | 30 | |
| I _{DD5} ⁽²⁾ | Sub idle mode: PCON = 0111B, SCMOD = 1001B V _{DD} = 3 V ± 10% 32 kHz crystal oscillator | | – | 6 | 15 | | |
| I _{DD6} ⁽²⁾ | Stop mode: CPU = fxt/4, SCMOD = 1101B V _{DD} = 5 V ± 10% | | – | 0.5 | 3 | | |
| I _{DD7} ⁽²⁾ | Stop mode: CPU = fx/4, SCMOD = 0100B V _{DD} = 5 V ± 10% | | – | | | | |

NOTES:

- Supply current does not include current drawn through internal pull-up resistors and LCD voltage dividing resistors.
- AMF or FMF is a normal input mode.
- Data includes the power consumption for sub-system clock oscillation.

Table 17-5. Main System Clock Oscillator Characteristics

(T_A = -40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

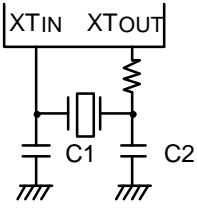
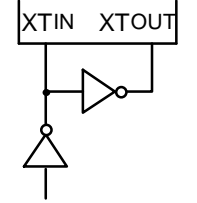
| Oscillator | Clock Configuration | Parameter | Test Condition | Min | Typ | Max | Units |
|--------------------|---|---|---|------|-----------------|-----|-------|
| Ceramic Oscillator |  | Oscillation frequency (1) | – | 0.4 | – | 6.0 | MHz |
| | | Stabilization time (2) | Stabilization occurs when V _{DD} is equal to the minimum oscillator voltage range. | – | – | 4 | ms |
| Crystal Oscillator |  | Oscillation frequency (1) | – | 0.4 | – | 6.0 | MHz |
| | | Stabilization time (2) | V _{DD} = 2.7 V to 5.5 V | – | – | 10 | ms |
| | | | V _{DD} = 1.8 V to 2.7 V | – | – | 30 | |
| External Clock |  | X _{IN} input frequency (1) | – | 0.4 | – | 6.0 | MHz |
| | | X _{IN} input high and low level width (t _{XH} , t _{XL}) | – | 83.3 | – | – | ns |
| RC Oscillator |  | Frequency (1) | V _{DD} = 5 V R = 15 KΩ, V _{DD} = 5 V R = 25 KΩ, V _{DD} = 3 V | 0.4 | – 2.0 1.0 | 2.5 | MHz |

NOTES:

- Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
- Stabilization time is the interval required for oscillator stabilization after a power-on occurs, or when stop mode is terminated.

Table 17-6. Subsystem Clock Oscillator Characteristics

($T_A = -40\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C}$, $V_{DD} = 1.8\text{ V to } 5.5\text{ V}$)

| Oscillator | Clock Configuration | Parameter | Test Condition | Min | Typ | Max | Units |
|--------------------|--|--|--|-----|--------|-----|---------------|
| Crystal Oscillator |  | Oscillation frequency (1) | – | 32 | 32.768 | 35 | kHz |
| | | Stabilization time (2) | $V_{DD} = 2.7\text{ V to } 5.5\text{ V}$ | – | 1.0 | 2 | s |
| | | | $V_{DD} = 1.8\text{ V to } 2.7\text{ V}$ | – | – | 10 | |
| External Clock |  | XT_{IN} input frequency (1) | – | 32 | – | 100 | kHz |
| | | XT_{IN} input high and low level width (t_{XTL} , t_{XTH}) | – | 5 | – | 15 | μs |

NOTES:

- Oscillation frequency and XT_{IN} input frequency data are for oscillator characteristics only.
- Stabilization time is the interval required for oscillator stabilization after a power-on occurs.

Table 17-7. Input/Output Capacitance

 $(T_A = 25\text{ }^\circ\text{C}, V_{DD} = 0\text{ V})$

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|--------------------|-----------|---|-----|-----|-----|-------|
| Input capacitance | C_{IN} | $f_{CLK} = 1\text{ MHz}$; Unmeasured pins are returned to V_{SS} | – | – | 15 | pF |
| Output capacitance | C_{OUT} | | – | – | 15 | pF |
| I/O capacitance | C_{IO} | | – | – | 15 | pF |

Table 17-8. A.C. Electrical Characteristics

 $(T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------------------|----------------------|---|------|-----|-----|---------------|
| Instruction cycle time (1) | t_{CY} | $V_{DD} = 2.7\text{ V}$ to 5.5 V | 0.67 | – | 64 | μs |
| | | $V_{DD} = 1.8\text{ V}$ to 5.5 V | 1.3 | | 64 | |
| Interrupt input high, low width | t_{INTH}, t_{INTL} | INT0 | (2) | – | – | μs |
| | | INT1, INT2, INT4, KS0–KS2 | 10 | | | |
| RESET Input Low Width | t_{RSL} | Input | 10 | – | – | μs |

NOTES:

- Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock/4 (fx/4) source.
- Minimum value for INT0 is based on a clock of $2t_{CY}$ or $128/f_{xx}$ as assigned by the IMOD0 register setting.

Table 17-8. A.C. Electrical Characteristics (continued)

 $(T_A = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$, $V_{DD} = 3.5\text{ V}$ to 5.5 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------------|-----------|------------|----------|--------------------|----------|---------------|
| A/D converting Resolution | – | – | 8 | 8 | 8 | bits |
| Absolute accuracy | – | – | – | – | ± 2 | LSB |
| AD conversion time | t_{CON} | – | 17 | $34/f_{xx}$ (note) | – | μs |
| Analog input voltage | V_{IAN} | – | V_{SS} | – | V_{DD} | V |
| Analog input impedance | R_{AN} | – | 2 | 1000 | – | $M\Omega$ |

NOTE: fxx stands for the system clock (fx or fxt).

Table 17-8. A.C. Electrical Characteristics (continued)

($T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ to 5.5 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|------------------------------|-----------|--|-----|-----|----------|-------|
| Input voltage (peak to peak) | V_{IN} | AMF/FMF mode, sine wave input | 0.3 | – | V_{DD} | V |
| Frequency | f_{AMF} | AMF mode, sine wave input; $V_{IN} = 300\text{mV}_{P-P}$ | 0.5 | – | 10 | MHz |
| | f_{FMF} | FMF mode, sine wave input; $V_{IN} = 300\text{mV}_{P-P}$ | 30 | | 150 | |

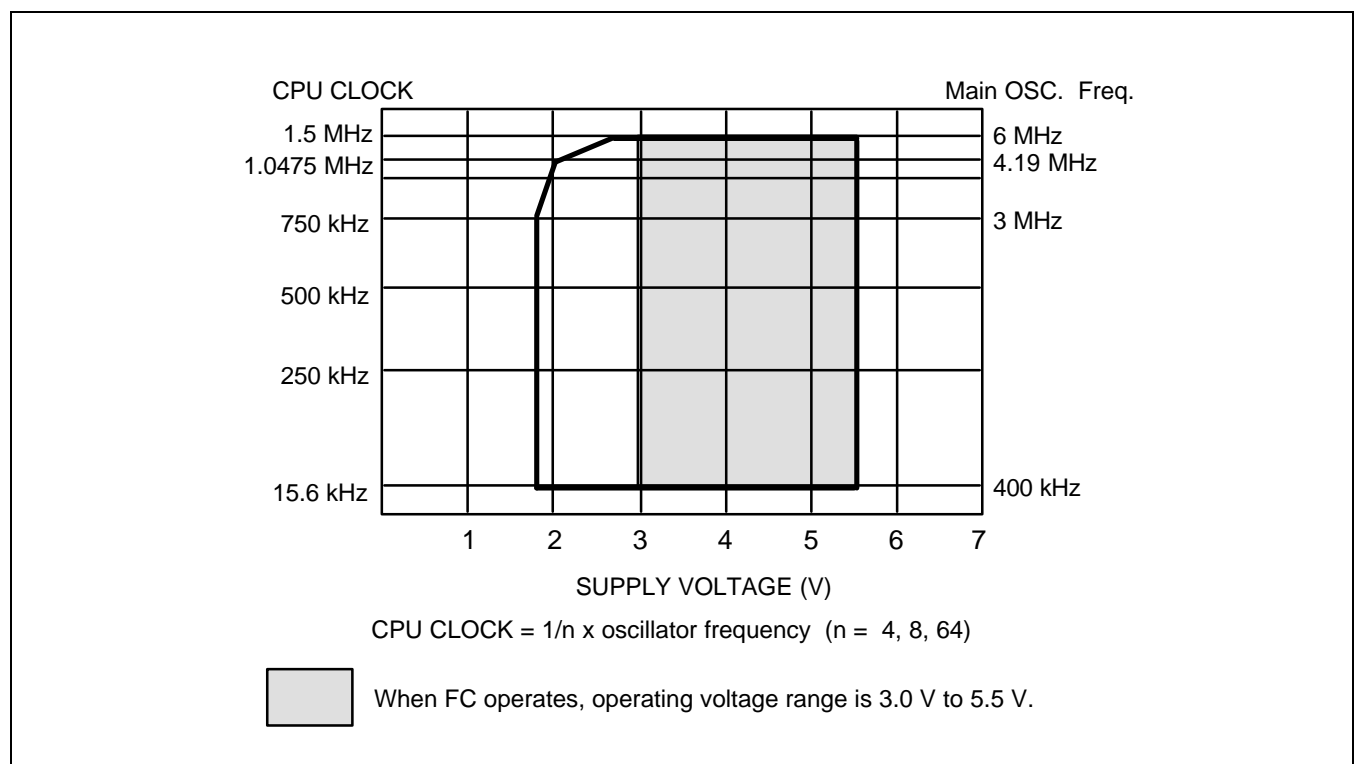


Figure 17-2. Standard Operating Voltage Range

Table 17-9. RAM Data Retention Supply Voltage in Stop Mode

($T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------|------------|---------------------------|-----|-----|-----|---------------|
| Data retention supply voltage | V_{DDDR} | Normal operation | 1.8 | – | 5.5 | V |
| Data retention supply current | I_{DDDR} | $V_{DDDR} = 1.8\text{ V}$ | – | 0.1 | 1 | μA |

TIMING WAVEFORMS

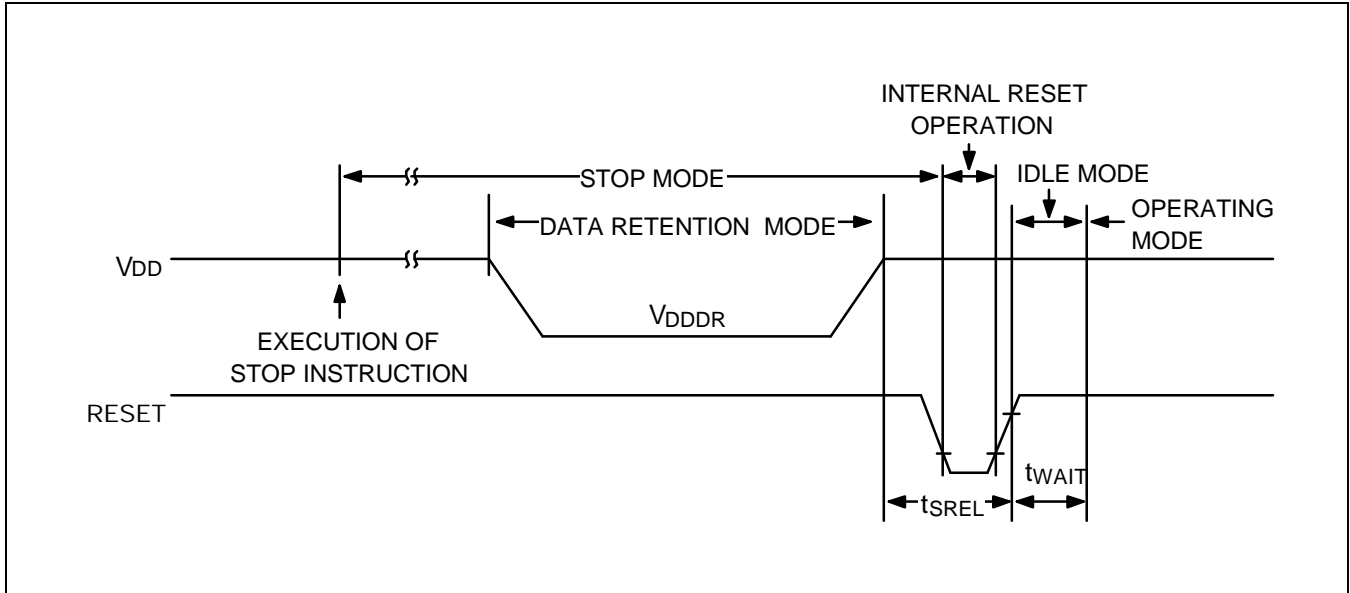


Figure 17-3. Stop Mode Release Timing When Initiated by RESET

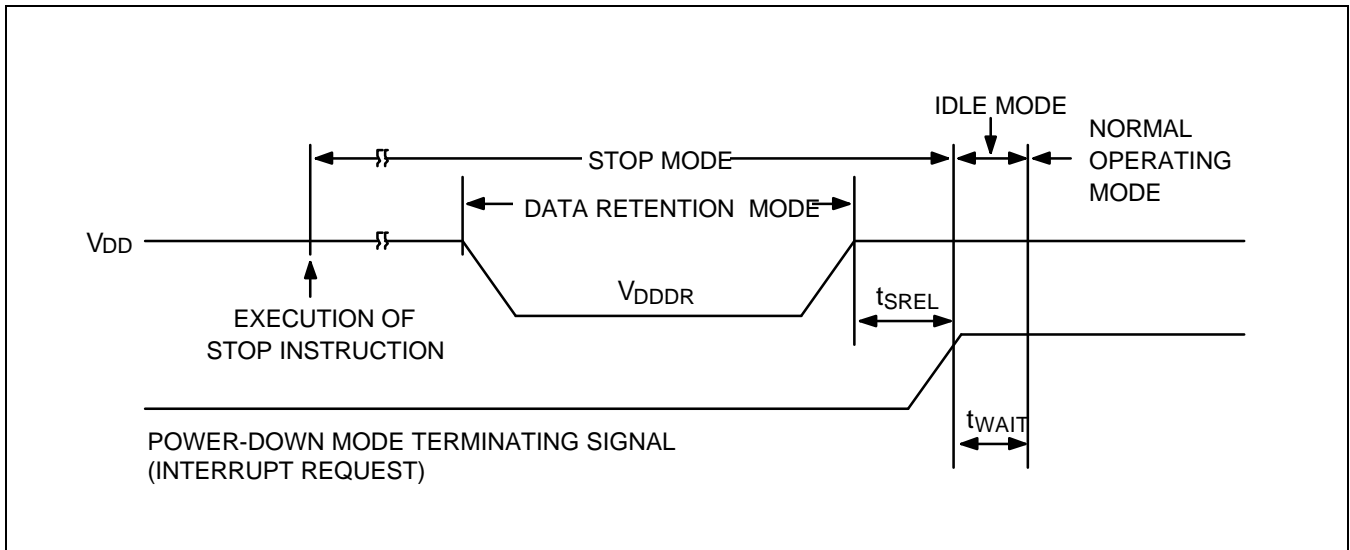


Figure 17-4. Stop Mode Release Timing When Initiated by an Interrupt Request

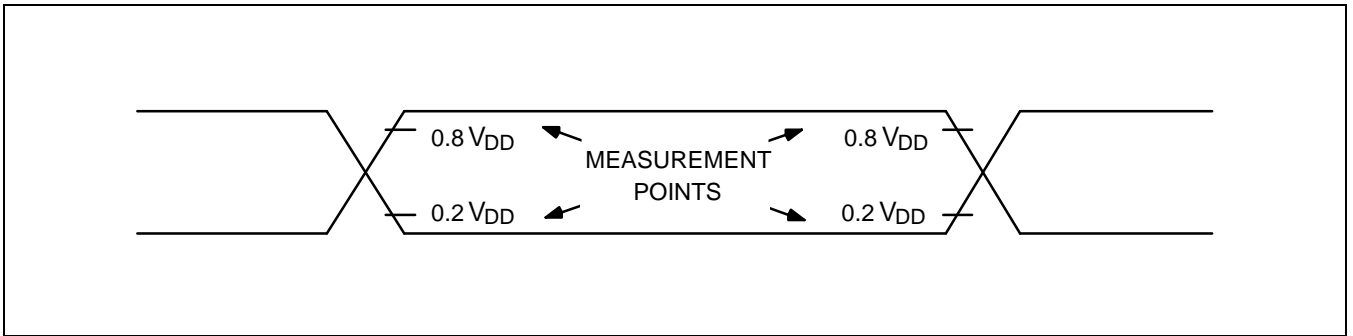


Figure 17-5. A.C. Timing Measurement Points (Except for X_{in} and XT_{in})

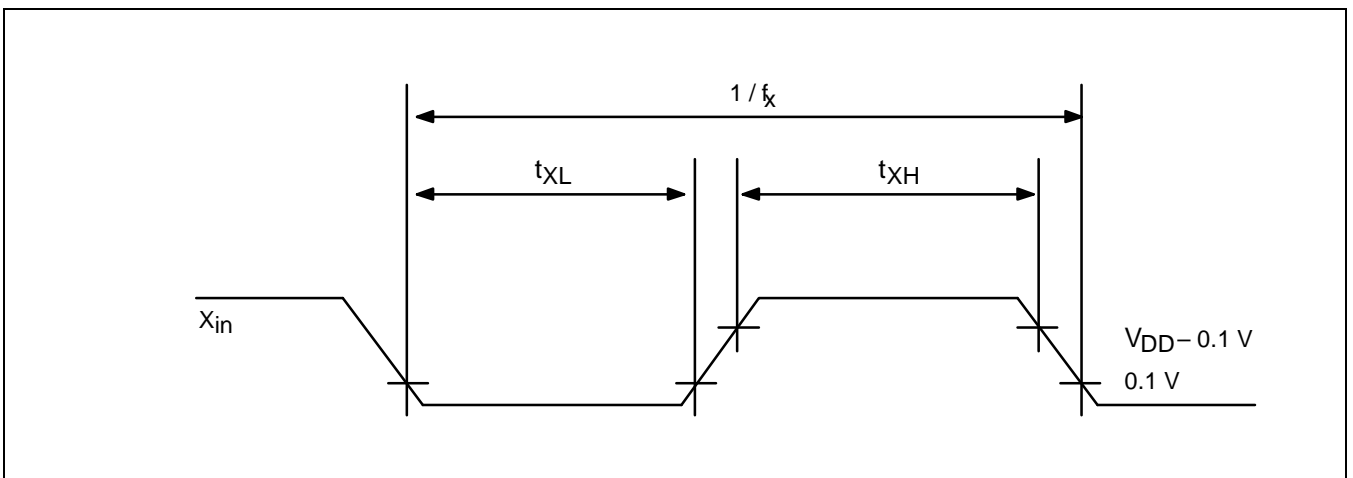


Figure 17-6. Clock Timing Measurement at X_{in}

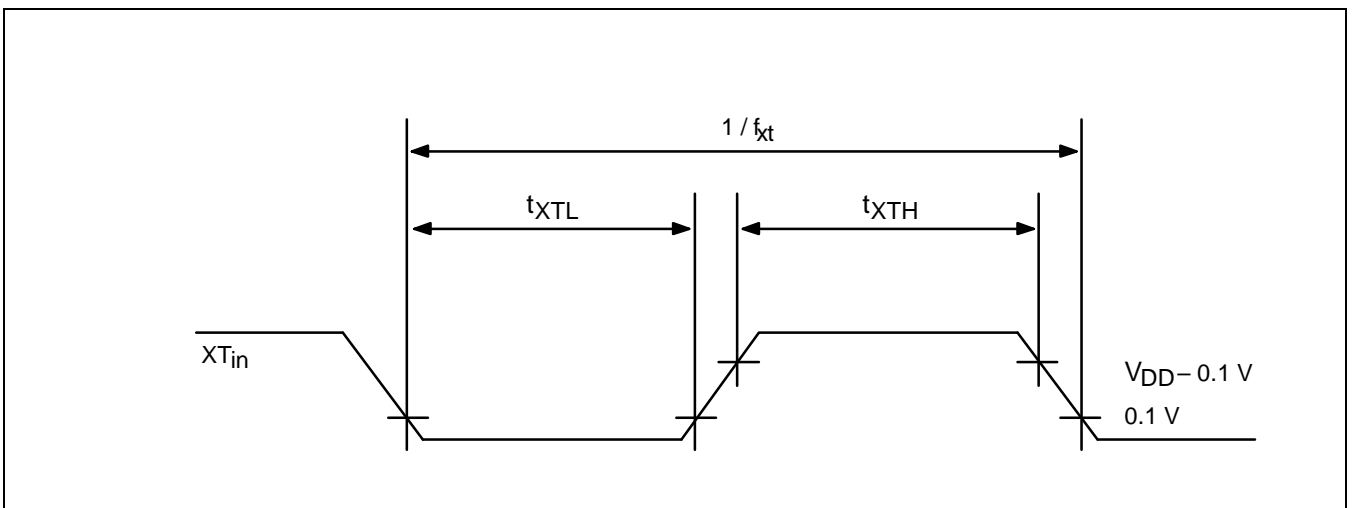


Figure 17-7. Clock Timing Measurement at XT_{in}

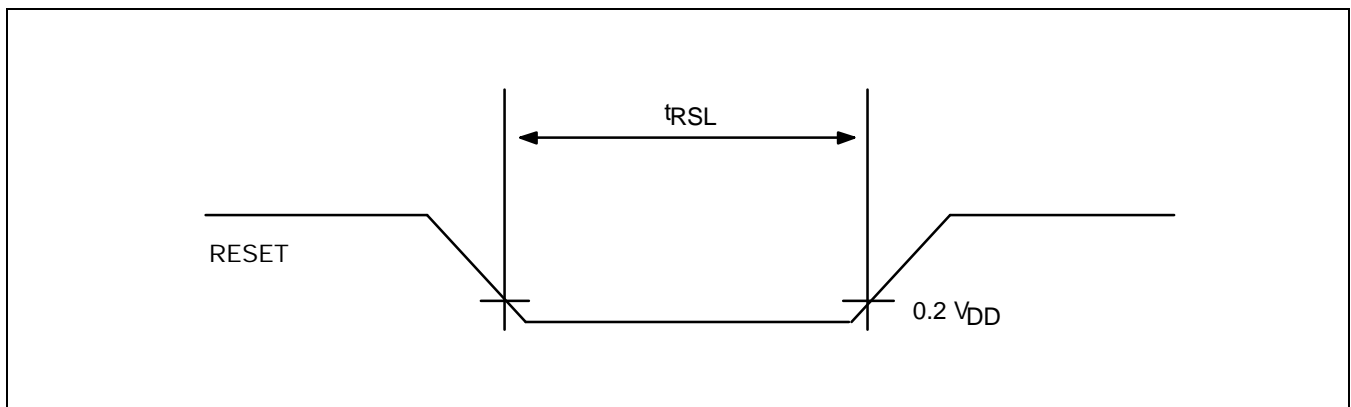


Figure 17-8. Input Timing for RESET Signal

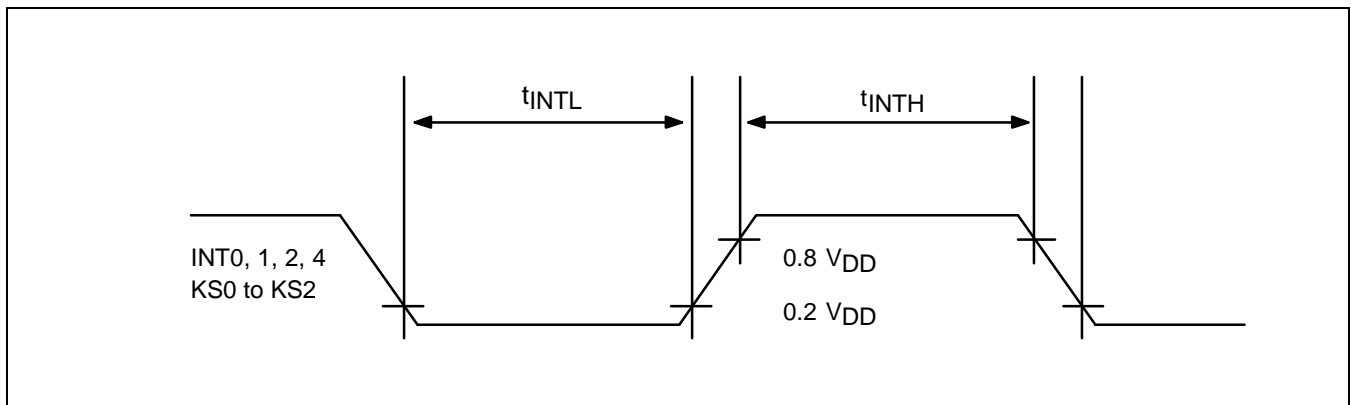


Figure 17-9. Input Timing for External Interrupts and Quasi-Interrupts