

**LVDS UHF CLOCK (XO)
SD-A2D7XXX Series**

Description

The **SD-A2D7XXX Series** of quartz crystal oscillators provides ultra high frequency with LVDS complementary outputs. The outputs can be Tri-stated for test automation or combining multiple clocks. The device is based on PLL multiplication for higher frequencies, and packaged in a miniature, low profile leadless ceramic SMD package with 6 gold plated pads.

Applications and Features

- Wide frequency range – 0.75MHz to 800.000MHz
- Fiber Channel; 10 GbE; Infiniband; Network Processors; SOHO Routing
- High Reliability - NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Low Phase Noise, Low Jitter
- High shock resistance, to 1000g
- Ultra High Frequency
- Tight frequency stability - ± 20 ppm overall available
- Grounded lid and internal by-pass capacitor reduce EMI
- RoHS Compliant, Lead Free Construction

Creating a Part Number

SD - A 2D7 X X X - FREQ

<p><u>Package Code</u> _____ SD 6 pad 5x7mm SMD</p> <p><u>Input Voltage</u> _____ A 3.3V\pm5%</p> <p><u>Enable Option</u> _____ H Enable High L Enable Low N No Enable option</p>	<p><u>Overall Frequency Stability, ppm</u> E ± 20 F ± 25 G ± 50 H ± 100 9 Customer specific</p> <p><u>Temperature Range, °C</u> A 0 to 50 B 0 to 70 C -20 to 70 D -40 to 85 9 Customer specific</p>
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**SD-A2D7XXX Series Continued
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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Operating Temperature Range	To	-40 to +85	°C
Storage Temperature Range	Tst	-50 to +90	°C
Supply Voltage	Vcc	-0.5 to 4.5	V
Enable/Disable Voltage	Ven/dis	0 to Vcc	V

Electrical Parameters

Parameter	Symb	Conditions, Note	MIN	TYP	MAX	Unit
Nominal Frequency	Fo		0.75		800	MHz
Supply Voltage	Vcc	Code A	3.135	3.3	3.465	V
Supply current	Icc			80	100	mA
Output Logic Type				LVDS		
Load		At receiving end between the outputs	90	100	110	Ohm
Output Levels	Vod	Differential amplitude	247	330	454	mV
		Amplitude error			50	mV
	Vof	Offset Voltage	1.125	1.25	1.375	V
		Offset Voltage error			50	mV
Duty Cycle (Symmetry)		At outputs crossing, room temperature	45/55	50/50	55/45	%
Rise/Fall Time	Tr/Tf	20 to 80, 80 to 20 %		0.5	0.7	ns
Jitter	Integrated	J	Integrated from Phase Noise, 12 KHz to 20 MHz, RMS		2.6 @ 155 2.5 @ 622	ps
	Wavecrest characterized	Random period,	155 MHz	4.3		ps
		Accumul., pk-to-pk	155 MHz	27		ps
Phase Noise	£(Δf)	155 MHz	@ 10 Hz		-60	dBc/Hz
			@ 100 Hz		-90	
			@ 1 KHz		-115	
			@ 10KHz		-125	
			@ 100KHz		-119	
			@ 1MHz		-130	
Frequency Stability	ΔF/F	Overall, including initial calibration, temperature, aging 10 years, shock and vibration	See "Creating a Part Number" Not all combinations available, consult factory			ppm
Enable High Option Pin 2 Enabled Pin 2 Disabled		CMOS logic 1 or N/C CMOS logic 0	0.7 Vcc 0		Vcc 0.3 Vcc	V
Enable Low Option Pin 2 Disabled Pin 2 Enabled		CMOS logic 1 or N/C CMOS logic 0	0.7 Vcc 0		Vcc 0.3 Vcc	V

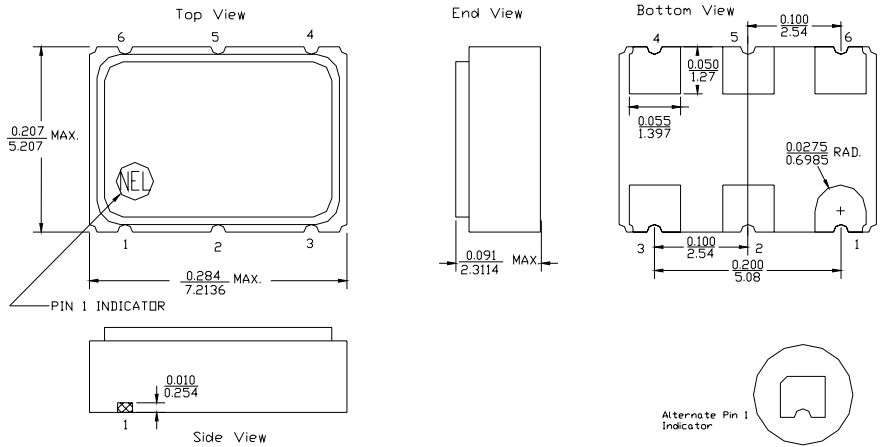


Rev. -

SD-A2D7XXX Series Continued

LVDS UHF CLOCK (XO) Electrical Connection

Pin	Connection
1	Enable/Disable
2	N.C.
3	V _{EE} /Ground
4	Output
5	/Output
6	V _{CC}

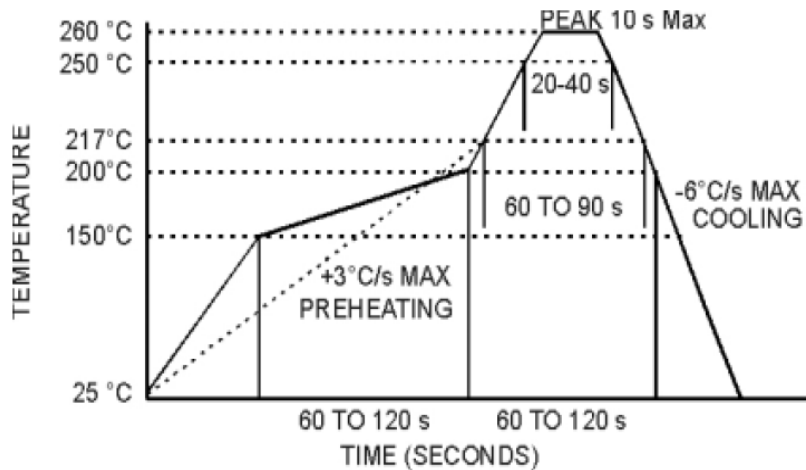


ALL DIMENSIONS: $\frac{IN}{mm}$
All tolerances are ± 0.005 inches (± 0.127 mm) unless otherwise specified.

Environmental and Mechanical Characteristics

Operating temp. range	see part # table
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. E
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Hermetic Seal	Leak rate less than 1×10^{-8} atm.cc/s of helium
Soldering conditions	See MAX reflow profile below

Maximum Reflow Profile



**FREQUENCY
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