



PRELIMINARY

SOLID STATE DEVICES, INC

14849 Firestone Boulevard · La Mirada, CA 90638  
Phone: (714) 670-SSDI (7734) · Fax: (714) 522-7424

### Designer's Data Sheet

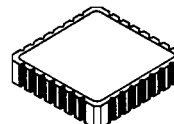
#### FEATURES:

- Rugged construction with poly silicon gate
- Low RDS(on) and high transconductance
- Excellent high temperature stability
- Very fast switching speed
- Fast recovery and superior dv/dt performance
- Increased reverse energy capability
- Low input and transfer capacitance for easy paralleling
- Hermetically sealed surface mount package
- TX, TXV and Space Level screening available
- Replaces: IRF340 Types

# SFF340-28

## 10 AMP 400 VOLTS 0.58Ω N-CHANNEL POWER MOSFET

28 PIN CLCC



#### MAXIMUM RATINGS

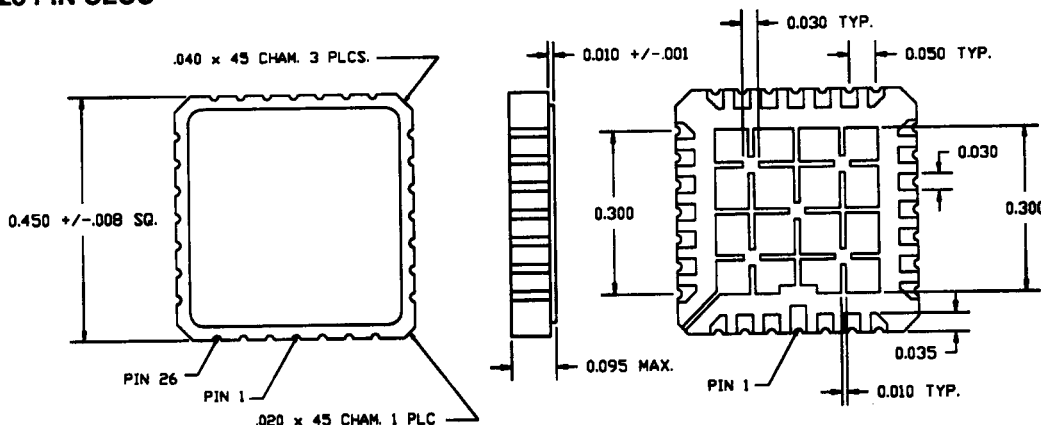
CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V <sub>DS</sub>	400	Volts
Gate to Source Voltage	V <sub>GS</sub>	±20	Volts
Continuous Drain Current	I <sub>D</sub>	10*	Amps
Operating and Storage Temperature	Top & T <sub>stg</sub>	-55 to +150	°C
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	3.5	°C/W
Total Device Dissipation @ TC=25°C	P <sub>D</sub>	36	Watts
Total Device Dissipation @ TC=80°C		27	

#### PACKAGE OUTLINE: 28 PIN CLCC

**PIN OUT:**  
**SOURCE: 1, 15-28**  
**DRAIN: 5-11**  
**GATE: 2, 3, 13, 14**

#### NOTE:

All Drain/Source Pins must be connected on the PC Board in order to maximize current capability and minimize RDS(on)



\* Rating based on size of chip. Device rating may vary depending on mounting and heatsink conditions. Consult SSDI Marketing department for thermal derating details.

NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: F00073 A

MED

# SFF340-28

PRELIMINARY



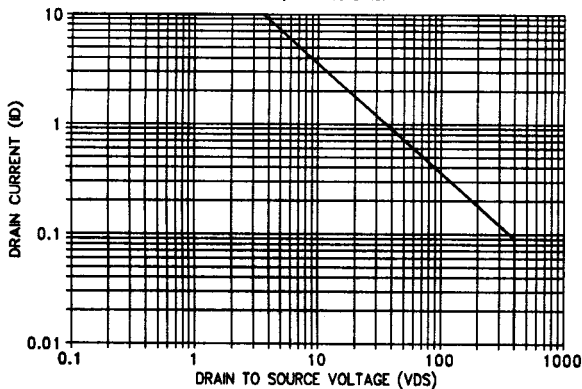
**SOLID STATE DEVICES, INC**

14849 Firestone Boulevard · La Mirada, CA 90638  
 Phone: (714) 670-SSDI (7734) · Fax: (714) 522-7424

## ELECTRICAL CHARACTERISTICS @ T<sub>J</sub>=25 °C (Unless Otherwise Specified)

RATING	SYMBOL	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage (V <sub>GS</sub> =0 V, I <sub>D</sub> =250μA)	BV <sub>DSS</sub>	400	---	---	V
Drain to Source on State Resistance (V <sub>GS</sub> =10 V, I <sub>D</sub> =60% Rated ID)	R <sub>DS(on)</sub>	---	0.42	0.58**	Ω
On State Drain Current (V <sub>DS</sub> > I <sub>D(on)</sub> X R <sub>DS(on)</sub> Max, V <sub>GS</sub> =10 V)	I <sub>D(on)</sub>	10*	---	---	A
Gate Threshold Voltage (V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA)	V <sub>GS(th)</sub>	2.0	---	4.0	V
Forward Transconductance (V <sub>DS</sub> ≥ 50V, I <sub>DS</sub> =60% rated ID)	g <sub>fs</sub>	5.8	8.7	---	S(Ω)
Zero Gate Voltage Drain Current (V <sub>DS</sub> =max rated voltage, V <sub>GS</sub> =0 V) (V <sub>DS</sub> =80% rated V <sub>DS</sub> , V <sub>GS</sub> =0 V, T <sub>A</sub> =125°C)	I <sub>DSS</sub>	---	---	250 1000	μA
Gate to Source Leakage Forward Gate to Source Leakage Reverse	At rated V <sub>GS</sub> I <sub>GSS</sub>	---	---	100 -100	nA
Total Gate Charge Gate to Source Charge Gate to Drain Charge	V <sub>GS</sub> =10 Volts 80% rated V <sub>DS</sub> I <sub>D</sub> =10A Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	---	43 6 22	65 9.3 33	nC
Turn on Delay Time Rise Time Turn Off Delay Time Fall Time	V <sub>DD</sub> =50% rated V <sub>DS</sub> I <sub>D</sub> =10A R <sub>G</sub> =9.1Ω R <sub>D</sub> =20Ω t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub>	---	14 27 50 24	9 30 74 36	nsec
Diode Forward Voltage (I <sub>S</sub> =rated ID, V <sub>GS</sub> =0 V, T <sub>J</sub> =25°C)	V <sub>SD</sub>	---	---	2.0	V
Diode Reverse Recovery Time Reverse Recovery Charge	T <sub>J</sub> =25°C I <sub>F</sub> =rated ID di/dt=100 A/μsec t <sub>rr</sub> Q <sub>RR</sub>	170 1.6	370 3.8	790 8.2	nsec μC
Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>GS</sub> =0 Volts V <sub>DS</sub> =25 Volts f=1 MHz C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	---	1300 210 37	---	pF

SAFE OPERATING AREA (S.O.A.)  
 T<sub>C</sub> = 25 °C, D.C. CONDITION



### NOTES:

- \* Rating based on size of chip. Device rating may vary depending on mounting and heatsink conditions. Consult SSDI Marketing department for thermal derating details.
- \*\* Due to package resistance; all Source/Drain pins must be connected on the PC Board in order to obtain the lowest R<sub>DS(on)</sub> possible.