Preliminary

SGA-8543Z

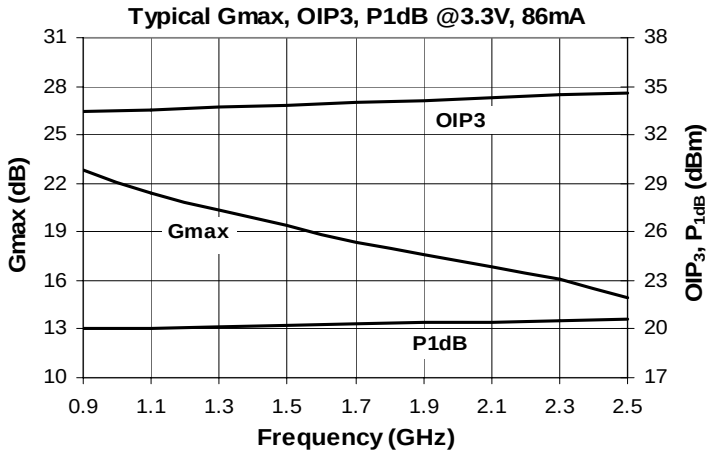
RoHS Compliant & Green Package

High IP3, Medium Power Discrete SiGe Transistor

Product Description

Sirenza Microdevices' SGA-8543Z is a high performance Silicon Germanium Heterostructure Bipolar Transistor (SiGe HBT) designed for operation from DC to 3.5 GHz. The SGA-8543Z is optimized for 3.3V operation but can be biased at 2.7V for low-voltage battery operated systems. The device provides low NF and excellent linearity at a low cost. It can be operated over a wide range of currents depending on the power and linearity requirements.

The matte tin finish on Sirenza's lead-free "Z" package is applied using a post annealing process to mitigate tin whisker formation and is RoHS compliant per EU Directive 2002/95. The package body is manufactured with green molding compounds that contain no antimony trioxide or halogenated fire retardants.



Product Features

- DC-3.5 GHz Operation
- Lead Free, RoHS Compliant & Green Package
- 1.5 dB NF_{MIN} @ 2.44 GHz
- 15.6 dB Gmax @ 2.44 GHz
- P_{1dB} = +20.6 dBm @ 2.44 GHz
- OIP_3 = +34.6 dBm @ 2.44 GHz
- Low Cost, High Performance, Versatility

Applications

- Analog and Digital Wireless Systems
- 3G, Cellular, PCS, RFID
- Fixed Wireless, Pager Systems
- PA stage for Medium Power Applications
- AN-079 contains detailed application circuits

Symbol	Parameters	Units	Frequency	Min.	Typ.	Max.
G_{MAX}	Maximun Available Gain $Z_S=Z_S^*$, $Z_L=Z_L^*$	dB	880 MHz 2440 MHz		22.9 15	
S_{21}	Insertion Gain [1]	dB	880 MHz		18	
G	Power Gain [2] $Z_S=Z_{SOPT}$, $Z_L=Z_{LOPT}$	dB	880 MHz 2440 MHz		19 14	
P_{1dB}	Output Power at 1dB Compression [2] $Z_S=Z_{SOPT}$, $Z_L=Z_{LOPT}$	dBm	880 MHz 2440 MHz		20 20.6	
OIP_3	Output Third Order Intercept Point [2] $Z_S=Z_{SOPT}$, $Z_L=Z_{LOPT}$	dBm	880 MHz 2440 MHz		33.4 34.6	
NF	Noise Figure [2] $Z_S=Z_{SOPT}$, $Z_L=Z_{LOPT}$	dB	880 MHz 2440 MHz		3.1 2.4	
NFmin	Minimum Noise Figure with I_{CE} = 25mA $Z_S=\Gamma_{OPT}$, $Z_L=Z_L^*$	dB	880 MHz 2440 MHz		1.0 1.5	
h_{FE}	DC Current Gain			120	180	300
BV_{CEO}	Collector - Emitter Breakdown Voltage	V		5.7	6	
Rth, j-l	Thermal Resistance (Junction - lead)	°C/W			151	
V_{CE}	Device Operating Voltage (collector- emitter)	V				3.8
I_{CE}	Device Operating Current (collector - emitter)	mA				95

Test Conditions: V_{CE} = 3.3V, I_{CE} = 86mA Typ. (unless noted otherwise), T_L = 25°C OIP_3 Tone Spacing = 1MHz, Pout per tone = 5 dBm

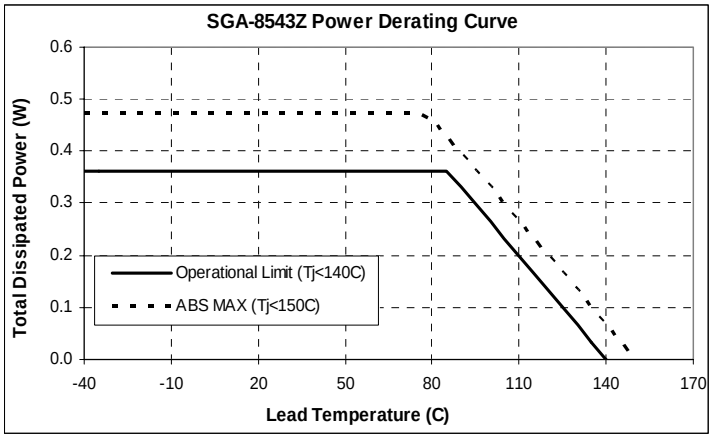
[1] 100% production tested using 50 ohm contact board (no matching circuitry) [2] Data with Application Circuit

Absolute Maximum Ratings

Parameter	Absolute Limit
Max Device Current (I_{CE})	105 mA
Max Device Voltage (V_{CE})	4.5 V
Max. RF Input Power* (See Note)	+18 dBm
Max. Dissipated Power	See Graph
Max. Junction Temp. (T_J)	+150°C
Operating Temp. Range (T_L)	See Graph
Max. Storage Temp.	+150°C

***Note:** Load condition 1, Z_L = 50 Ohms
Load condition 2, ZL = 10:1 VSWR

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.
Bias Conditions should also satisfy the following expression:
$I_D V_D < (T_J - T_L) / R_{TH, j-l}$ $T_L = T_{LEAD}$



Reliability & Qualification Information	
Parameter	**Rating**
ESD Rating - Human Body Model (HBM)	Class 1B
Moisture Sensitivity Level	MSL 1

This product qualification report can be downloaded at *www.sirenza.com*

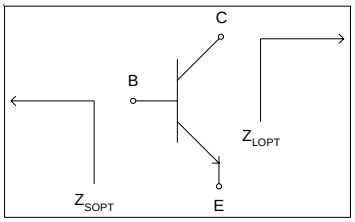
Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

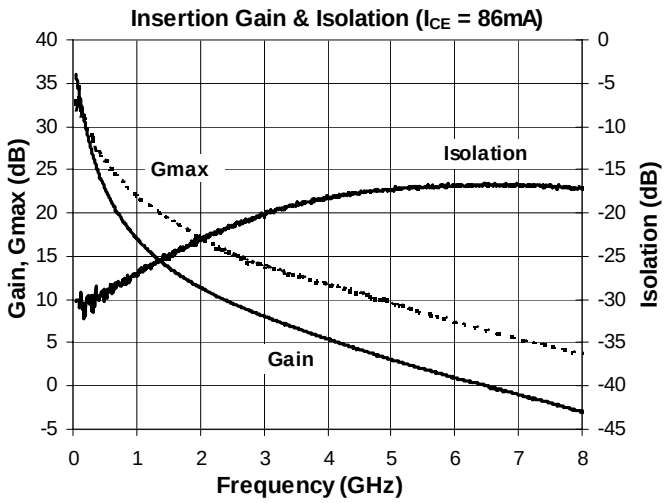
Typical performance - Engineering Application Circuits (See AN-079)

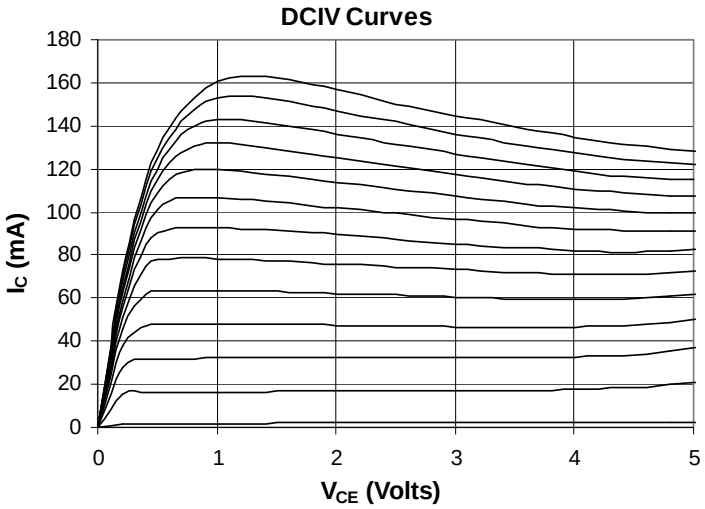
Freq (MHz)	V_{CE} (V)	I_{CE} (mA)	P_{1dB} (dBm)	OIP_3 (dBm)	Gain (dB)	S11 (dB)	S22 (dB)	NF (dB)	Z_{SOPT} (Ω)	Z_{LOPT} (Ω)
880	3.3	86	20.0	33.4	19.0	-15.0	-11.0	3.1	22.7 - j2.5	32.5 + j11.9
2440	3.3	86	20.6	34.6	14.0	-16.0	-22.0	2.4	9.3 - j9.9	21.4 + j1.9

Test Conditions: V_S = 5V I_S = 96mA Typ. OIP_3 Tone Spacing = 1MHz, Pout per tone = 5 dBm TL = 25°C

Data above represents typical performance of the application circuits noted in Application Note AN-079. Refer to the application note for additional RF data, PCB layouts, and BOMs for each application circuit. The application note also includes biasing instructions and other key issues to be considered. For the latest application notes please visit our site at www.sirenza.com or call your local sales representative.





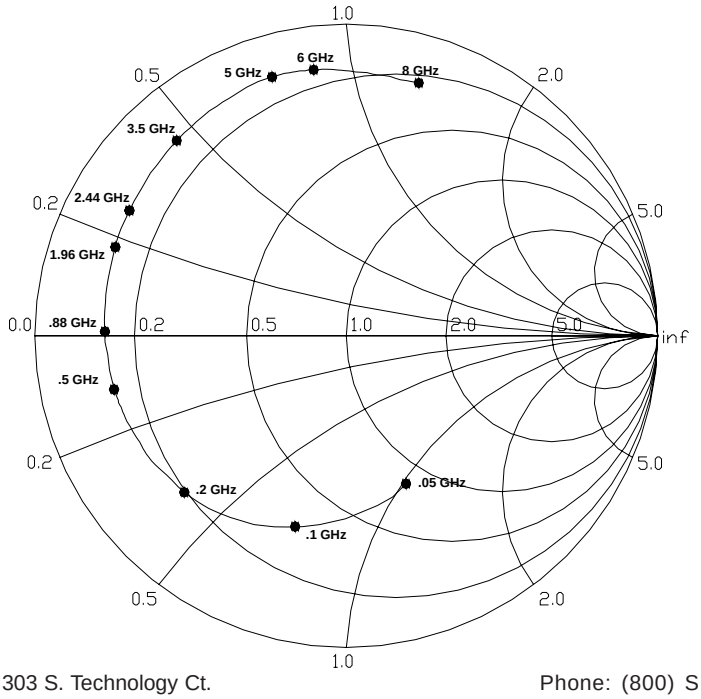


I_B = 0.1 - 1.1 mA, T=25°C

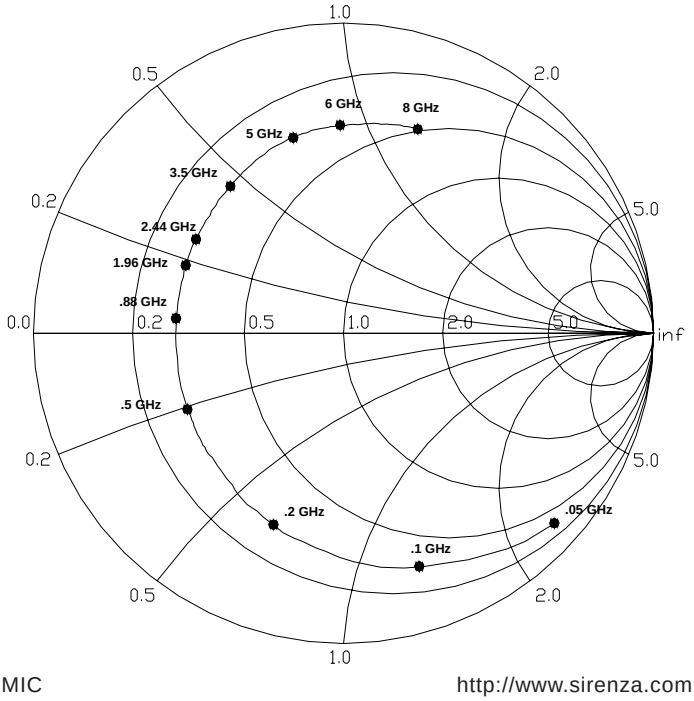
Typical Performance - De-embedded S-parameters

Note: S-parameters are de-embedded to the device leads with Z_S=Z_L=50Ω. The device was mounted on Sirenza's recommended evaluation board. De-embedded S-parameters can be downloaded from our website (www.sirenza.com)

S11 Vs. Frequency



S22 Vs. Frequency



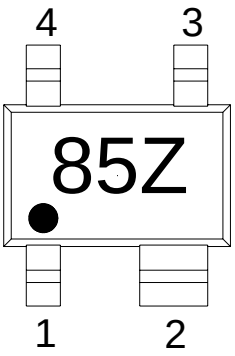
Pin Description

Pin #	Function	Description
1	RF IN	RF input / Base Bias. External DC blocking capacitor required
2	GND	Connection to ground. Use via holes to reduce lead inductance. Place via holes as close to lead as possible
3	RF OUT	RF Out / Collector bias. External DC blocking capacitor required
4	GND	Same as pin 2

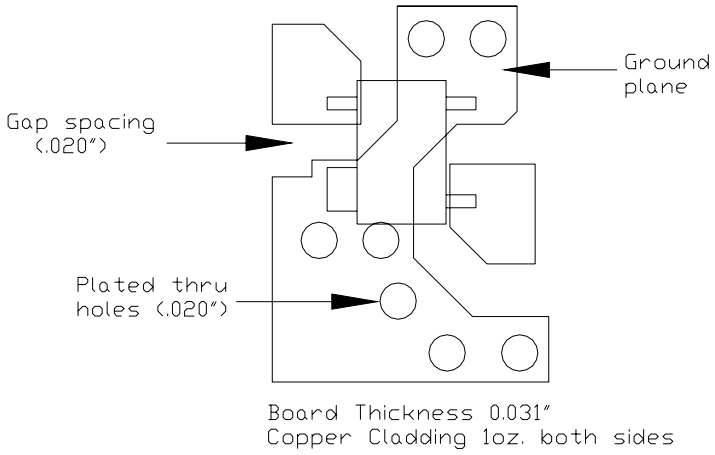
Part Number Ordering Information

Part Number	Reel Size	Devices / Reel
SGA-8543Z	7"	3000

Part Identification

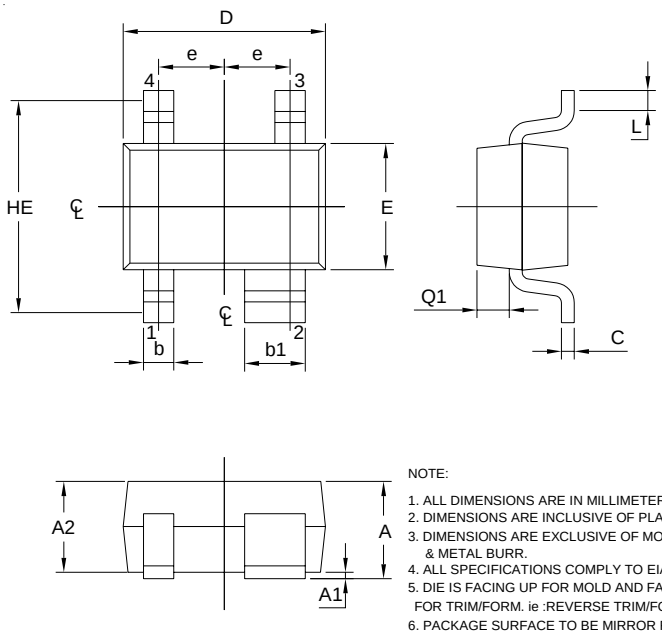


Suggested Pad Layout



Use multiple plated-through vias holes located close to the package pins to ensure a good RF ground connection to a continuous groundplane on the backside of the board.

Package Dimension



SYMBOL	MIN	MAX
E	1.15	1.35
D	1.85	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
Q1	0.10	0.40
e	0.65 BSC	
b	0.25	0.40
b1	0.55	0.70
c	0.10	0.18
L	0.10	0.30

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70.
5. DIE IS FACING UP FOR MOLD AND FACING DOWN FOR TRIM/FORM. ie :REVERSE TRIM/FORM.
6. PACKAGE SURFACE TO BE MIRROR FINISH.