

HITACHI

SH7750 (SH-4 Series)

SuperH™ RISC Processor

Product Brief

Designed for



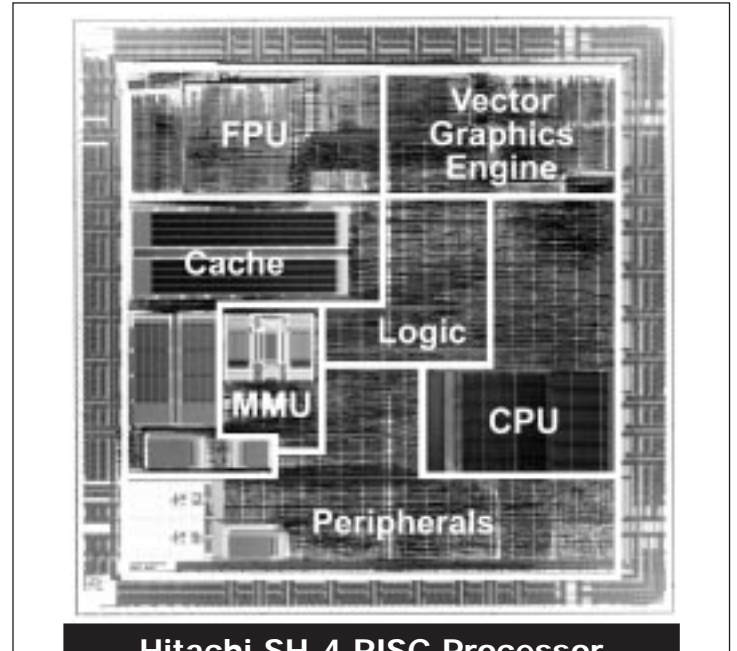
Microsoft
Windows[®]CE

Description

The SH7750 (SH-4 series) is a high performance, cost-effective, 2 issue superscalar RISC microprocessor for embedded applications. The SuperH™ architecture is the leader in code density among RISC microprocessors, reducing memory costs in embedded applications. It features a 64-bit external data bus, a 16-bit fixed-length instruction set and a 128-bit vector graphics engine.

The SH7750 is used in consumer, computing, multimedia, and communication markets. Applications include handheld PCs, sub-notebook PCs, Internet appliances, set top boxes, and game machines. The device can be paired with an ASSP companion device for a low cost, low IC count, and differentiated system.

Hitachi optimized the SH7750 MMU, cache size, and peripheral mix for Windows[®]CE applications.



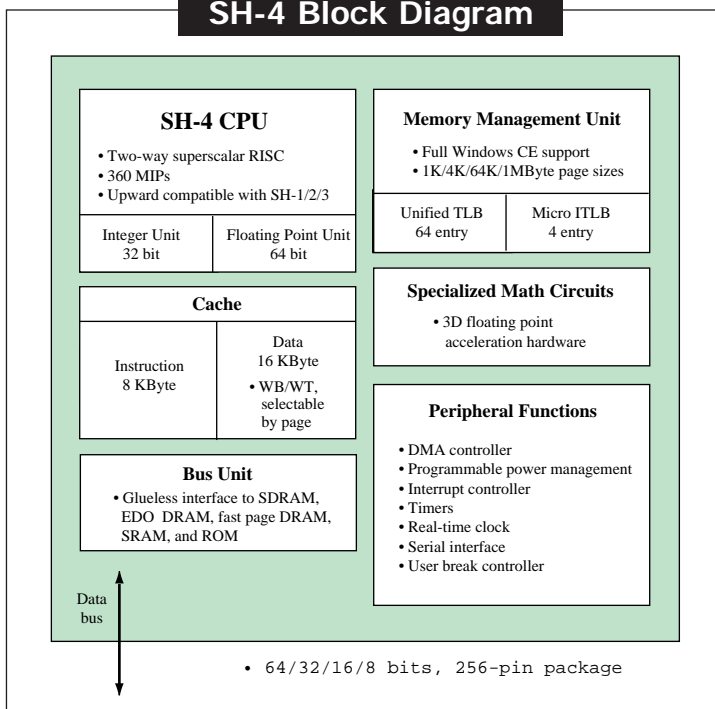
Hitachi SH-4 RISC Processor

Features

- General
 - 200 MHz/360 MIPS at 3.3V I/O, 1.8V internal
 - 16 x 32-bit general purpose registers
 - 256 pin LBGA

- CPU
 - Code compatible with SH7000/7600/7700 series
 - 16 x 32-bit general purpose registers
 - 32 x 32-bit single-precision floating point registers or 16 x 64-bit double-precision floating point registers or 4 x 128-bit single-precision vector registers and register matrix
 - 16-bit fixed instruction length for high code density
 - 32 x 32 + 64 --> 64 bits multiply-accumulate unit for special functions such as software modems
 - MMU Designed for Windows[®]CE 1KB, 4KB, 64KB, and 1MB page sizes, 64-entry, fully associative UTLB
 - 4 entry, fully associative μ TLB
 - 5 stage pipeline

SH-4 Block Diagram



- Memory
 - On-chip cache, 8KB instruction and 16KB data
 - Write back or write through, selectable by page
 - Low voltage cache to reduce power consumption
 - On-chip bus state controller allows direct connection to DRAM, SDRAM, SRAM, ROM, and Flash ROM
 - 8, 16, 32, or 64-bit data bus support
- Peripherals
 - DMA, 4 channels
 - Timers, 3 channels x 32-bits
 - Watchdog timer

- Realtime clock
- PCMCIA control logic
- Serial communications interface, 1 channel (asynchronous/synchronous, with smart card interface)
- Serial communication interface 1 channel (asynchronous, with 16 byte transmit and receive FIFOs)
- PLL with x1/8, x1/6, x1/4, x1/2, x3/4, x1, x3/2, x2, x3, x6 external clock capability
- Interrupt controller

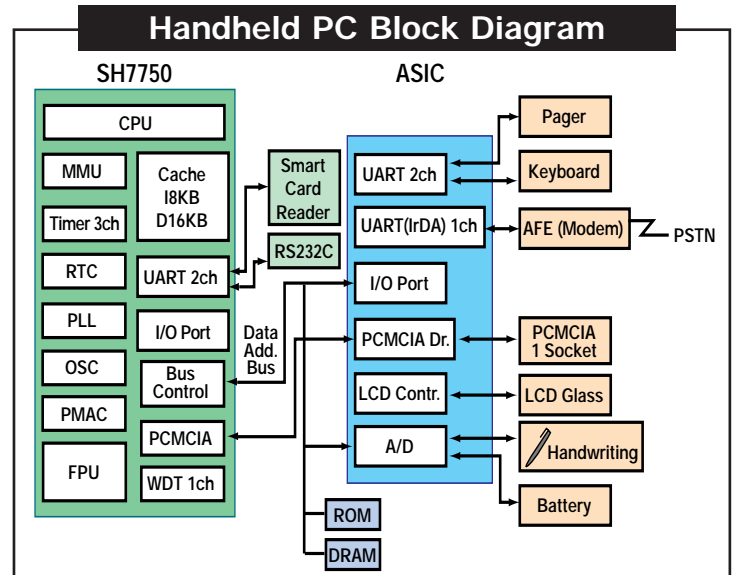
- General purpose I/O, 16 lines
- Dynamic power control
 - Low power modes: sleep and standby
 - Peripheral turn off capability
- User break controller for on-chip debugging

Support

- Hardware:
 - Hitachi E10 emulator
 - Hitachi D9000 development platform for SH7750 and Windows®CE
- Software:
 - Hitachi:
 - C, C++ compiler, assembler, simulator/debugger
 - Third parties:
 - C, C++ compiler, assembler, simulator/debugger, Cygnus Support (gnu), Green Hills Software, Microsoft® VC++ for Windows CE
- Operating Systems:
 - Windows®CE, Hitachi OS, and others

Middleware

- V.32 (up to 33.6 Kbps) Data/FAX software modem
- Voice recognition
- Voice compression
- Handwriting recognition
- JPEG video compression
- Image compression for FAX: MH, MR, MMR



Ordering Information

Part numbers:

SH7750-HD6417750BP200 (200 MHz, LBGA-256)

Complete SH-4 technical documentation is online at:

<http://www.hitachi.com/semiconductor>

This document may, wholly or partially, be subject to change without notice.

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