



N-Channel 20-V (D-S) MOSFET

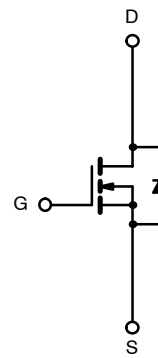
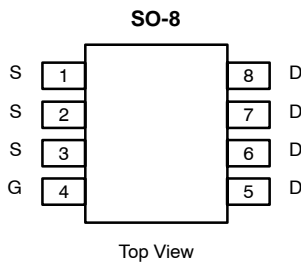
PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
20	0.0027 @ V _{GS} = 4.5 V	25
	0.0042 @ V _{GS} = 2.5 V	22

FEATURES

- Ultra Low On-Resistance Using High Density TrenchFET® Gen II Power MOSFET Technology
- Q_g Optimized
- 100% R_g Tested

APPLICATIONS

- Synchronous Rectification
- Point-Of-Load



N-Channel MOSFET

Ordering Information: Si4378DY—E3
Si4378DY-T1—E3 (with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	10 secs	Steady State	Unit
Drain-Source Voltage	V _{DS}	20		V
Gate-Source Voltage	V _{GS}	± 12		
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	25	19
		T _A = 70 °C	20	13
Pulsed Drain Current (10 μs Pulse Width)	I _{DM}	70		A
Continuous Source Current (Diode Conduction) ^a	I _S	2.9	1.3	
Avalanche Current	L = 0.1 mH I _{AS}	40		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	3.5	1.6
		T _A = 70 °C	2.2	1
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 sec	29	35
		Steady State	67	80
Maximum Junction-to-Foot (Drain)	R _{thJF}	13	16	°C/W

Notes

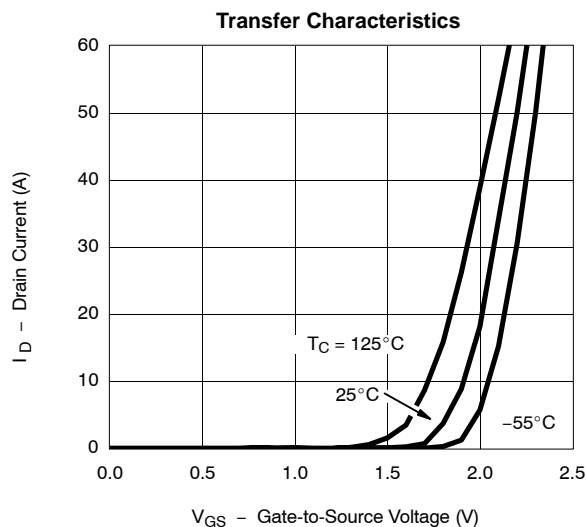
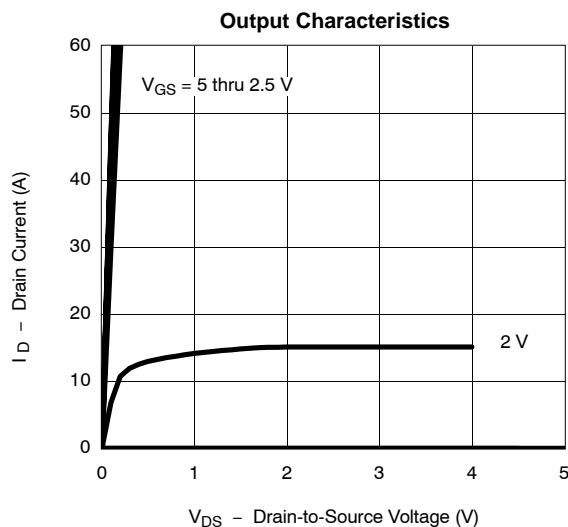
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.6		1.8	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	30			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 25 A		0.0022	0.0027	Ω
		V _{GS} = 2.5 V, I _D = 22 A		0.0034	0.0042	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 25 A		150		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.9 A, V _{GS} = 0 V		0.72	1.1	V
Dynamic^b						
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		8500		pF
Output Capacitance	C _{oss}			1250		
Reverse Transfer Capacitance	C _{rss}			650		
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 25 A		55		nC
Gate-Source Charge	Q _{gs}			16		
Gate-Drain Charge	Q _{gd}			10		
Gate Resistance	R _g		0.8	1.3	2.0	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _g = 6 Ω		85	130	ns
Rise Time	t _r			65	100	
Turn-Off Delay Time	t _{d(off)}			140	210	
Fall Time	t _f			50	80	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.9 A, di/dt = 100 A/μs		50	80	

Notes

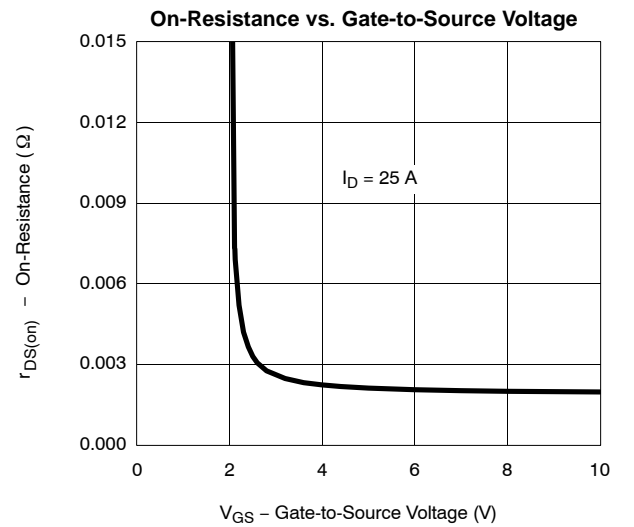
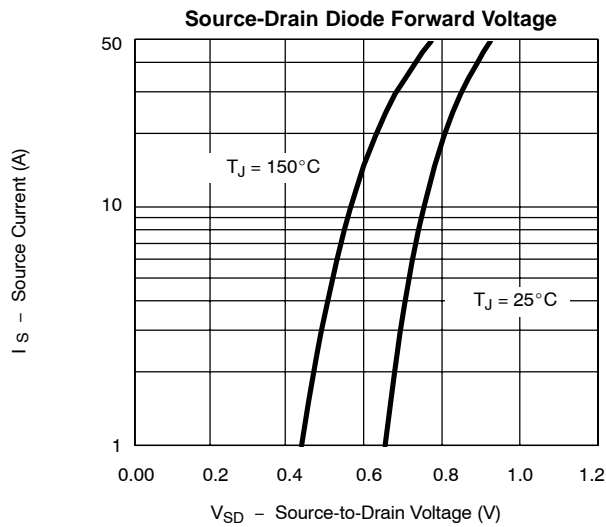
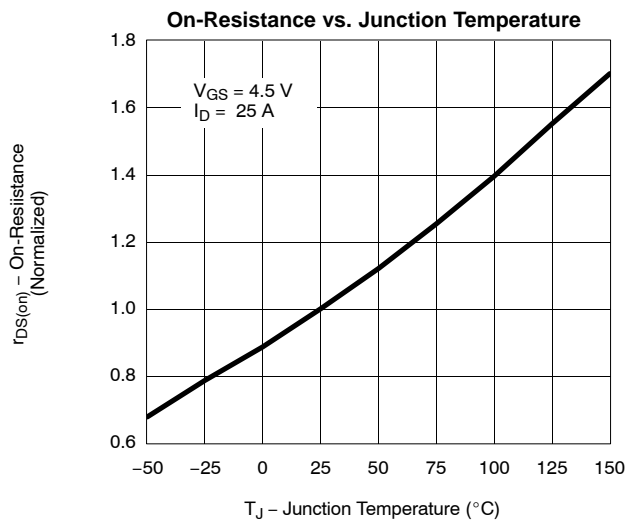
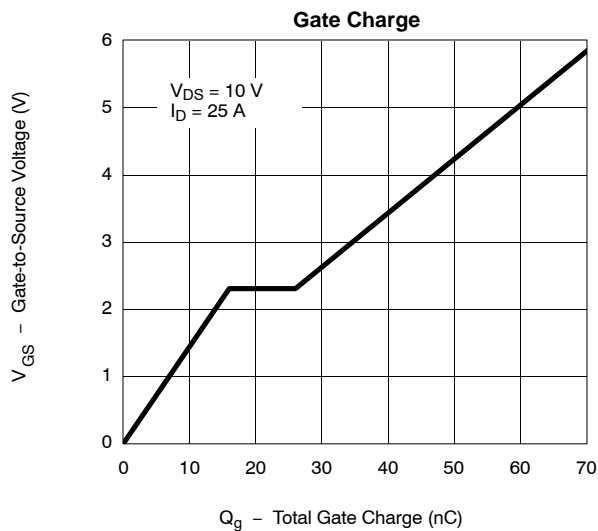
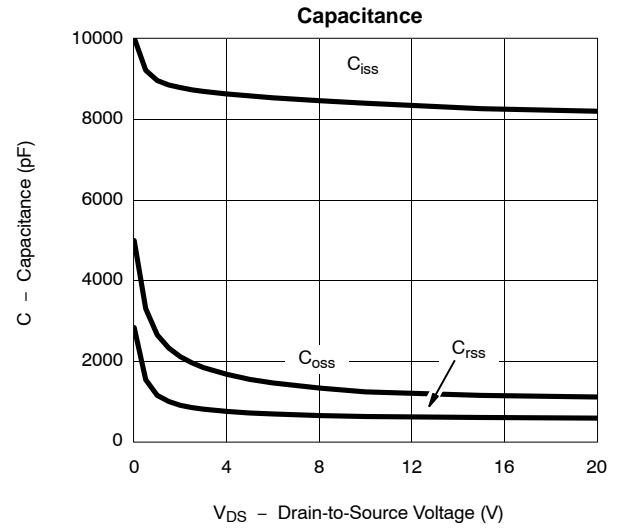
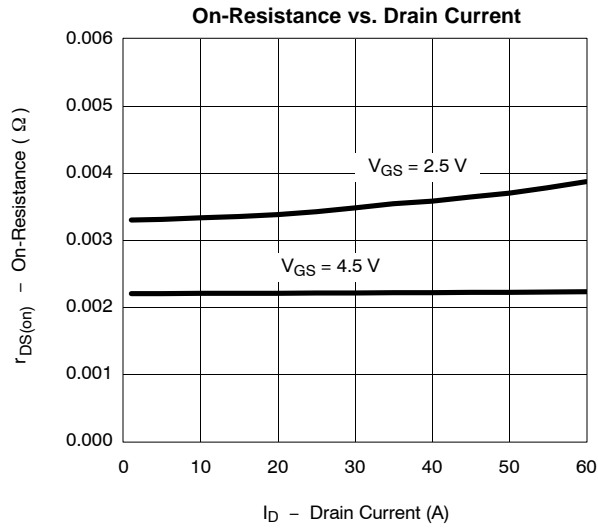
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

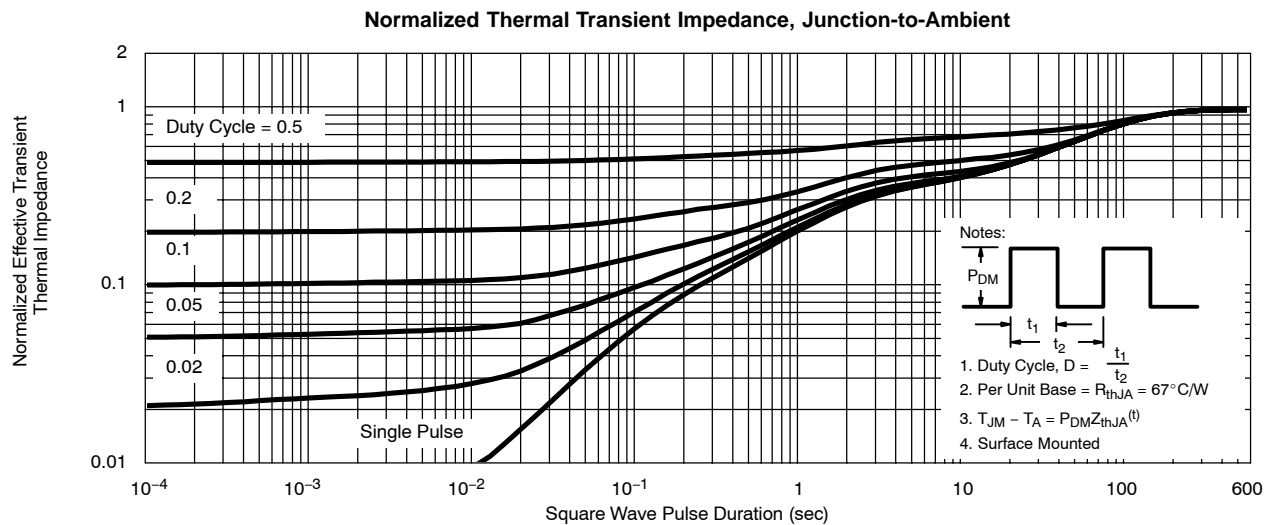
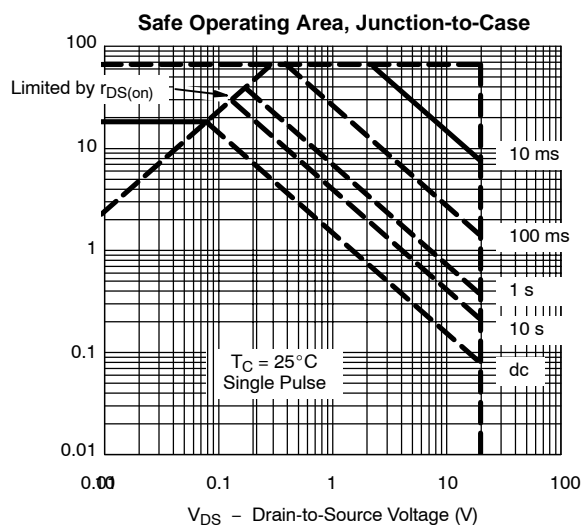
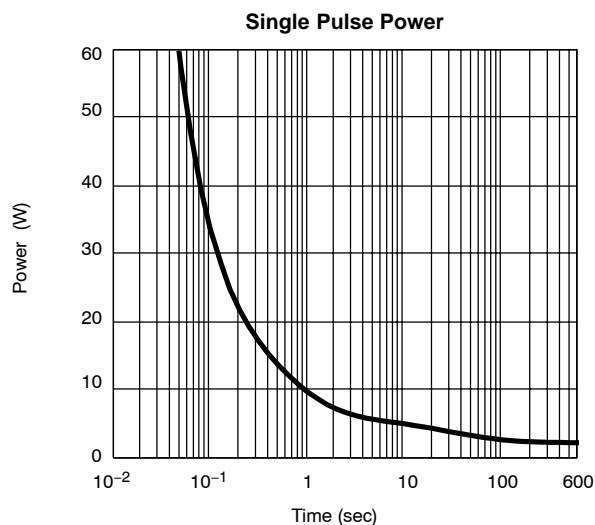
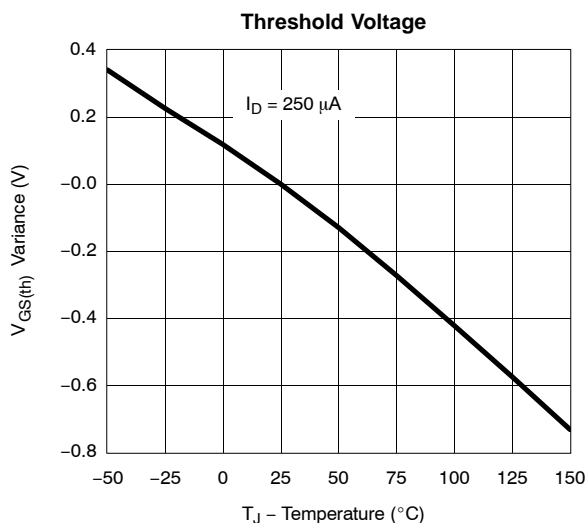




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