High-Side N-Channel Switch with Current Limit

FEATURES

- User Set Over Current Limit From 400 mA to 2.4 A
- Low $r_{DS(on)}$ 45 mΩ (max) at 25°C
- Fault Indicator
- Under Voltage Lockout

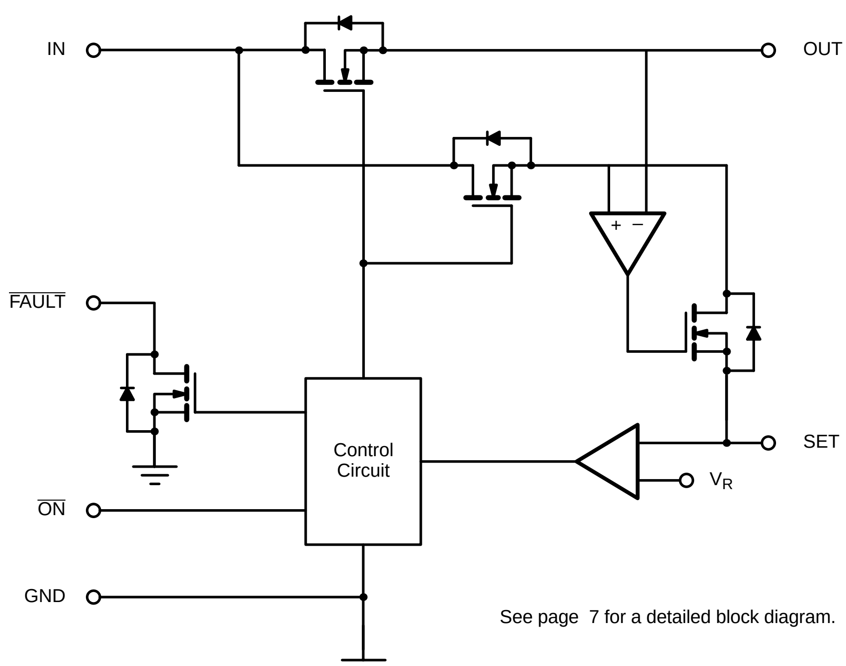
APPLICATIONS

- Notebook Computers Power Management
- USB Power Distribution
- Hot Plug In Power Supplies
- Power Supply/Load Protection
- Battery-Charger Circuits

DESCRIPTION

The Si4779CY n-channel high-side switch combines a low $r_{DS(on)}$ MOSFET switch with a user set, pulse gate control (PGC) based current limit. This switch is designed to protect the system power supply from overloads and short circuit conditions in applications such as USB. The PGC based approach to the current limiter provides the additional benefit of keeping the MOSFET junction temperature within specification, thereby eliminating the need for thermal shutdown. The low quiescent current makes the Si4779CY ideal for use in battery powered devices. The Si4779CY operates on both 3-V and 5-V busses, and is packaged in the LITTLE FOOT® SO-8 package.

FUNCTIONAL BLOCK DIAGRAM



See page 7 for a detailed block diagram.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		**Symbol**	**Steady State**	**Unit**
Voltage, IN to GND		V_{IN}	–0.3 to 7	V
Voltage, $\overline{ON}$		V_{ON}	–0.3 to 7	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	2.4	A
	T_A = 85°C		2.4	
Maximum Power Dissipation[a]	T_A = 70°C	P_D	0.65	W
Operating Junction and Storage Temperature Range		T_j, T_{stg}	–65 to 125	°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS			
Parameter	**Symbol**	**Steady State**	**Unit**
Voltage, IN to GND	V_{IN}	3.0 to 5.0	V
Voltage, $\overline{ON}$ or $\overline{FAULT}$ to GND	V_{ON}, V_{FAULT}	0 to 5.0	
Operating Temperature Range	T_A	0 to 85	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Junction-to-Ambient[a]	Steady State	R_{thJA}	98	120	°C/W
Junction-to-Foot (Drain)[b]		R_{thJF}	37	46	

Notes
a. Surface mounted on 1" x1" FR4 board, 0.062" thick, 2-oz copper double sided.
b. Junction-to-foot thermal impedance represents the effective thermal impedance of all heat carrying leads in parallel and is intended for use in conjunction with the thermal impedance of the PC board pads to ambient ($R_{thJA} = R_{thJF} + R_{thPCB-A}$). It can also be used to estimate chip temperature if power dissipation and the lead temperature of a heat carrying (drain) lead is known.

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified T_A = 25°C, V_{IN} = 5 V	Limits Min	Typ[a]	Max	Unit
Basic Operations						
Operating Voltage	V_{IN}		2.7		5.5	V
On-State Resistance	$r_{DS(on)}$	V_{IN} = 4.75 V, I_D = 2 A		0.035	0.045	Ω
		V_{IN} = 3.0 V, I_D = 2 A		0.045	0.055	
Supply Current	$I_{SUP(off)}$	$\overline{ON}$ = IN, V_{IN} = 5.5 V, V_{OUT} = 0 V			2	µA
	$I_{SUP(on)}$	$\overline{ON}$ = GND, V_{IN} = V_{OUT} = 5.5 V, I_{OUT} = 0 A			70	
$\overline{ON}$ Input Low Voltage	V_{ONL}	V_{IN} = 2.7 to 5.5 V			0.8	V
$\overline{ON}$ Input High Voltage	V_{ONH}	V_{IN} = 2.7 to 3.6 V	2.0			
		V_{IN} = 4.5 to 5.5 V	2.4			
$\overline{ON}$ Input Current	I_{ON}	$V_{\overline{ON}}$ = 5.5 V		0.01	±1	µA
Protection						
Over Current Limit Range[b]	I_{LIMIT}	Tolerance = ±20%, V_{IN} = 5 V	0.4		2.4	A
Under Voltage Lockout (falling edge)	UVLO		2.0	2.3	2.6	V
Under Voltage Hysteresis	ΔUVLO			0.1		
$\overline{FAULT}$ Output Voltage Low[b]	V_{FAULT}	I_{SINK} = 100 µA			0.4	
$\overline{FAULT}$ Logic Output Leakage Current	I_{FL}	V_{IN} = V_{FAULT} = 5.5 V		0.01	1	µA
Dynamic[b]						
Turn-On Time	t_{on}	V_{IN} = 5 V, R_L = 11 Ω, C_L = 40 µF		3		ms
Rise Time	t_r			3.5		
Turn-Off Time	t_{off}	V_{IN} = 5 V, I_{OUT} = 500 mA		1.5		µs
Fall Time	t_f			0.5		
Cycle Time	t_{cyc}	V_{IN} = 5 V, R_L = 0.5 Ω		8		ms

Notes
a. Typical values at T_A = 25°C are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. Guaranteed by design. Derived from I_{SET} current ratio, current-limit amplifier and external set resistor accuracy.

TIMING DIAGRAMS

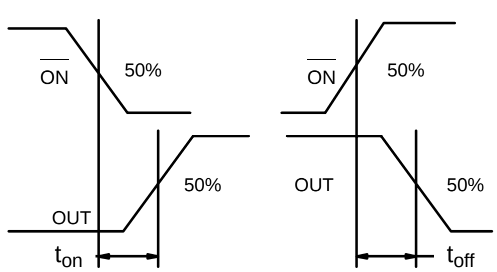


FIGURE 1.

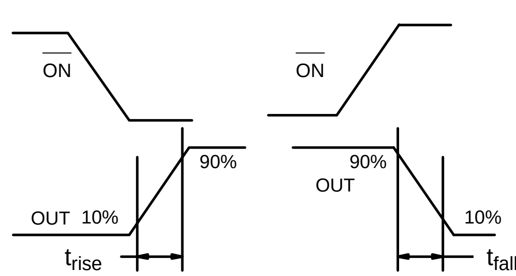


FIGURE 2.

TIMING DIAGRAMS

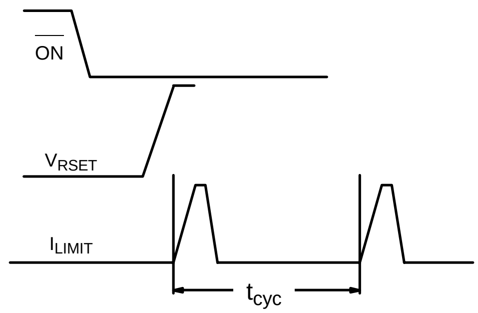
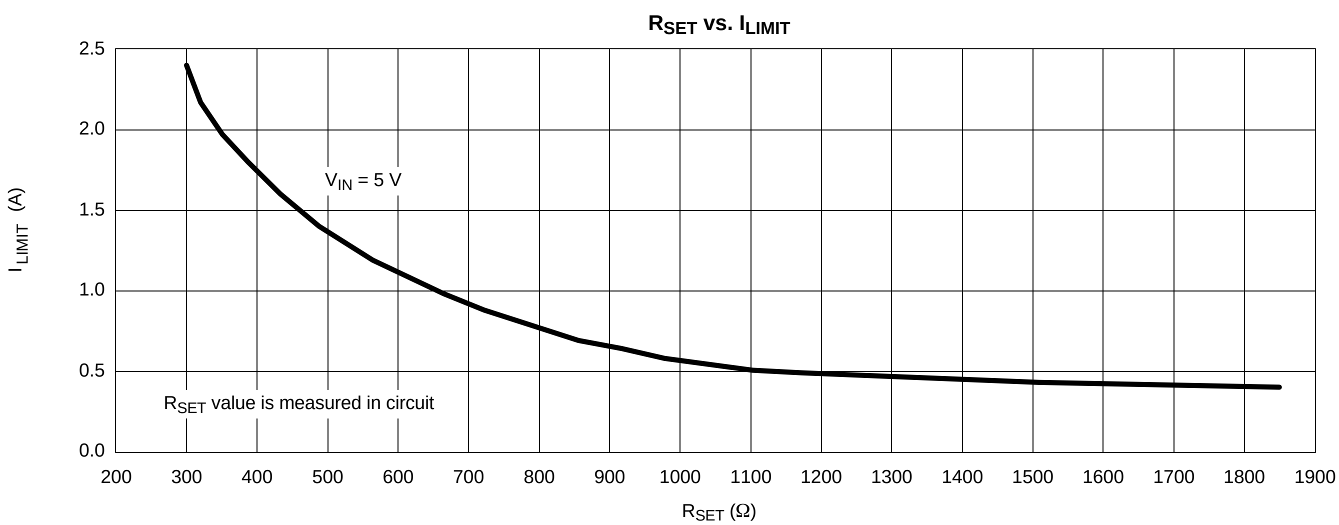
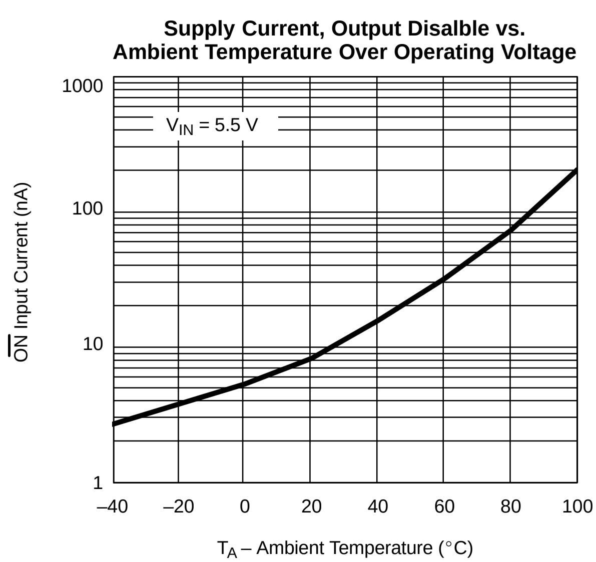
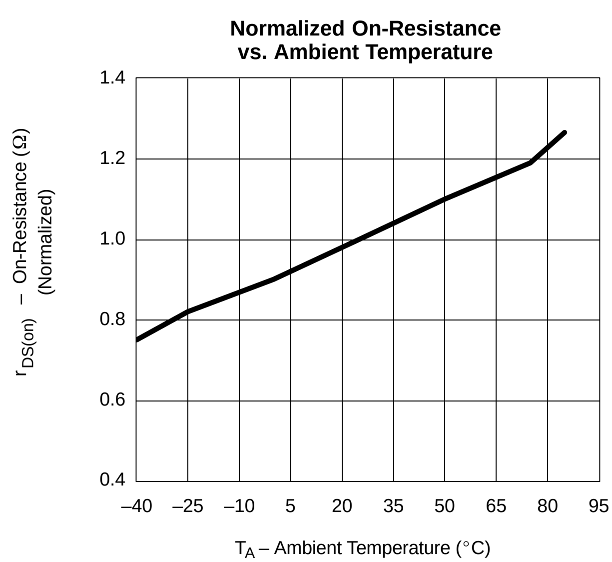


FIGURE 3.

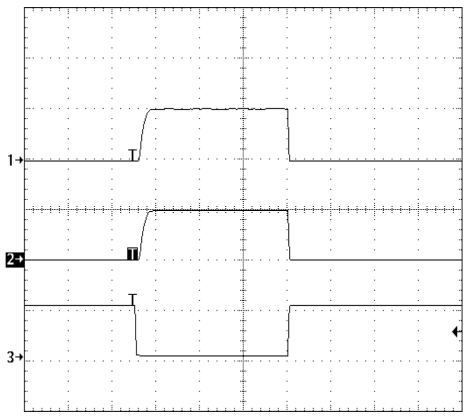
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)







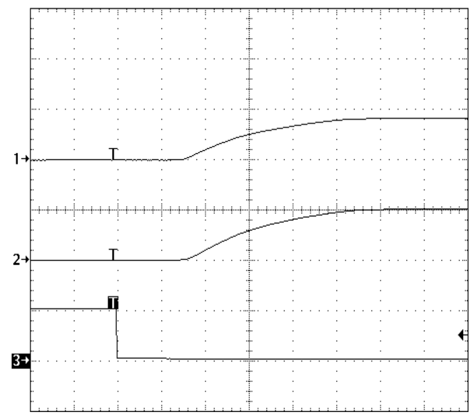
TYPICAL WAVEFORMS (V_{IN} = 5 V, T_A = 25° UNLESS OTHERWISE NOTED)



20 ms/div

CH1: I_{OUT}, 2 A/div
CH2: V_{OUT}, 5 V/div, C_L = 47 µF
CH3: $\overline{ON}$, 5 V/div

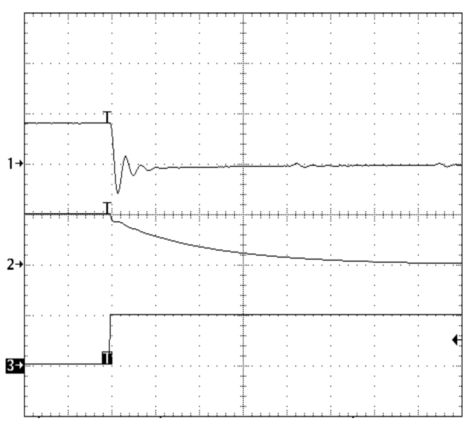
FIGURE 4. Switch Turn-ON/OFF Time



1 ms/div

CH1: I_{OUT}, 0.5 A/div
CH2: V_{OUT}, 5 V/div, C_L = 10 µF
CH3: $\overline{ON}$, 5 V/div

FIGURE 5. Switch Turn-ON Time

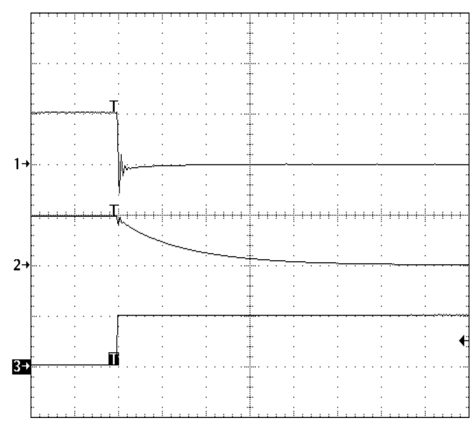


50 µs/div

CH1: I_{OUT}, 0.5 A/div
CH2: V_{OUT}, 5 V/div, C_L = 10 µF
CH3: $\overline{ON}$, 5 V/div

NOTE: Discharge time based primarily on external R and C

FIGURE 6. Switch Turn-OFF Time



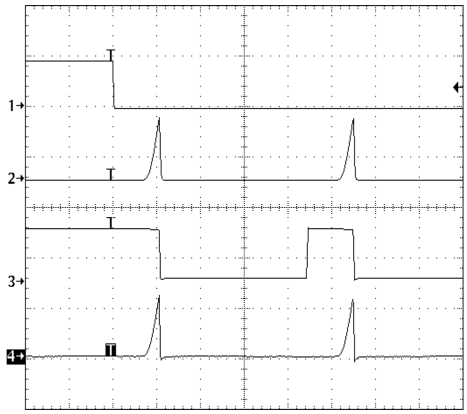
200 µs/div

CH1: I_{OUT}, 0.5 A/div
CH2: V_{OUT}, 5 V/div, C_L = 150 µF
CH3: $\overline{ON}$, 5 V/div

NOTE: Discharge time based primarily on external R and C

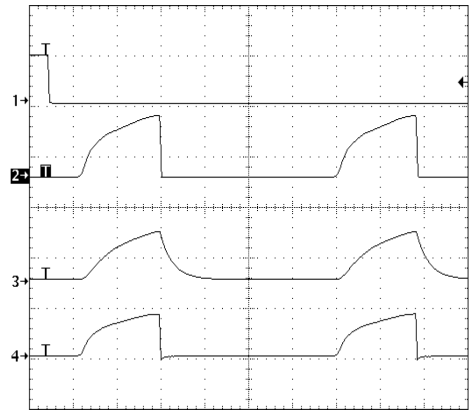
FIGURE 7. Switch Turn-OFF Time

TYPICAL WAVEFORMS (V_{IN} = 5 V, T_A = 25° UNLESS OTHERWISE NOTED)


2 ms/div

CH1: $\overline{ON}$, 5 V/div
CH2: V_{OUT}, 5 V/div, R_L = 0.5 Ω, C_L = 47 μF
CH3: $\overline{FAULT}$, 5 V/div
CH4: I_{OUT}, 1 A/div

FIGURE 8. FAULT to Short Response (t_{cyc})


2 ms/div

CH1: $\overline{ON}$, 5 V/div
CH2: V_{RESET}, 500 mV/div
CH3: V_{OUT}, 5 V/div, R_L = 5.6 Ω, C_L = 100 μF
CH4: I_{OUT}, 1 A/div

FIGURE 9. V_{RESET} to Over Current Response


2 ms/div

CH1: $\overline{ON}$, 5 V/div
CH2: PS Droops, 50 mV/div, Offset = 5 V
CH3: V_{OUT}, 1 V/div, R_L = 0.5 Ω, C_L = 100 μF
CH4: I_{OUT}, 0.5 A/div

NOTE: Special test with 820-μF capacitor at PS and R_{SET} setup for 0.5 A.

FIGURE 10. Power Supply Droops vs. Short


2 ms/div

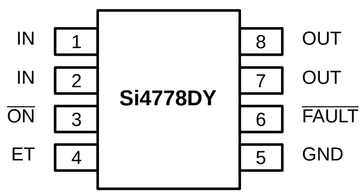
CH1: $\overline{ON}$, 5 V/div
CH2: PS Droops, 100 mV/div, Offset = 5 V
CH3: V_{OUT}, 1 V/div, R_L = 0.5 Ω, C_L = 100 μF
CH4: I_{OUT}, 2 A/div

NOTE: Special test with 820-μF capacitor at PS and R_{SET} setup for 2.4 A.

FIGURE 11. Power Supply Droops vs. Short

PIN CONFIGURATION

SO-8



Top View

PIN DESCRIPTION		
Pin	**Symbol**	**Description**
1, 2	IN	Input. N-channel MOSFET drain, bypass IN with a 100-µF capacitor to GND.
3	$\overline{\text{ON}}$	Active-low switch-on input, logic low turns switch on. $\overline{\text{ON}}$ needs to be connected to V_{IN} during power up, then connect to GND to activate the switch after power up.
4	SET	Current-limit input. A resistor from SET to GND sets the current limit for the switch.
5	GND	Ground
6	$\overline{\text{FAULT}}$	Fault indicator output. This open drain output goes low when the circuit is in current limit or in short circuit protection mode.
7, 8	OUT	Switch output. N-channel MOSFET source.

DETAILED BLOCK DIAGRAM

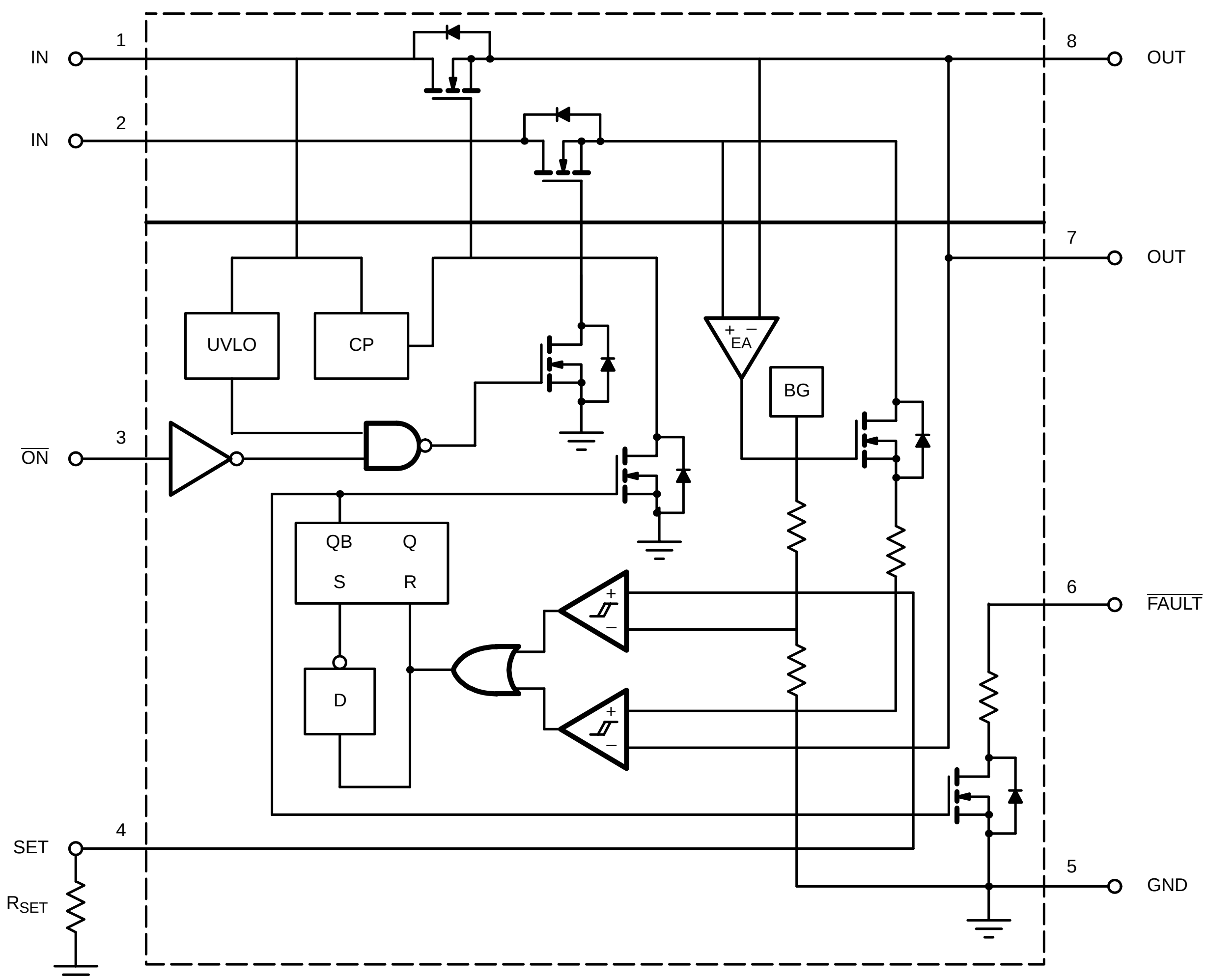


FIGURE 12.

DETAILED DESCRIPTION

The SI4779CY limits the output current to a user-defined level. When the output current passes through the main switch a fraction of this current passes through a replica switch and R_{SET}.

R_{SET} is an external sense resistor used to set the level of the over current limit; the over current limit should be set between 0.4 A and 2.4 A (see graph for R_{SET} value vs. current limit). The circuit shuts down the switch when the current flowing through the switch exceeds Ilimit. After a short period of time, the circuit will slowly turn on the switch again. The length of time off is based on average power consumption, which is designed to be kept under 500 mW.

If the output is shorted , the circuit will go into an on-off cycle to protect the switch and to prevent the battery from draining down.

The fault output ($\overline{\text{FAULT}}$) goes low when the circuit is in over current limit or short circuit protection mode. A 100-kΩ pull-up resistor from $\overline{\text{FAULT}}$ to IN provides a logic-control signal.

APPLICATIONS DIAGRAM

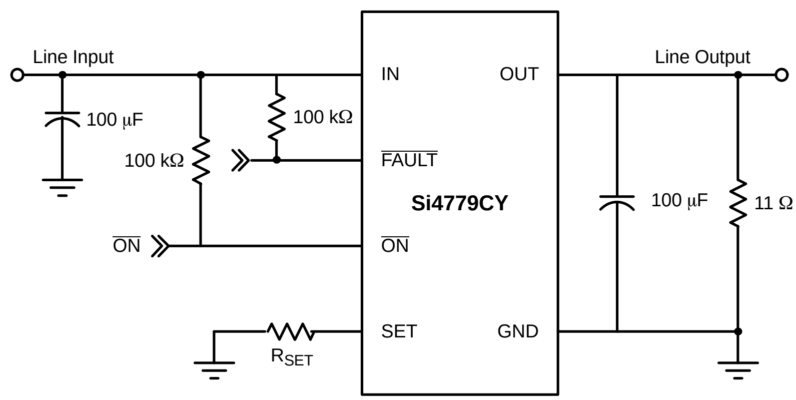


FIGURE 13.