P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-12	0.016 @ V_{GS} = -4.5 V	-13
	0.022 @ V_{GS} = -2.5 V	-11
	0.028 @ V_{GS} = -1.8 V	-9.8

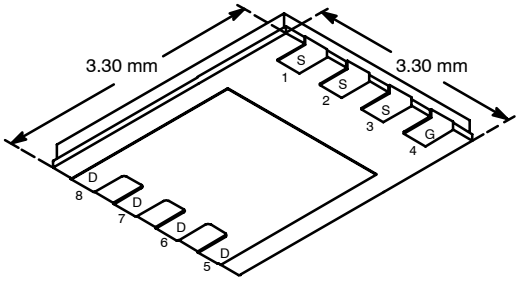
FEATURES

- TrenchFET® Power MOSFETS: 1.8-V Rated
- New PowerPAK® Package
  - Low Thermal Resistance, R_{thJC}
  - Low 1.07-mm Profile

APPLICATIONS

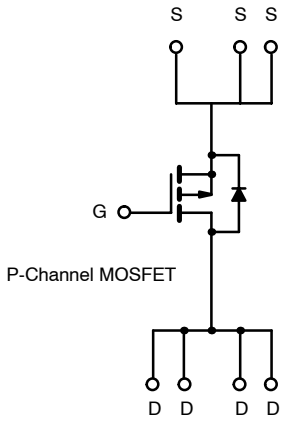
- Load Switch
- Power Switch
- PA Switch

PowerPAK 1212-8



Bottom View

Ordering Information: Si7405DN-T1



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	-12		V
Gate-Source Voltage		V_{GS}	±8		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	-13	-8.3	A
	T_A = 85°C		-9.4	-6.0	
Pulsed Drain Current		I_{DM}	-30		
continuous Source Current (Diode Conduction)[a]		I_S	-3.2	-1.3	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	3.8	1.5	W
	T_A = 85°C		2.0	0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	26	33	°C/W
	Steady State		65	81	
Maximum Junction-to-Case	Steady State	R_{thJC}	1.9	2.4	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

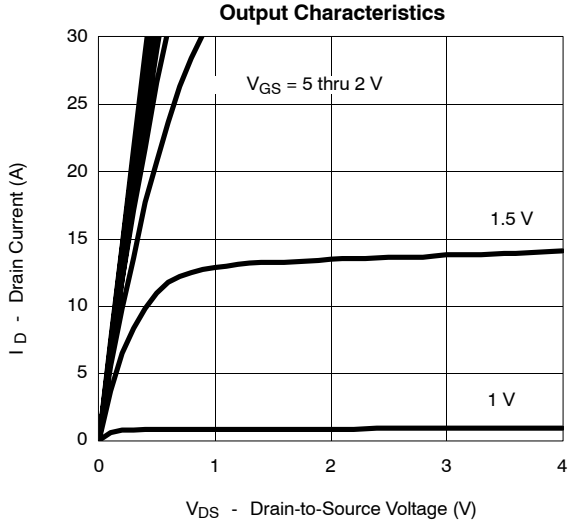
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -2 mA	-0.45			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -12 V, V_{GS} = 0 V			-1	µA
		V_{DS} = -12 V, V_{GS} = 0 V, T_J = 85°C			-5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ -5 V, V_{GS} = -4.5 V	-30			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = -4.5 V, I_D = -13 A		0.013	0.016	Ω
		V_{GS} = -2.5 V, I_D = -11 A		0.018	0.022	
		V_{GS} = -1.8 V, I_D = -3 A		0.022	0.028	
Forward Transconductance[a]	g_{fs}	V_{DS} = -6 V, I_D = -13 A		35		S
Diode Forward Voltage[a]	V_{SD}	I_S = -3.2 A, V_{GS} = 0 V		-0.7	-1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = -6 V, V_{GS} = -4.5 V, I_D = -13 A		35	50	nC
Gate-Source Charge	Q_{gs}			6.6		
Gate-Drain Charge	Q_{gd}			7.7		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -6 V, R_L = 6 Ω I_D ≅ -1 A, V_{GEN} = -4.5 V, R_G = 6 Ω		25	40	ns
Rise Time	t_r			50	75	
Turn-Off Delay Time	$t_{d(off)}$			175	260	
Fall Time	t_f			150	225	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = -3.2 A, di/dt = 100 A/µs		30	60	

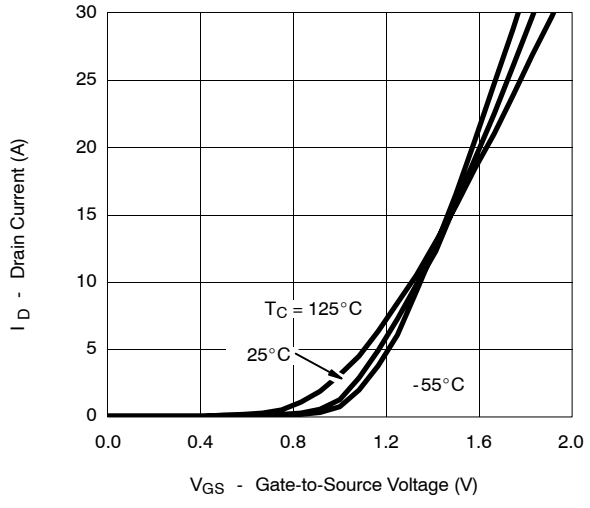
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

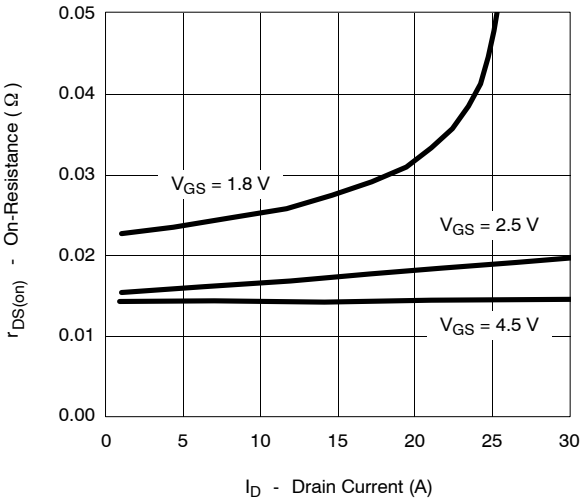


Transfer Characteristics

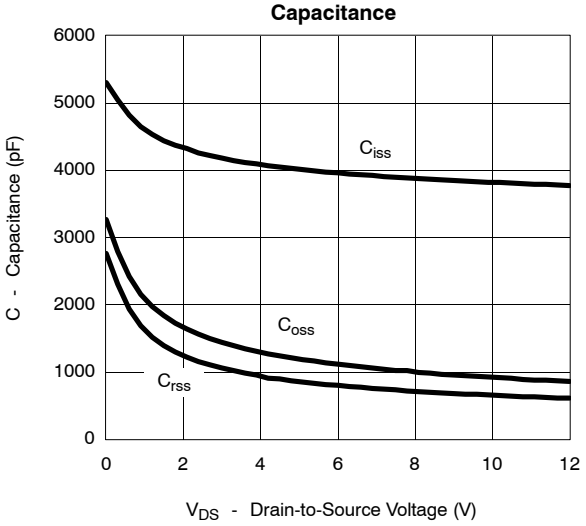


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

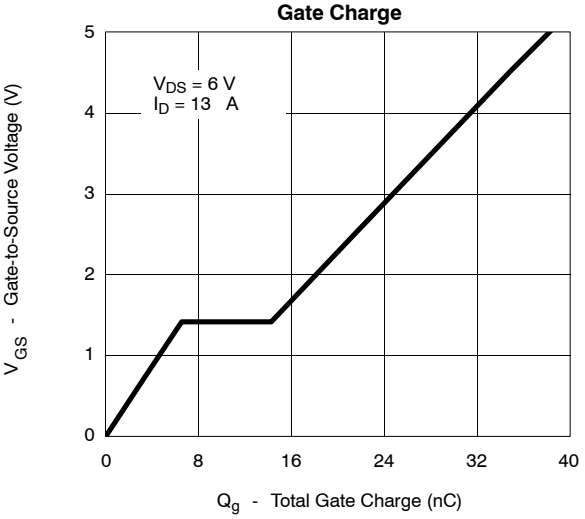
On-Resistance vs. Drain Current



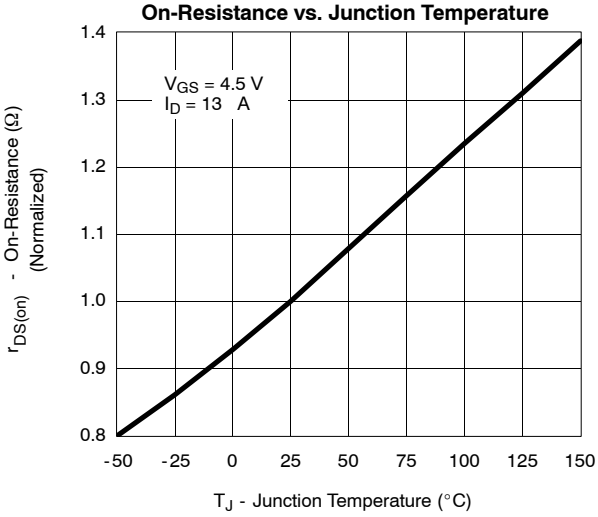
Capacitance



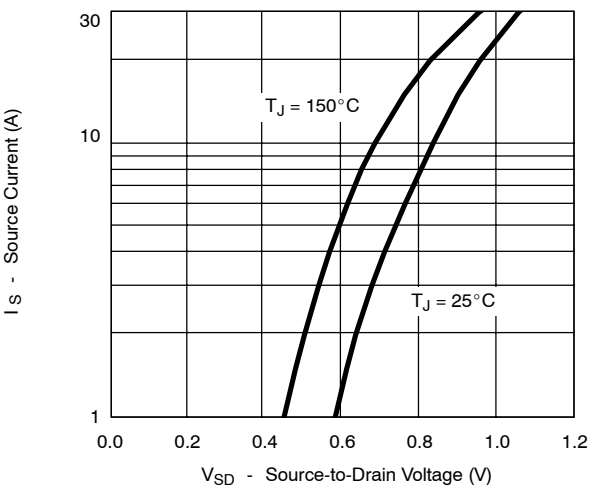
Gate Charge



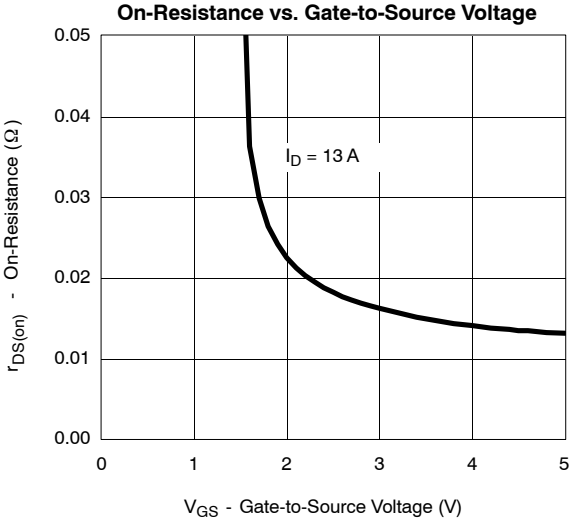
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

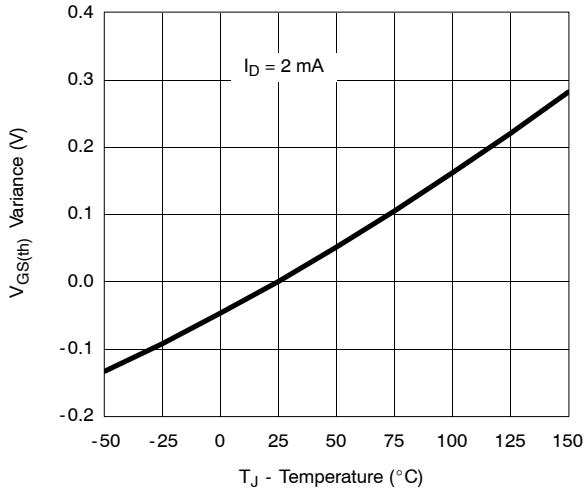


On-Resistance vs. Gate-to-Source Voltage

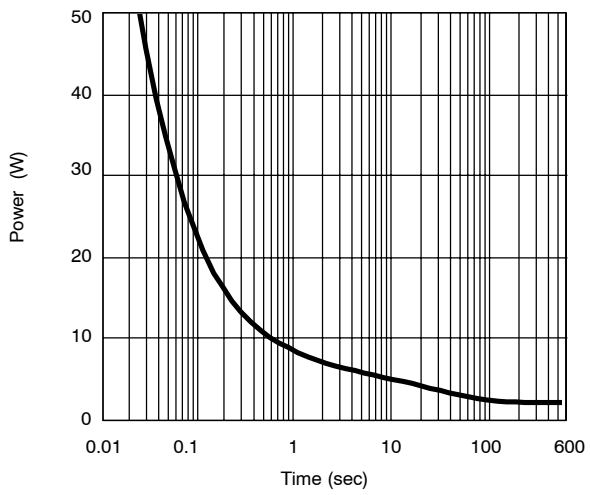


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

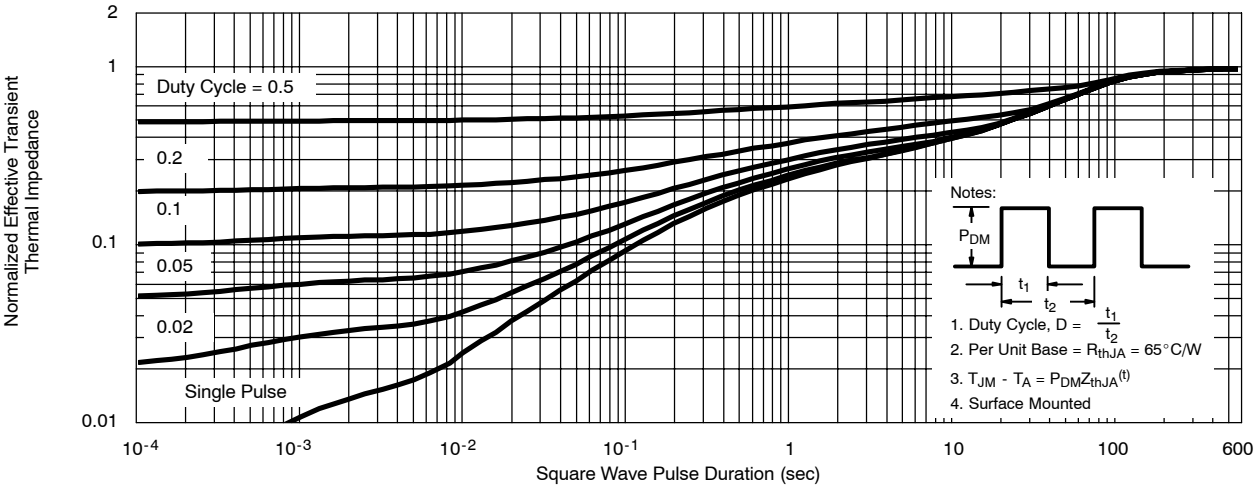
Threshold Voltage



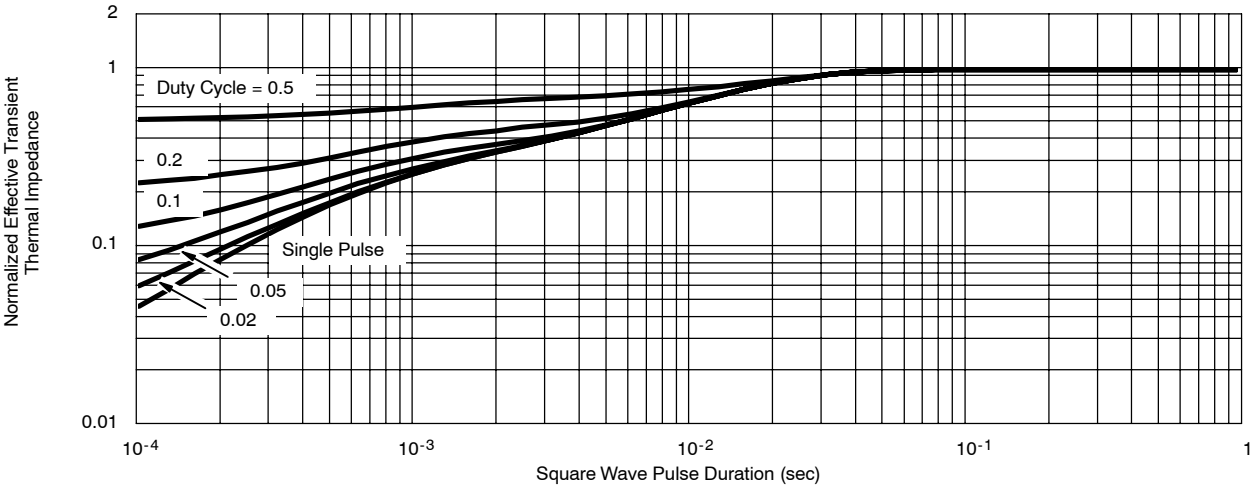
Single Pulse Power, Juncion-To-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case



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